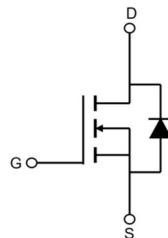


Description

Features <ul style="list-style-type: none"> ● 1000V, 2A ● $R_{DS(ON)} < 7.2\Omega$ @ $V_{GS} = 10V$ ● Fast Switching ● Improved dv/dt Capability 	Application <ul style="list-style-type: none"> ● Load Switch ● PWM Application ● Power management <p style="text-align: center;">100% UIS 100% ΔV_{ds}</p>
 TO-251	 Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	TUBE (PCS)	Inner Box (PCS)	Per Carton (PCS)
VSM2N100-T1	VSM2N100	TUBE	TO-251	80	4,000	32,000

Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise specified)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		1000	V
V_{GSS}	Gate-Source Voltage		± 30	V
I_D	Continuous Drain Current	$T_c = 25^\circ C$	2	A
		$T_c = 100^\circ C$	1.3	A
I_{DM}	Pulsed Drain Current ^{note1}		8	A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}		16.2	mJ
P_D	Power Dissipation	$T_c = 25^\circ C$	75	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.67	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient		60	$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ C$

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	1000	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=1000\text{V}$, $V_{GS}=0\text{V}$, $T_J=25^\circ\text{C}$	-	-	1	μA
I_{GSS}	Gate to Body Leakage Current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 30\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	3	3.5	4	V
$R_{DS(\text{on})}$	Static Drain-Source on-Resistance note3	$V_{GS}=10\text{V}$, $I_D=1\text{A}$	-	6	7.2	Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$	-	419	-	pF
C_{oss}	Output Capacitance		-	45	-	pF
C_{rss}	Reverse Transfer Capacitance		-	9	-	pF
Q_g	Total Gate Charge	$V_{DD}=800\text{V}$, $I_D=2\text{A}$, $V_{GS}=15\text{V}$	-	16	-	nC
Q_{gs}	Gate-Source Charge		-	2	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	8	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=500\text{V}$, $I_D=2\text{A}$, $R_G=25\Omega$	-	36	-	ns
t_r	Turn-on Rise Time		-	12	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	100	-	ns
t_f	Turn-off Fall Time		-	43	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	2	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	8	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS}=0\text{V}$, $I_{SD}=1\text{A}$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS}=0\text{V}$, $I_S=2\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$	-	432.5	-	ns
Q_{rr}	Reverse Recovery Charge		-	424	-	μC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: $T_J = 25^\circ\text{C}$, $V_{DD} = 50\text{V}$, $V_G = 10\text{V}$, $L = 10\text{mH}$, $I_{AS} = 1.8\text{A}$

3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 1\%$

Typical Performance Characteristics

Figure 1: Output Characteristics

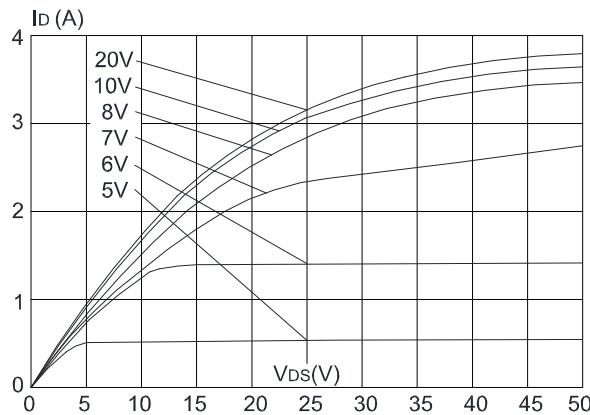


Figure 2: Typical Transfer Characteristics

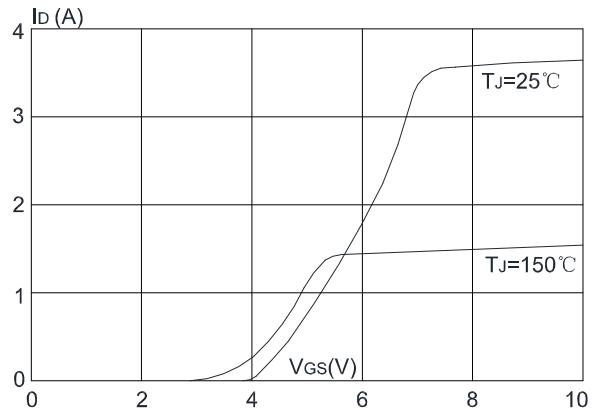


Figure 3: On-resistance vs. Drain Current

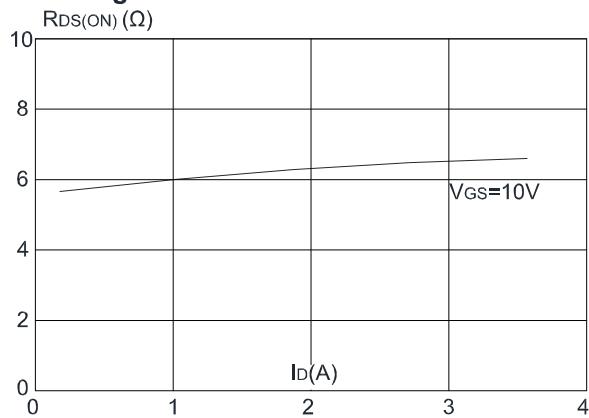


Figure 5: Gate Charge Characteristics

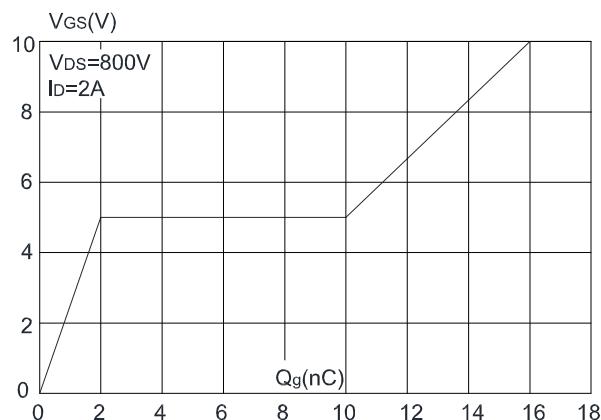


Figure 4: Body Diode Characteristics

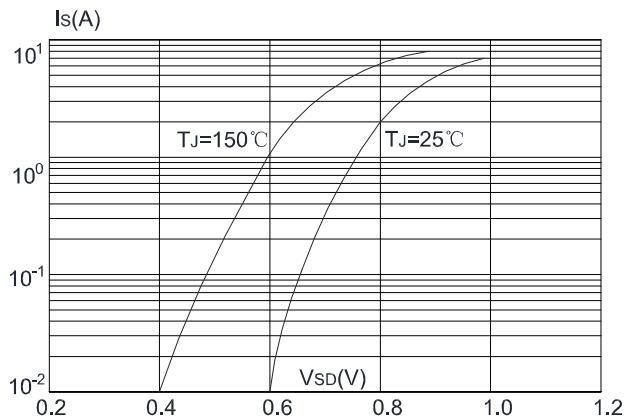


Figure 6: Capacitance Characteristics

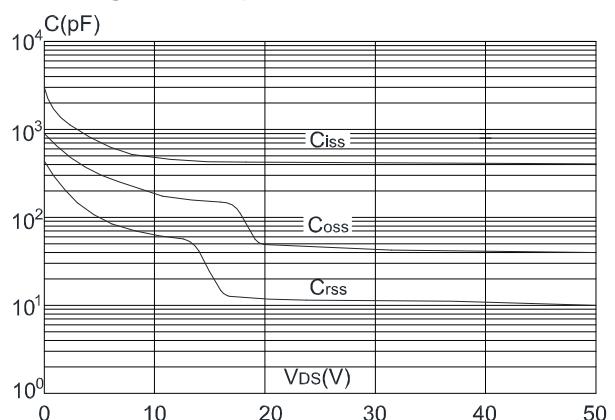


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

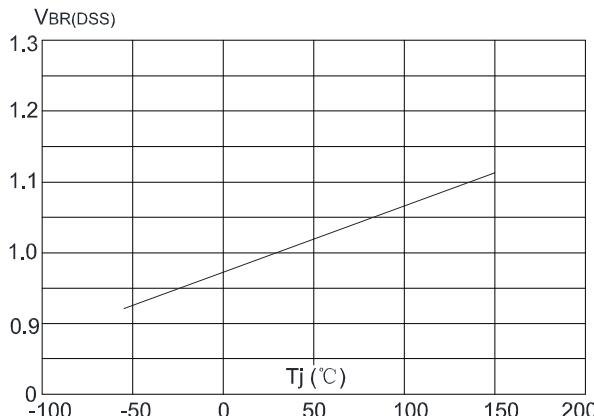


Figure 8: Normalized on Resistance vs. Junction Temperature

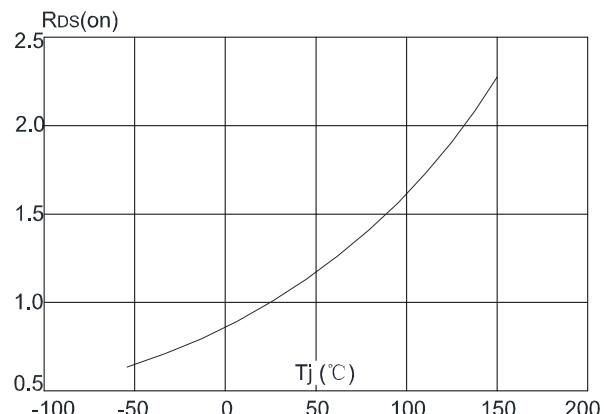


Figure 9: Maximum Safe Operating Area

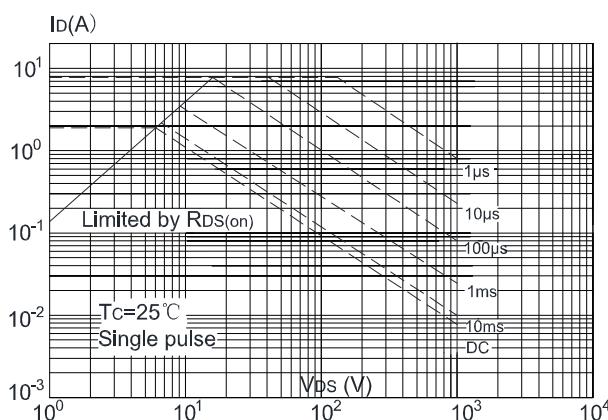


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

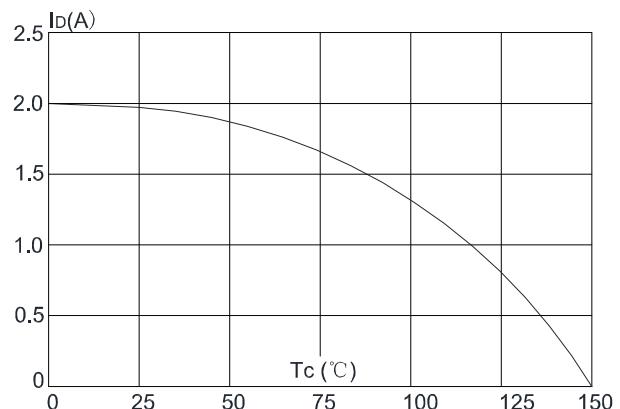
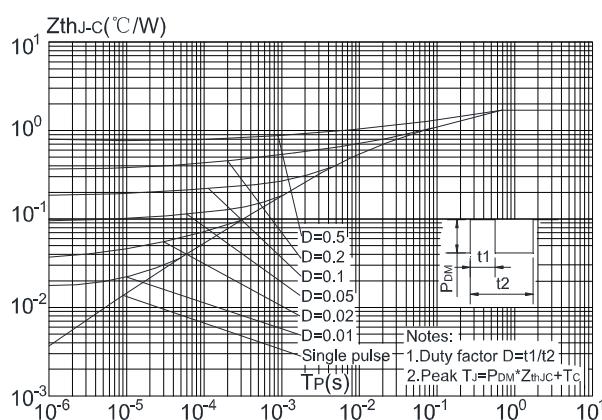


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



Test Circuit

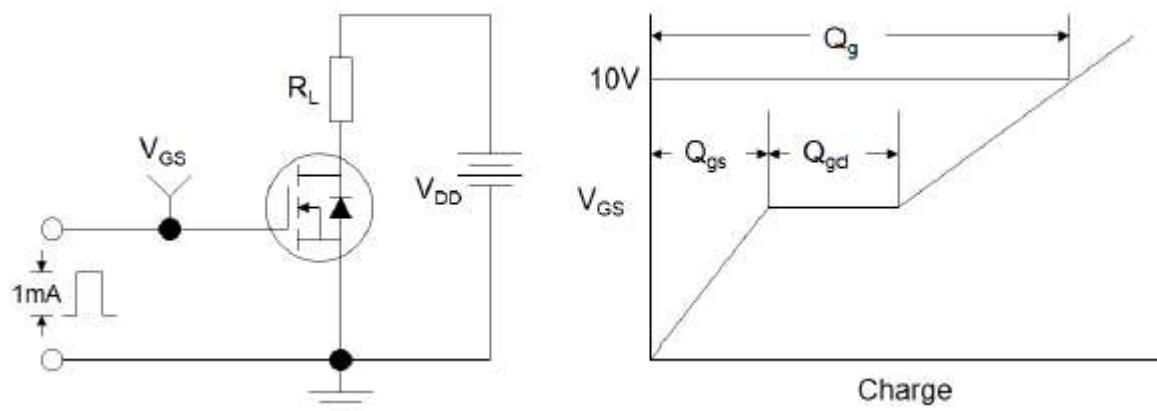


Figure1:Gate Charge Test Circuit & Waveform

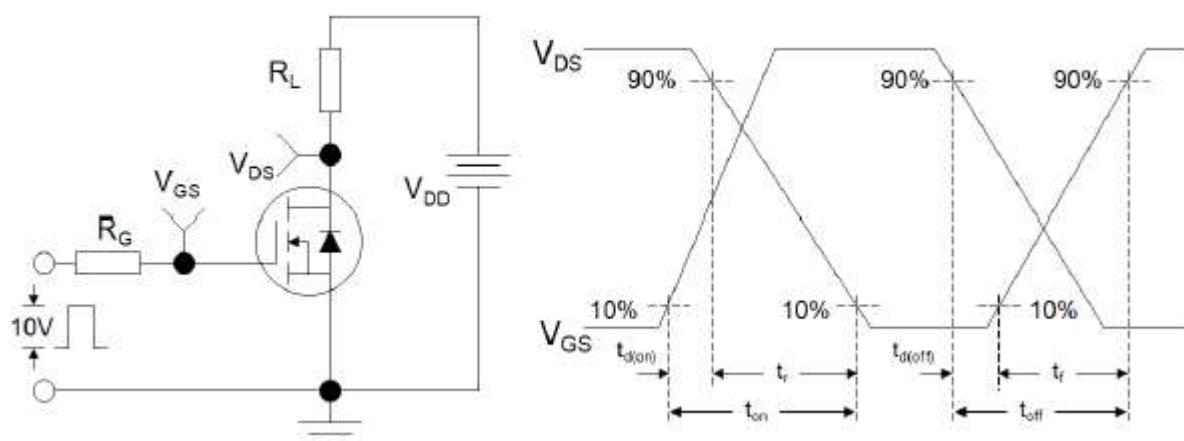


Figure 2: Resistive Switching Test Circuit & Waveforms

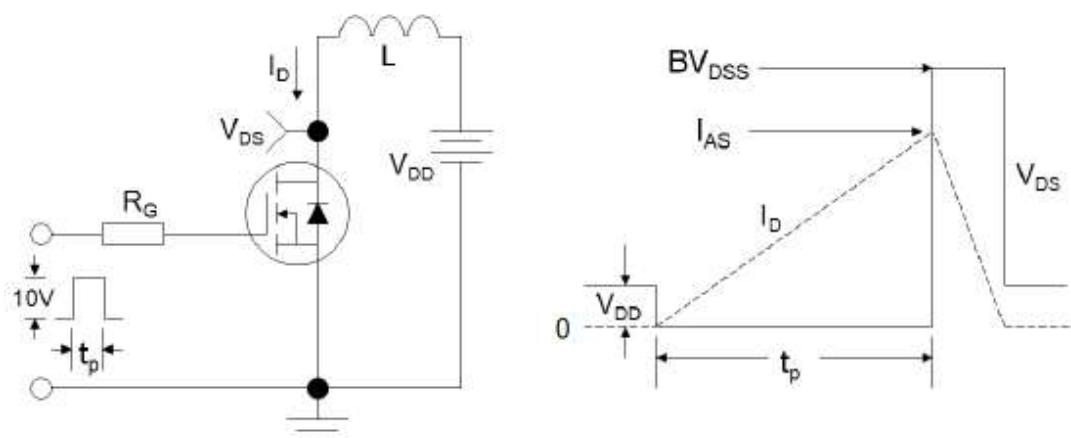


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms