

Description

Features

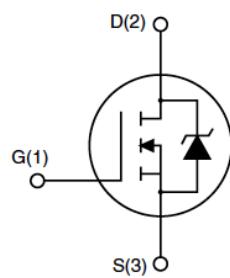
- 100V, 33A
- $R_{DS(ON)}=30m\Omega$ @ $V_{GS} = 10V$
- Fast Switching
- 100% Avalanche Tested
- Improved dv/dt Capability

Application

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)



TO-220C



Schematic Diagram

Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise specified)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		100	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current	$T_c = 25^\circ C$	33	A
		$T_c = 100^\circ C$	23	A
I_{DM}	Pulsed Drain Current ^{note1}		110	A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}		185	mJ
P_D	Power Dissipation	$T_c = 25^\circ C$	130	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.15	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient		62	$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	$^\circ C$

Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 100\text{V}, V_{GS} = 0\text{V}$	-	-	1	μA
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D = 250\mu\text{A}$	2.0	-	4.0	V
$R_{DS(\text{on})}$	Static Drain-Source On-Resistance note3	$V_{GS} = 10\text{V}, I_D = 16\text{A}$	-	30	44	$\text{m}\Omega$
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$	-	1960	-	pF
C_{oss}	Output Capacitance		-	250	-	pF
C_{rss}	Reverse Transfer Capacitance		-	40	-	pF
Q_g	Total Gate Charge	$V_{DS} = 80\text{V}, I_D = 16\text{A}, V_{GS} = 10\text{V}$	-	-	71	nC
Q_{gs}	Gate-Source Charge		-	-	14	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	-	21	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{V}, I_D = 16\text{A}, R_G = 5.1\Omega, V_{GS} = 10\text{V}$	-	11	-	ns
t_r	Turn-On Rise Time		-	35	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	39	-	ns
t_f	Turn-Off Fall Time		-	35	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	33	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	110	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 16\text{A}, T_J = 25^\circ\text{C}$	-	-	1.2	V
t_{rr}	Reverse Recovery Time	$T_J = 25^\circ\text{C}, I_F = 16\text{A}, dI/dt = 100\text{A}/\mu\text{s}$	-	115	170	ns
Q_{rr}	Reverse Recovery Charge		-	505	760	uC

Notes: 1. Repetitive Rating: Pulse width limited by maximum junction temperature

2. $I_{AS} = 16\text{A}, L = 1.5\text{mH}, R_G = 25\Omega$ Starting $T_J = 175^\circ\text{C}$

3. Pulse Test: Pulse width $\leq 400\mu\text{s}$, Duty Cycle $\leq 2\%$

Typical Performance Characteristics

Figure1: Output Characteristics

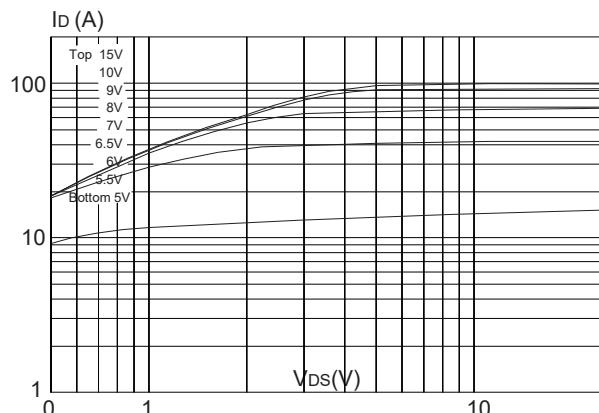


Figure 3: On-resistance vs. Drain Current

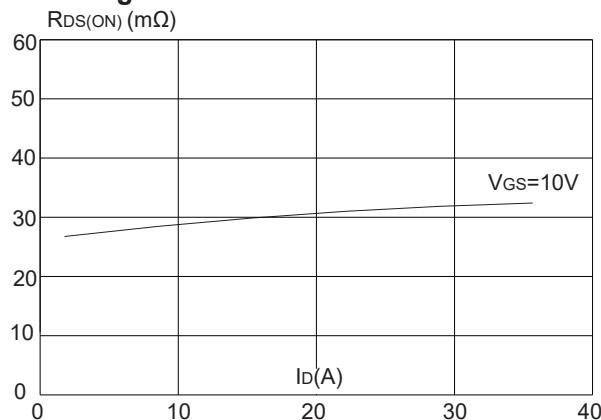


Figure 5: Gate Charge Characteristics

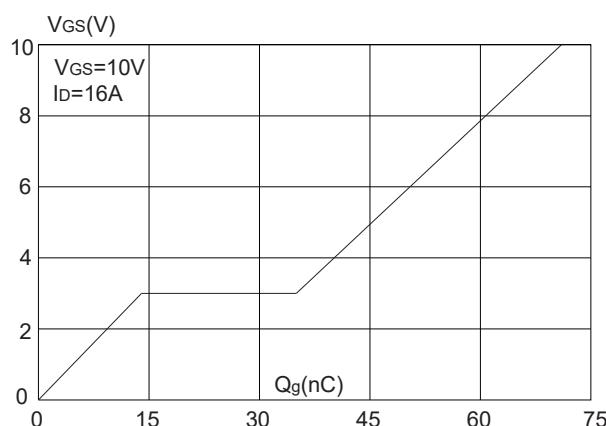


Figure 2: Typical Transfer Characteristics

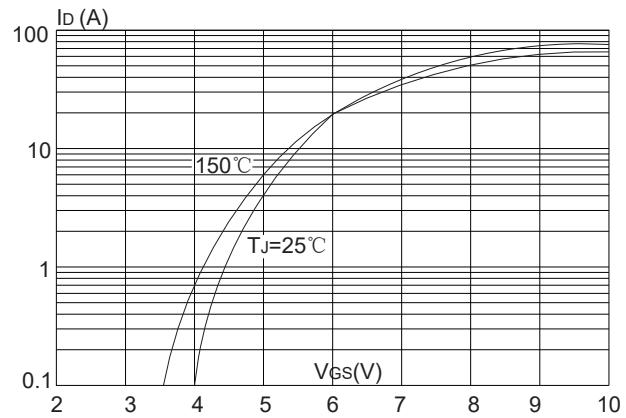


Figure 4: Body Diode Characteristics

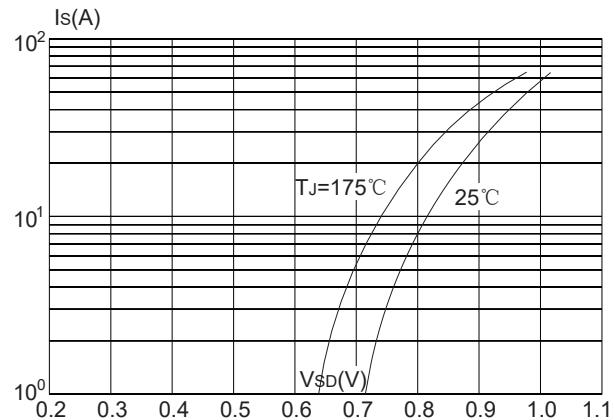


Figure 6: Capacitance Characteristics

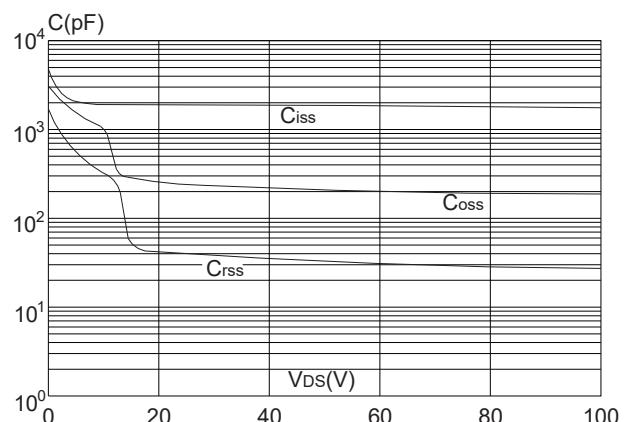


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

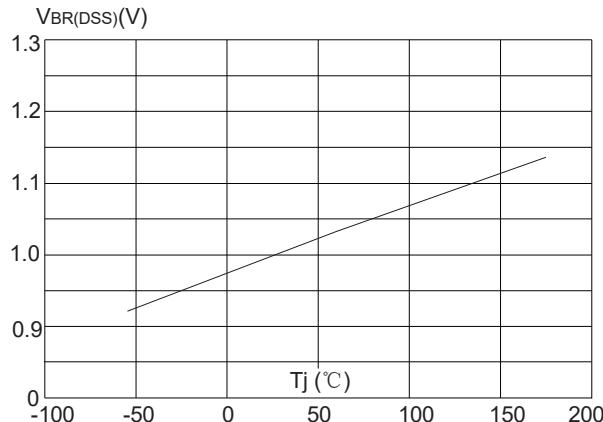


Figure 8: Normalized on Resistance vs. Junction Temperature

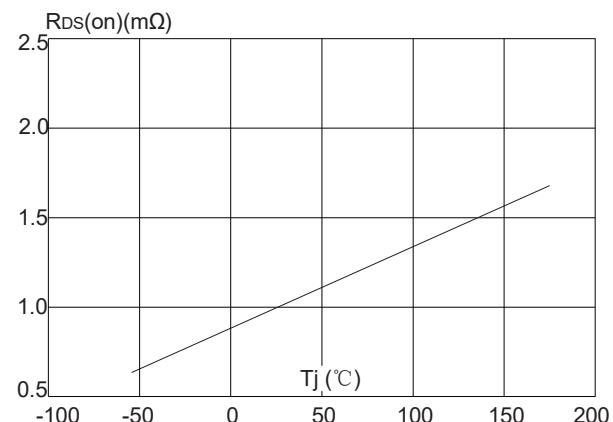


Figure 9: Maximum Safe Operating Area

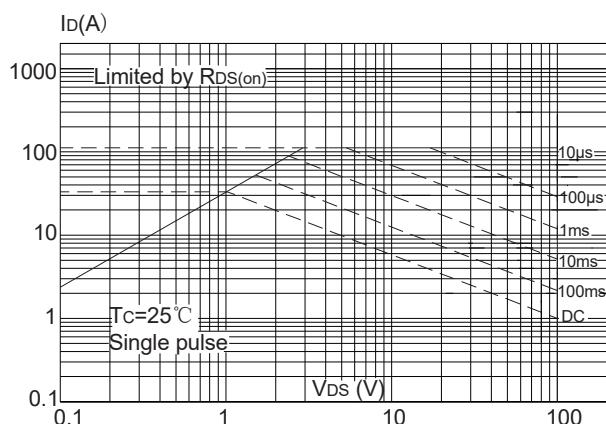


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

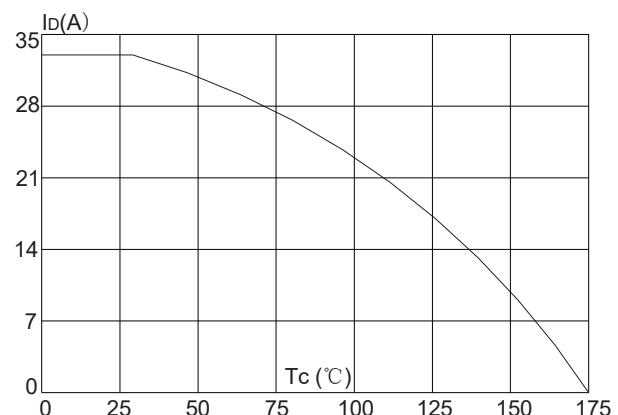
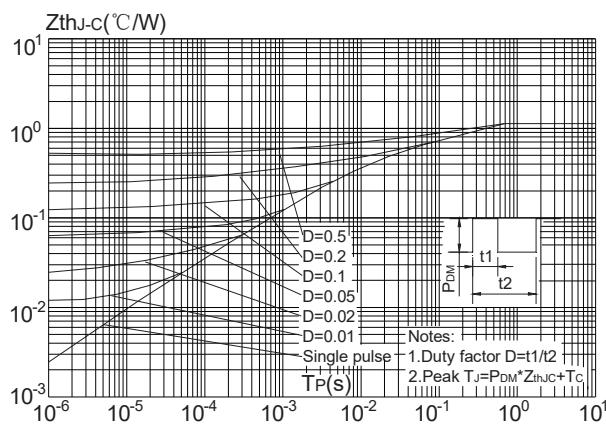


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case (TO-220C, TO-263)



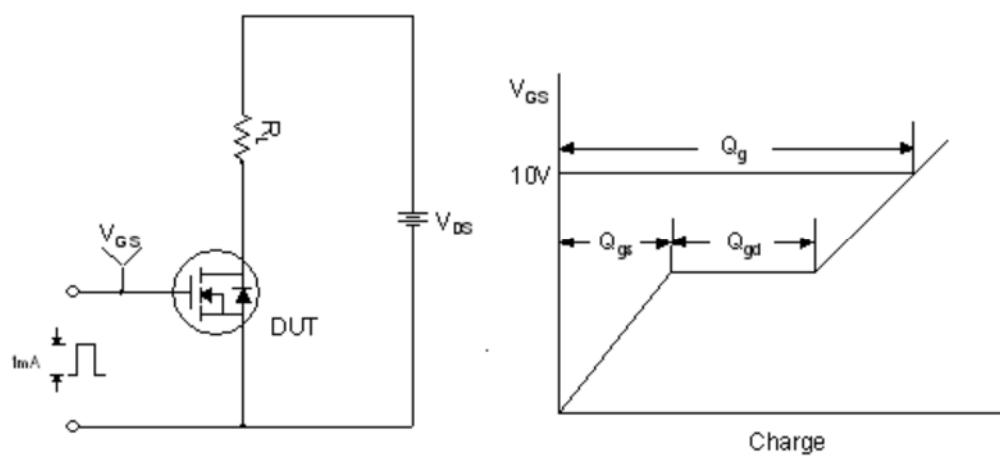


Figure 1. Gate Charge Test Circuit & Waveform

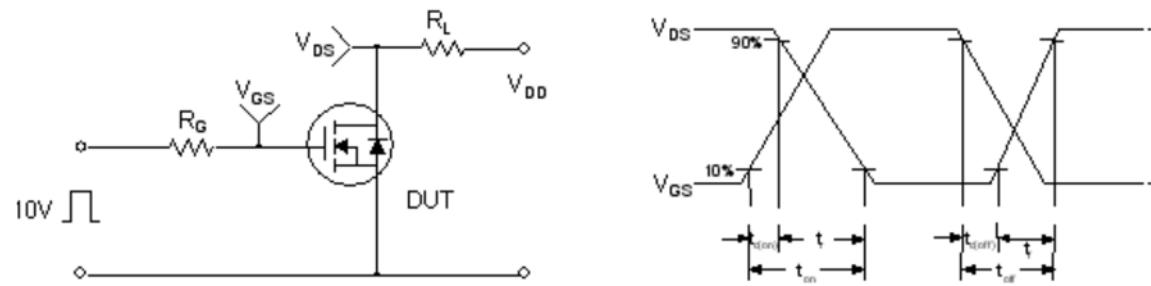


Figure 2. Resistive Switching Test Circuit & Waveforms

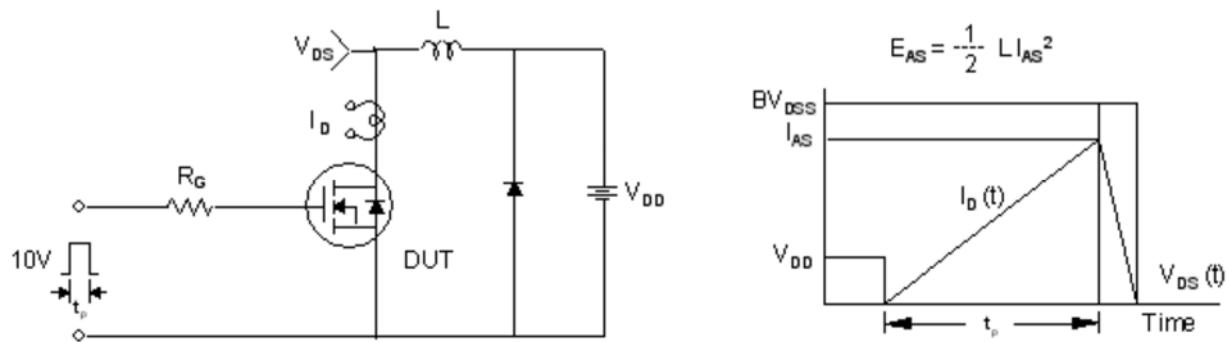
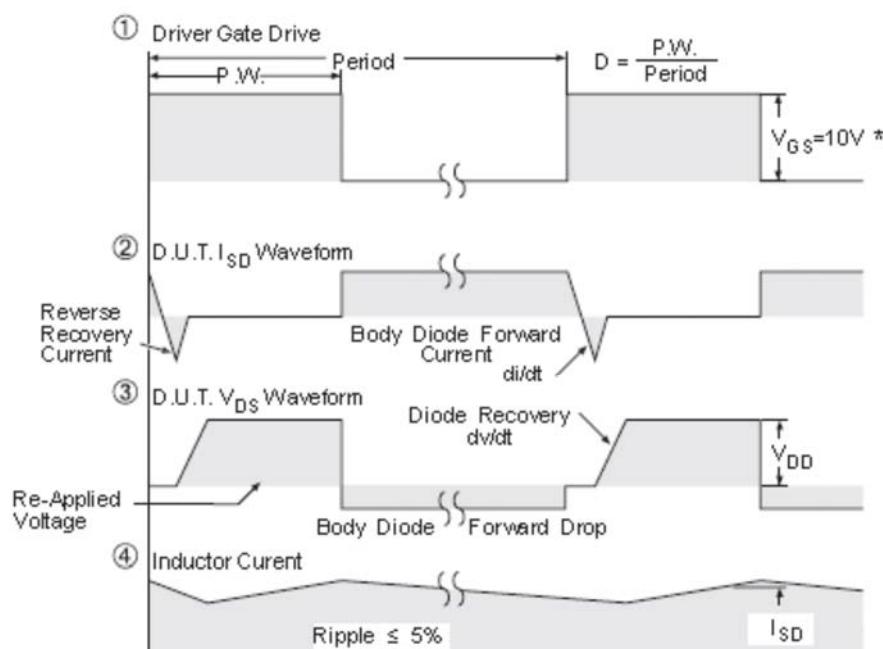
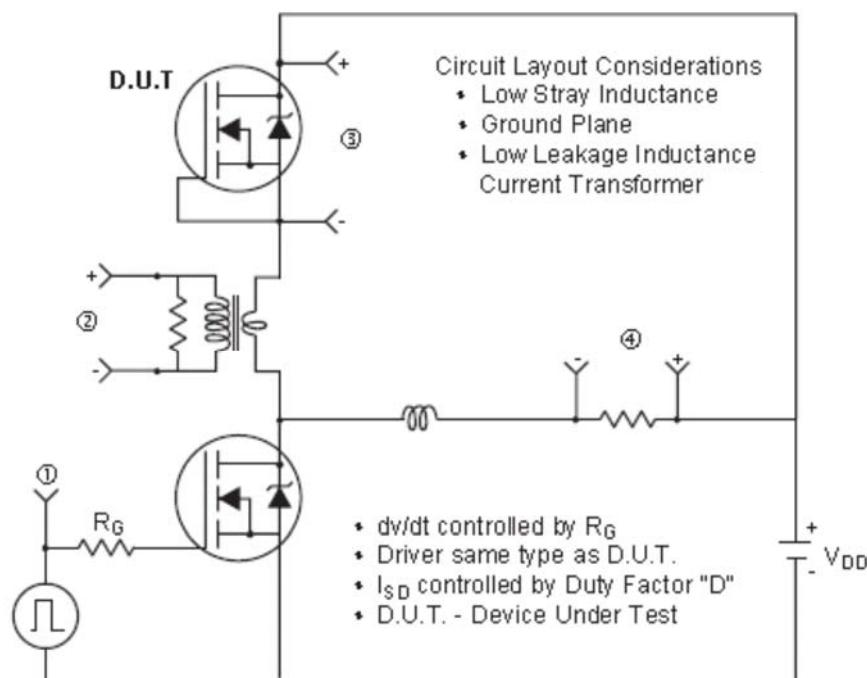


Figure 3. Unclamped Inductive Switching Test Circuit & Waveforms



* $V_{GS} = 5V$ for Logic Level Devices

Figure 4. Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)