Description

The VSM3N10 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge.This device is suitable for use in inverter and other applications.

Genera Features

N-channel

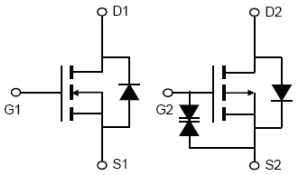
- V_{DS} = 100V,I_D = 3A
  $R_{DS(ON)}$ <130mΩ @ V_{GS}=10V
  $R_{DS(ON)}$ <140mΩ @ V_{GS}=4.5V

P-channel

- V_{DS} = -100V,I_D =- 3A
  $R_{DS(ON)}$ <200mΩ @ V_{GS}=-10V
  $R_{DS(ON)}$ <230mΩ @ V_{GS}=-4.5V

- High Power and current handing capability
- Lead free product is acquired

SOP-8



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM3N10-S8	VSM3N10	SOP-8	Ø330mm	12mm	4000 units

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter		Symbol	N-channel	P-channel	Unit
Drain-Source Voltage		V_{DS}	100	-100	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Drain Current-Continuous (Note 2)	T_A=25°C	I_D	3	-3	A
	T_A=70°C		2.45	-2.45	A
Drain Current -Pulsed (Note 1)		I_{DM}	12	-12	
Power Dissipation	T_A=25°C	P_D	2	2	W
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55 To 150	-55 To 150	℃

Thermal Characteristic

Parameter	Symbol	Typ	Max	Unit
Thermal Resistance,Junction-to-Ambient (Note 2) **(N-channel)**	$R_{\theta JA}$	-	62.5	℃/W
Thermal Resistance,Junction-to-Ambient (Note 2) **(P-channel)**	$R_{\theta JA}$	-	62.5	℃/W

N-channel Electrical Characteristics (T_C=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	100	110	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.0	1.5	2.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=3A	-	95	130	mΩ
		V_{GS}=4.5V, I_D=3A		100	140	
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=3A	3.5	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=50V,V_{GS}=0V, F=1.0MHz	-	730	-	PF
Output Capacitance	C_{oss}		-	37	-	PF
Reverse Transfer Capacitance	C_{rss}		-	27	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=50V, R_L=15Ω V_{GS}=10V,R_G=2.5Ω	-	11	-	nS
Turn-on Rise Time	t_r		-	7.4	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	35	-	nS
Turn-Off Fall Time	t_f		-	9.1	-	nS
Total Gate Charge	Q_g	V_{DS}=50V,I_D=3A, V_{GS}=10V	-	21.5		nC
Gate-Source Charge	Q_{gs}		-	3.2	-	nC
Gate-Drain Charge	Q_{gd}		-	6	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=3A	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	3	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF =3A di/dt = 100A/μs(Note3)	-	26		nS
Reverse Recovery Charge	Qrr		-	27		nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.

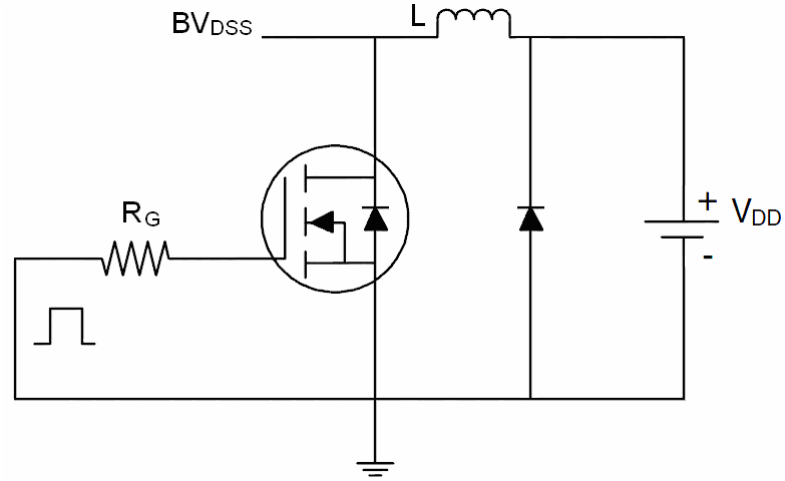
2. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design.Surface Mounted on FR4 Board, t ≤ 10 sec. The current rating is based on the t ≤ 10s thermal resistance rating.

3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

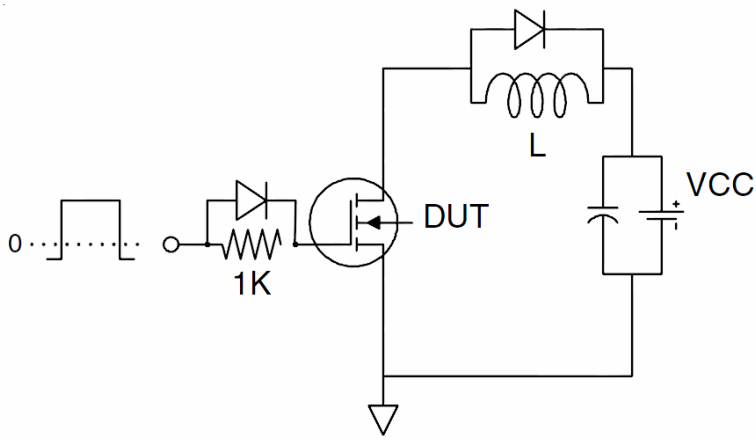
4. Guaranteed by design, not subject to production .

Test Circuit

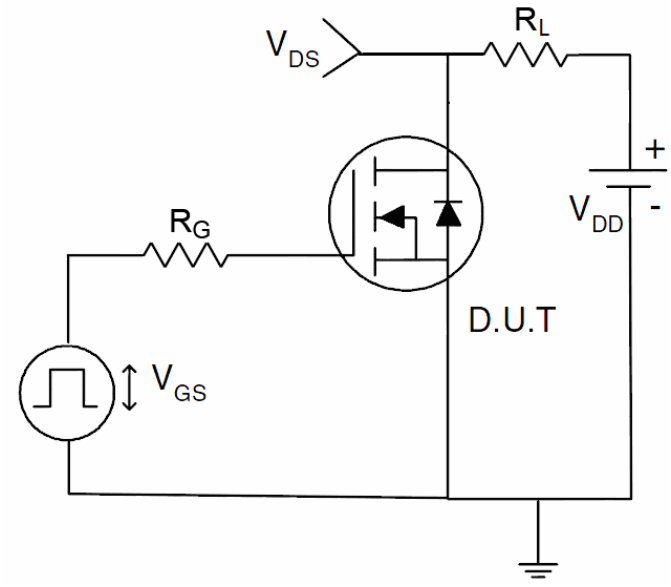
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



N-channelTypical Electrical and Thermal Characteristics (Curves)

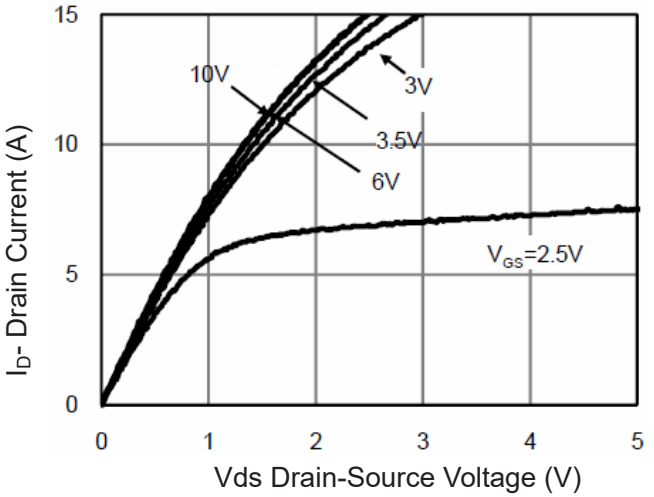


Figure 1 Output Characteristics

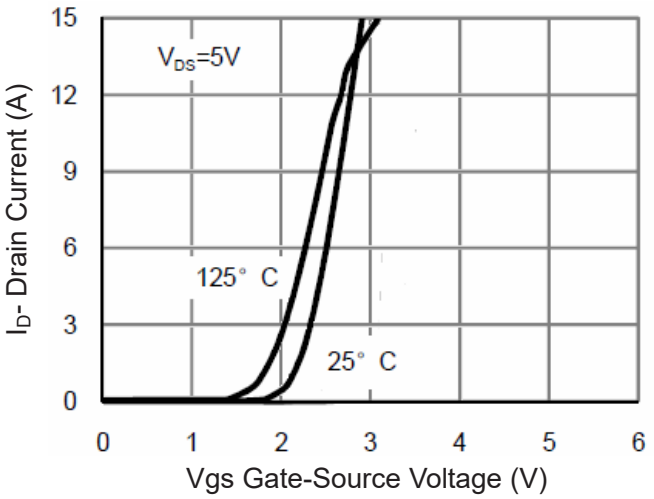


Figure 2 Transfer Characteristics

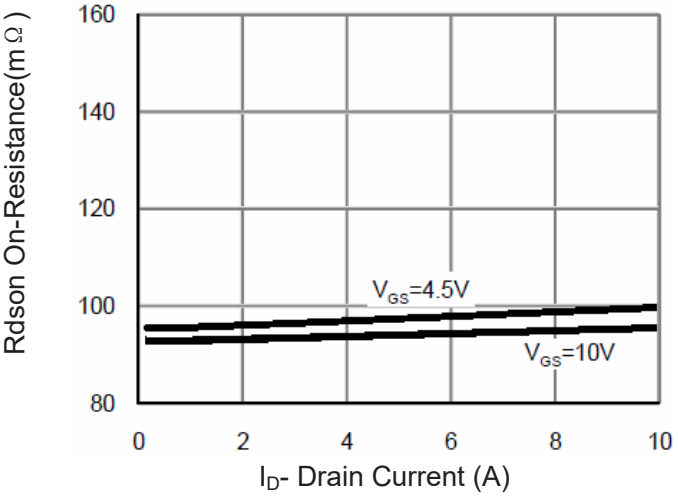


Figure 3 Rdson- Drain Current

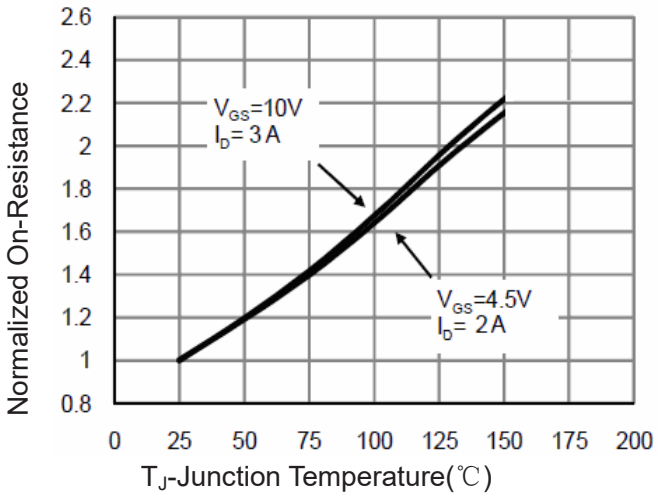


Figure 4 Rdson-Junction Temperature

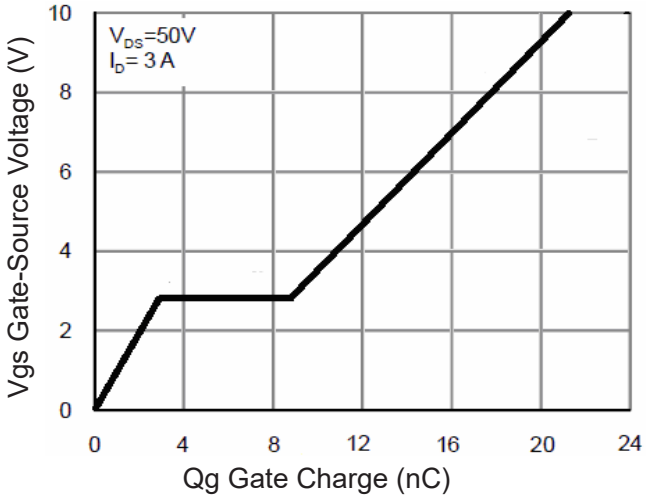


Figure 5 Gate Charge

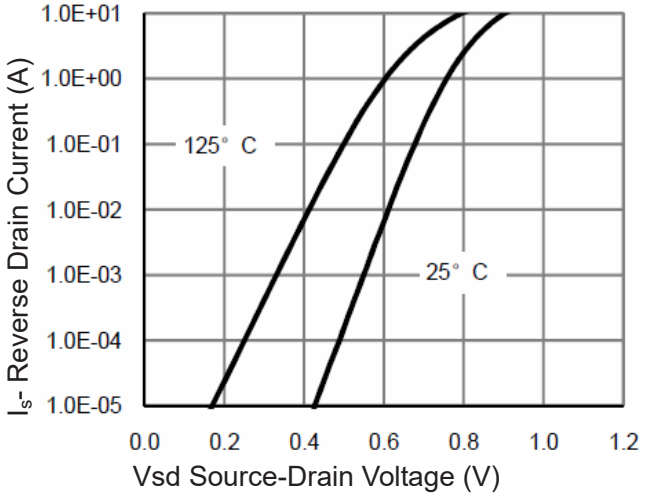


Figure 6 Source- Drain Diode Forward

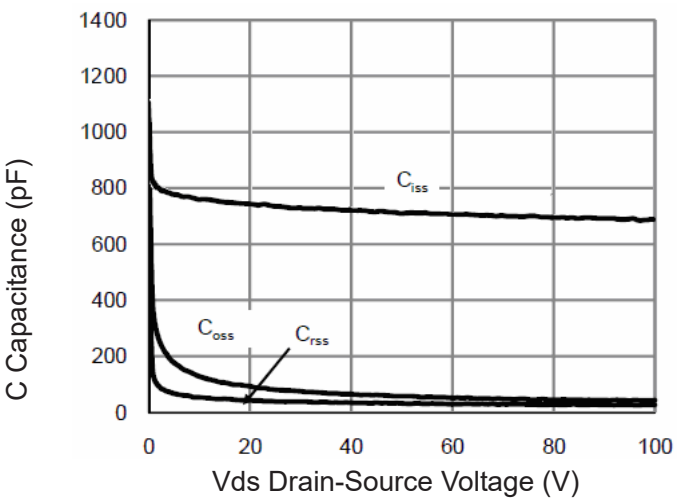


Figure 7 Capacitance vs Vds

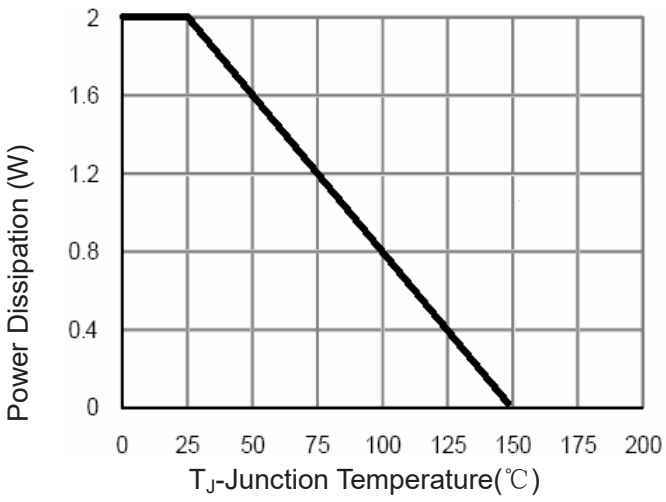


Figure 9 Power De-rating

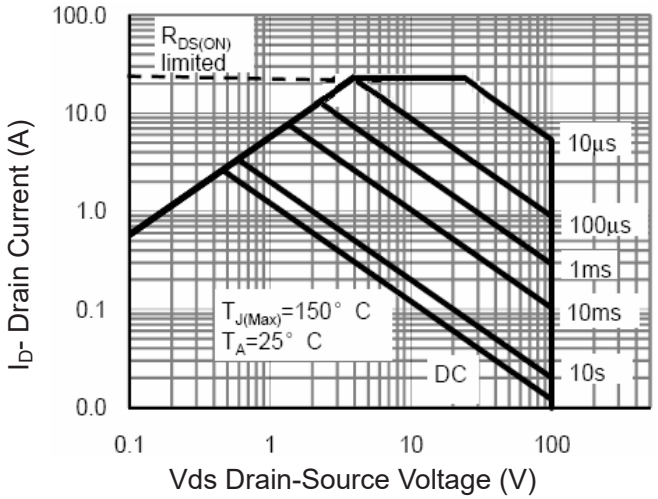


Figure 8 Safe Operation Area

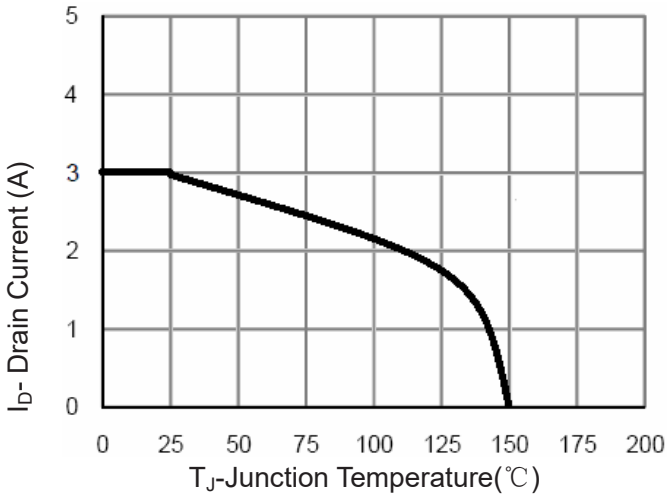


Figure 10 Current De-rating

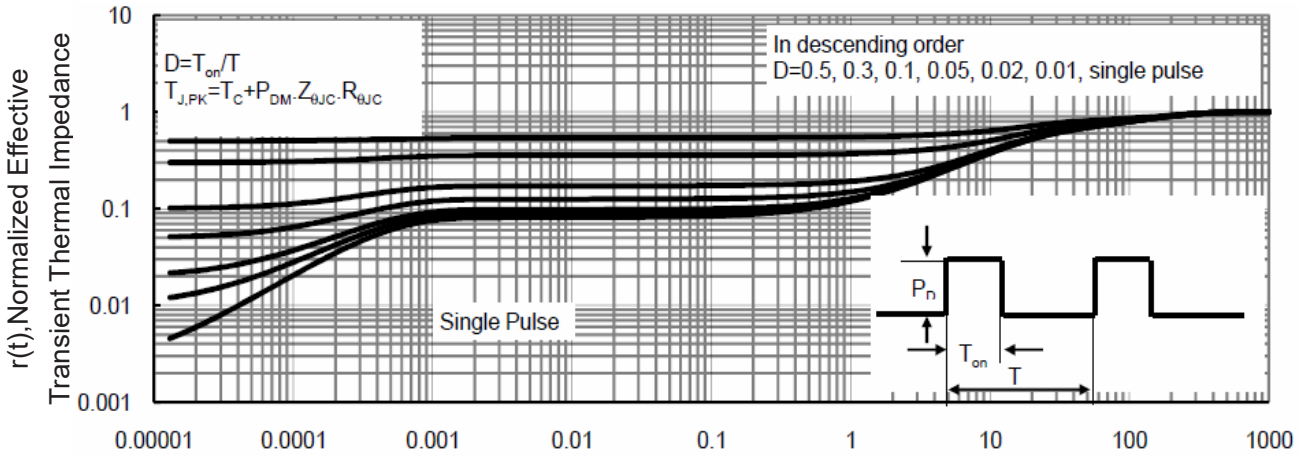


Figure 11 Normalized Maximum Transient Thermal Impedance

P-channel Electrical Characteristics (T_A=25℃unless otherwise noted)

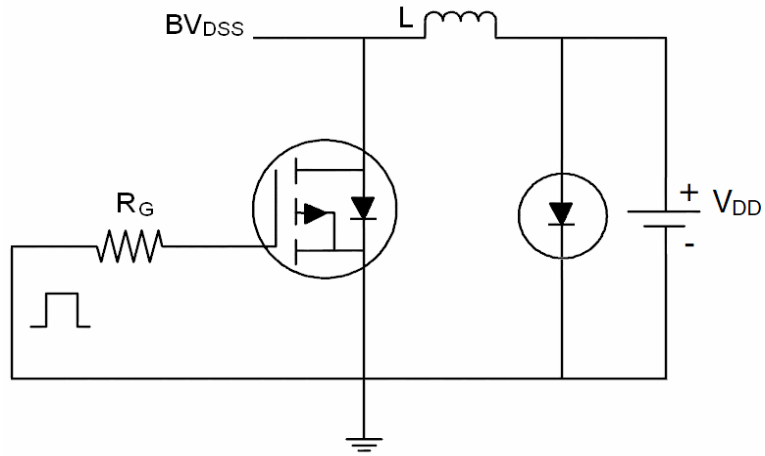
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-100V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±10	μA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-1	-1.9	-3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-3A	-	170	200	mΩ
		V_{GS}=-4.5V, I_D=-2A		200	230	
Forward Transconductance	g_{FS}	V_{DS}=-5V,I_D=-3A	2	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=-25V,V_{GS}=0V, F=1.0MHz	-	760	-	PF
Output Capacitance	C_{oss}		-	260	-	PF
Reverse Transfer Capacitance	C_{rss}		-	170	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-50V,I_D=-3A V_{GS}=-10V,R_{GEN}=9Ω	-	14	-	nS
Turn-on Rise Time	t_r		-	18	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	50	-	nS
Turn-Off Fall Time	t_f		-	18	-	nS
Total Gate Charge	Q_g	V_{DS}=-50V,I_D=-3A, V_{GS}=-10V	-	25	-	nC
Gate-Source Charge	Q_{gs}		-	5	-	nC
Gate-Drain Charge	Q_{gd}		-	7	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=-3A	-	-	-1.2	V
Diode Forward Current (Note 2)	I_S	-	-	-	-3	A
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F =-3A di/dt = 100A/μs (Note3)	-	35	-	nS
Reverse Recovery Charge	Qrr		-	46	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

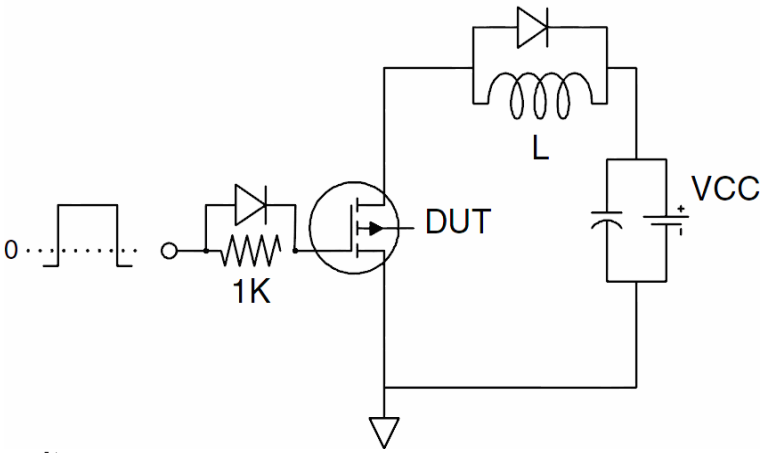
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. E_{AS} condition：Tj=25℃,V_{DD}=-50V,V_G=-10V,L=0.5mH,Rg=25Ω

Test Circuit

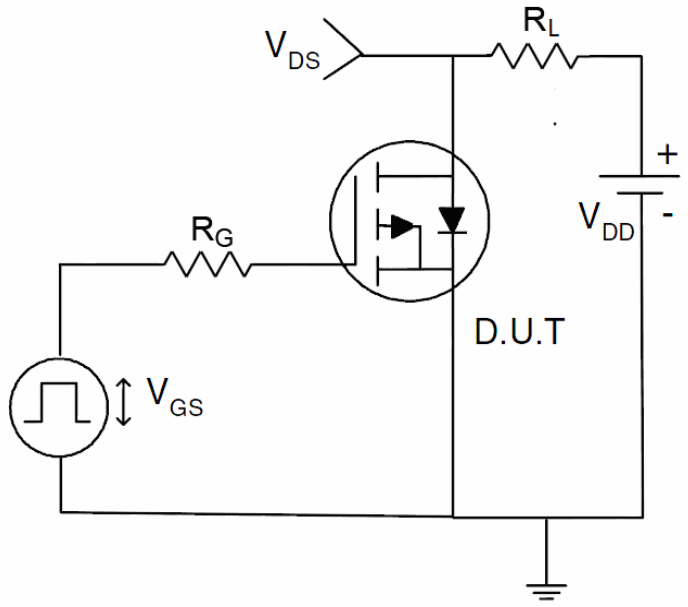
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

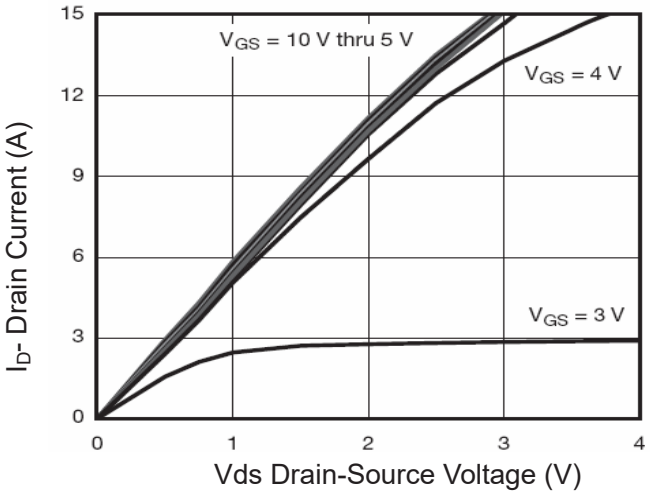


Figure 1 Output Characteristics

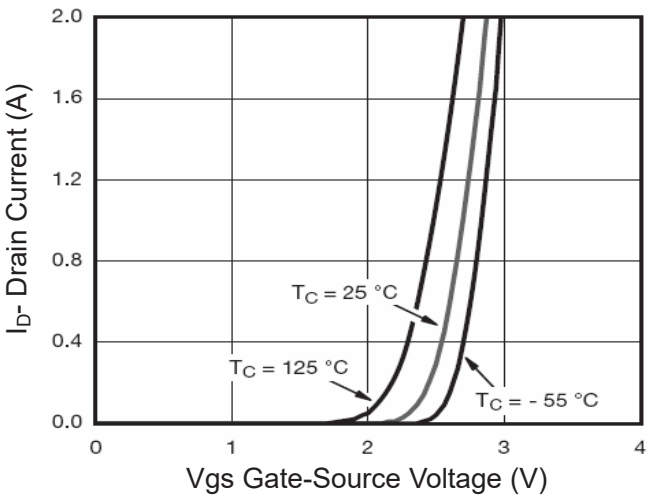


Figure 2 Transfer Characteristics

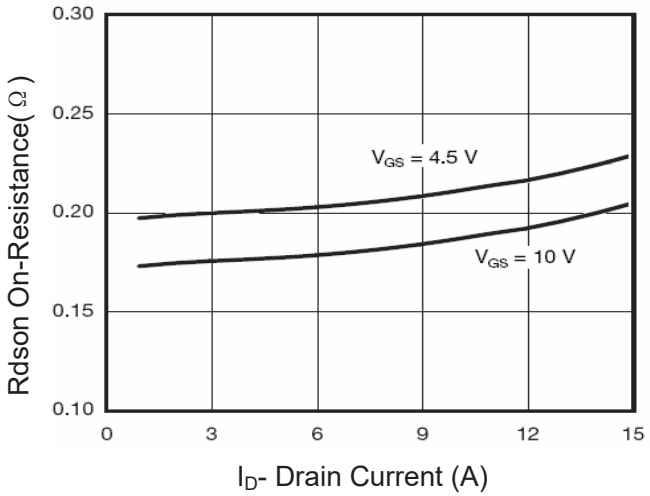


Figure 3 Rdson- Drain Current

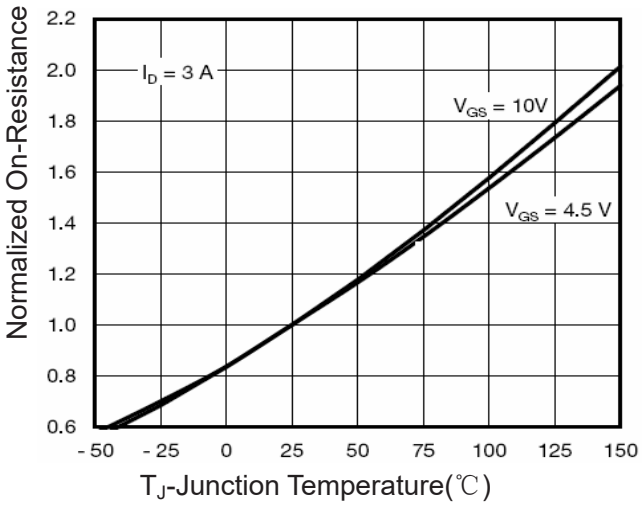


Figure 4 Rdson-JunctionTemperature

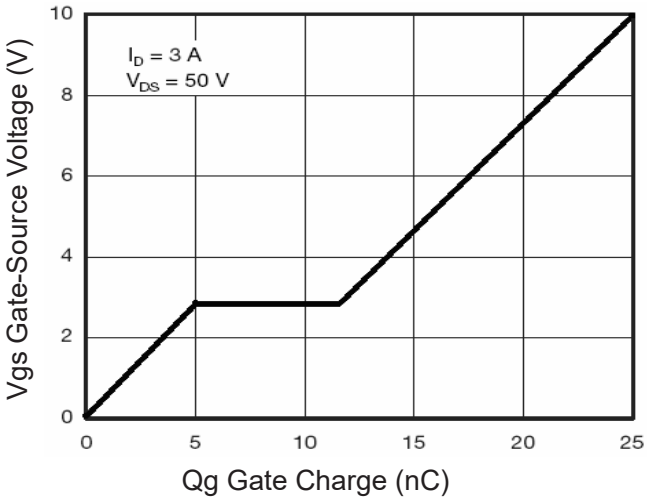


Figure 5 Gate Charge

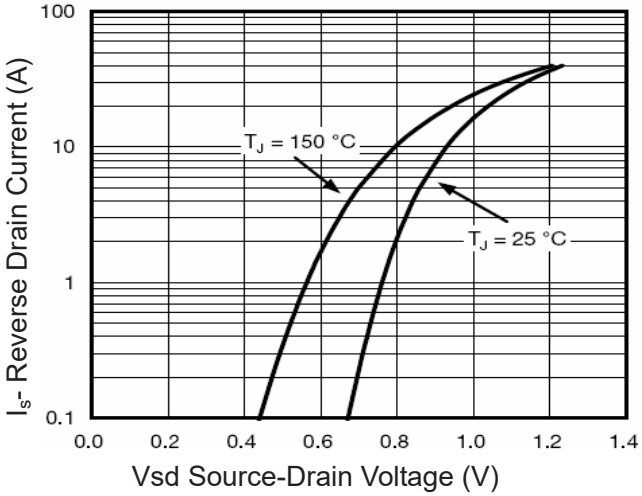


Figure 6 Source- Drain Diode Forward

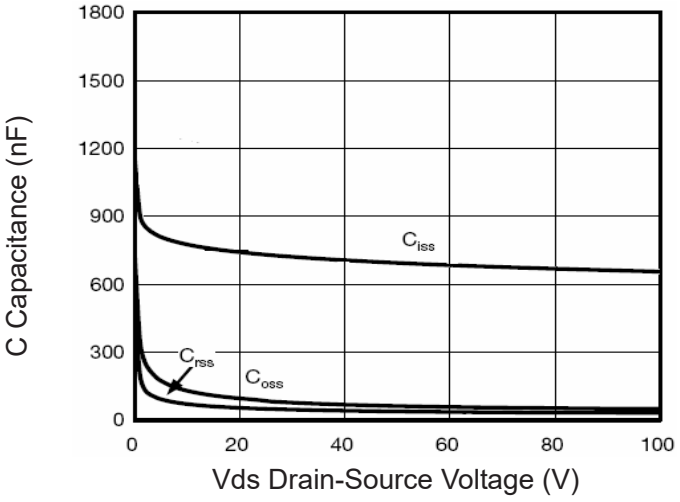


Figure 7 Capacitance vs Vds

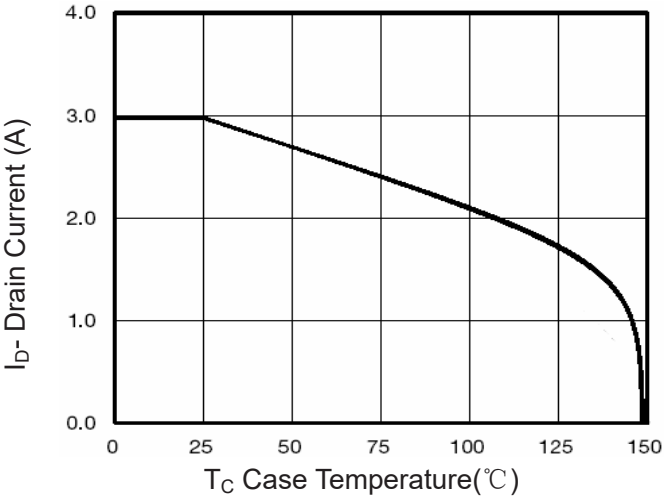


Figure 9 Drain Current vs Case Temperature

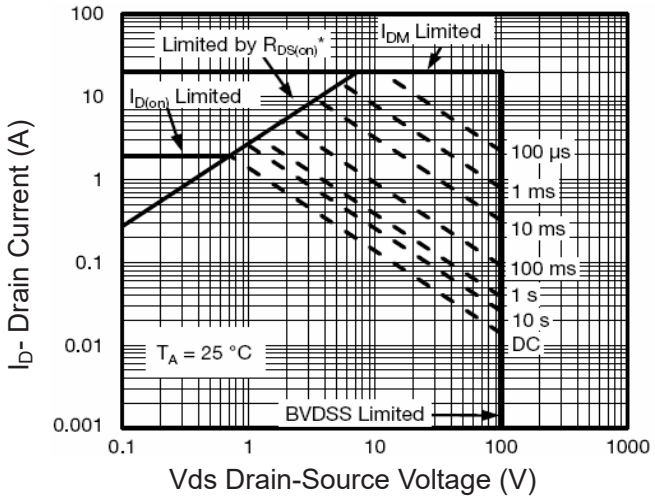


Figure 8 Safe Operation Area

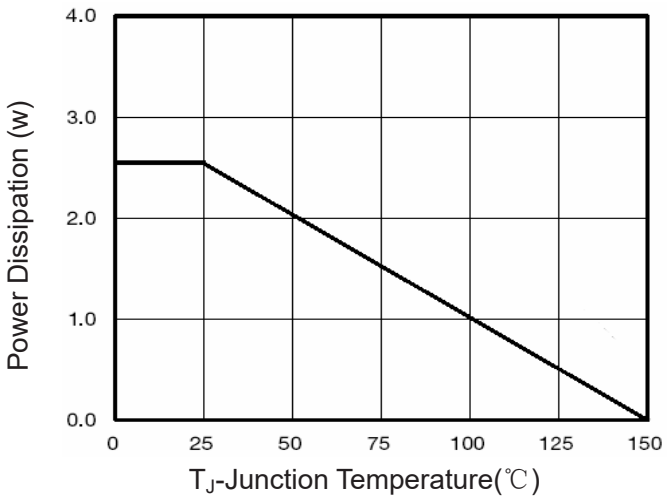


Figure 10 Power De-rating

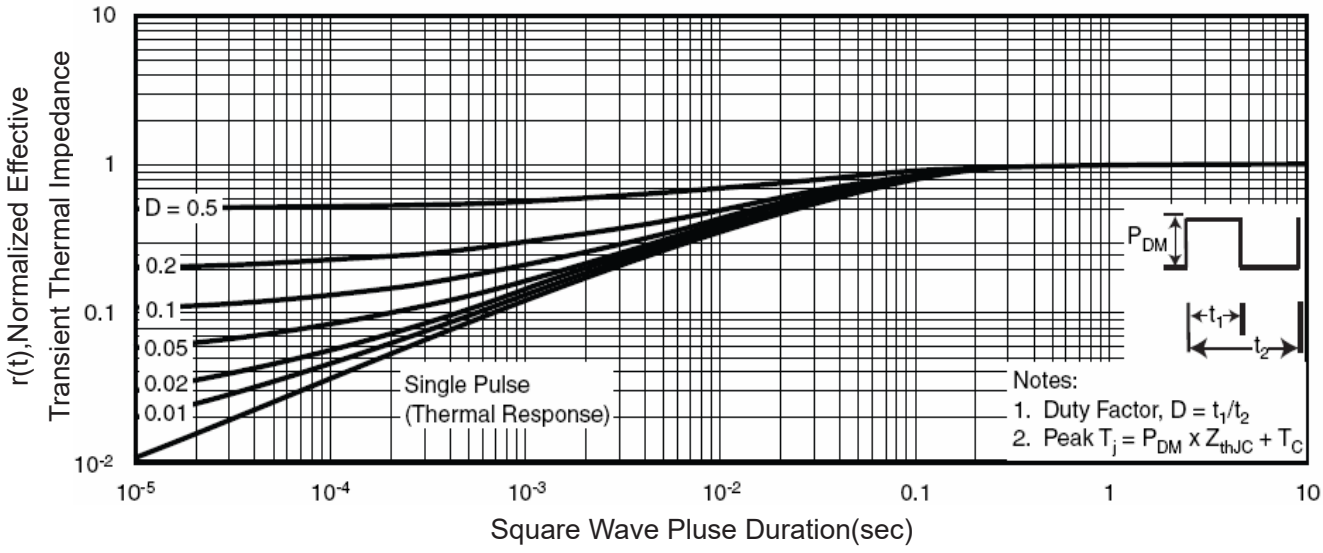


Figure 11 Normalized Maximum Transient Thermal Impedance