Description

The VSM80N07 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.

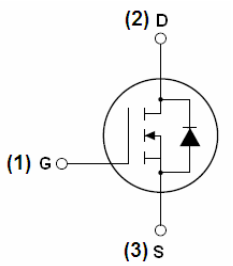
General Features

- V_{DS} = 75V,I_D =80A
  $R_{DS(ON)}$ <8mΩ @ V_{GS}=10V（Typ：6.5mΩ）
- Special process technology for high ESD capability
- Special designed for Convertors and power controls
- High density cell design for ultra low Rdson
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

TO-263



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM80N07-T3	VSM80N07	TO-263	-	-	-

Absolute Maximum Ratings (TA=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	75	V
Gate-Source Voltage	V_{GS}	±25	V
Drain Current-Continuous	I_D	80	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	60	A
Pulsed Drain Current	I_{DM}	320	A
Maximum Power Dissipation	P_D	170	W
Peak diode recovery voltage	dv/dt	15	V/ns
Derating factor		1.13	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	580	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to- Case (Note 2)	$R_{\theta Jc}$	0.88	℃/W

Electrical Characteristics (T_A=25℃unless otherwise noted)

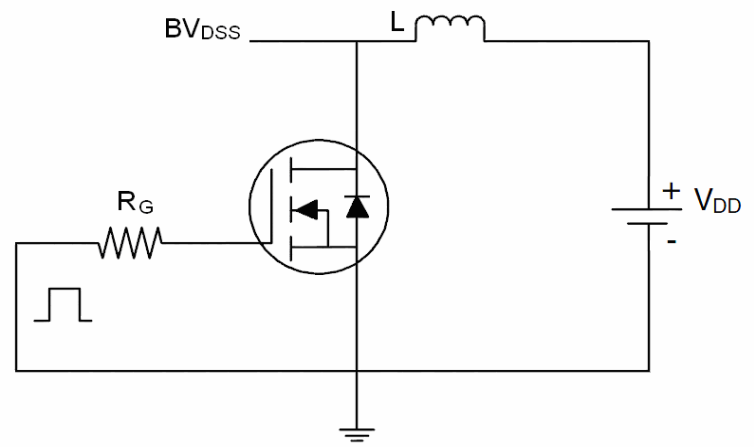
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	75	84	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±25V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2	2.85	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=30A	-	6.5	8	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=30A	-	60	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=25V,V_{GS}=0V, F=1.0MHz		4400		PF
Output Capacitance	C_{oss}			340		PF
Reverse Transfer Capacitance	C_{rss}			260		PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=30V,I_D=2A,R_L=15Ω V_{GS}=10V,R_G=2.5Ω		17.8		nS
Turn-on Rise Time	t_r			11.8		nS
Turn-Off Delay Time	$t_{d(off)}$			56		nS
Turn-Off Fall Time	t_f			14.6		nS
Total Gate Charge	Q_g	V_{DS}=30V,I_D=30A, V_{GS}=10V		100		nC
Gate-Source Charge	Q_{gs}			20		nC
Gate-Drain Charge	Q_{gd}			30		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=40A	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	80	A
Reverse Recovery Time	t_{rr}	Tj=25℃,I_{SD}=40A,V_{GS}=0V			36	nS
Reverse Recovery Charge	Qrr	Tj=25℃,I_F=75A,di/dt=100A/μs			56	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

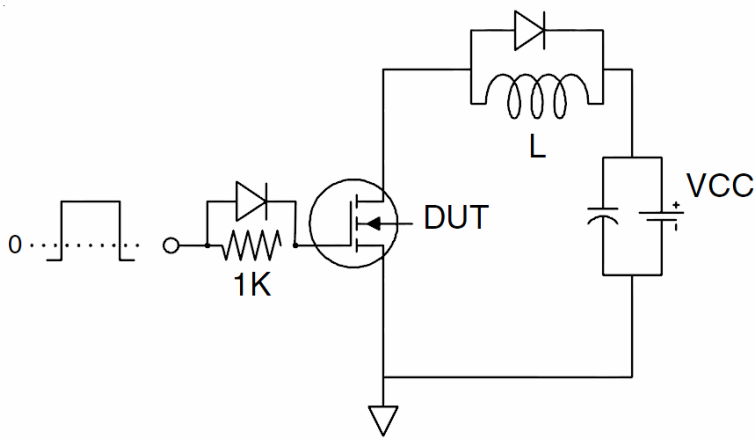
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition：Tj=25℃,V_{DD}=50V,V_G=10V,L=0.5mH, I_D=62A

Test circuit

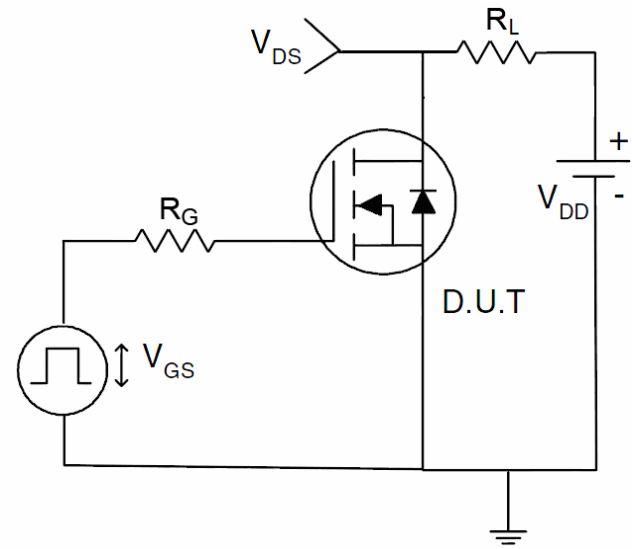
1）E_{AS} test Circuits



2）Gate charge test Circuit



3）Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (curves)

Figure1. Safe operating area

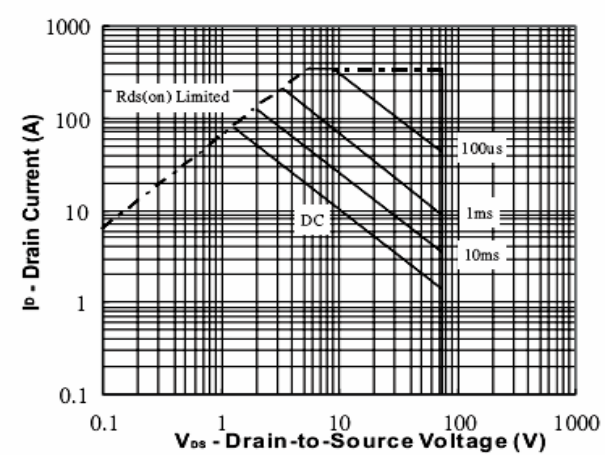


Figure2. Source-Drain Diode Forward Voltage

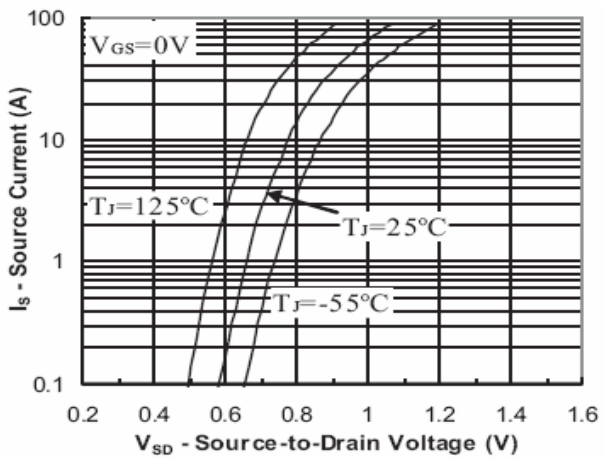


Figure3. Output characteristics

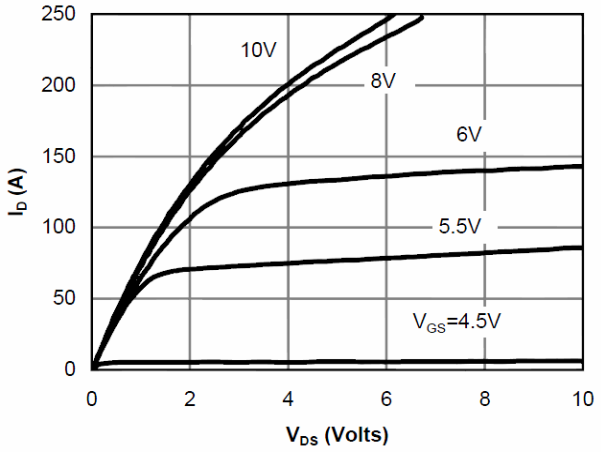


Figure4. Transfer characteristics

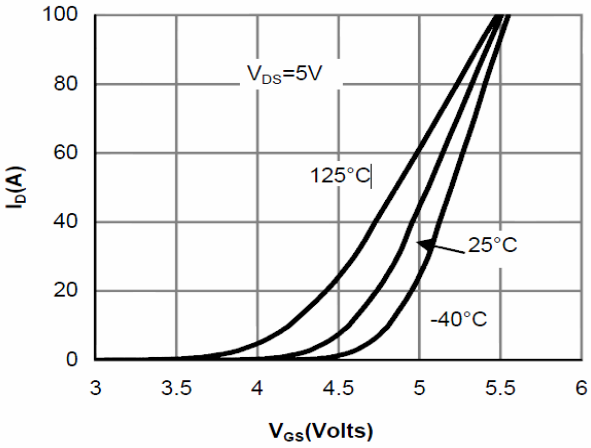


Figure5. Static drain-source on resistance

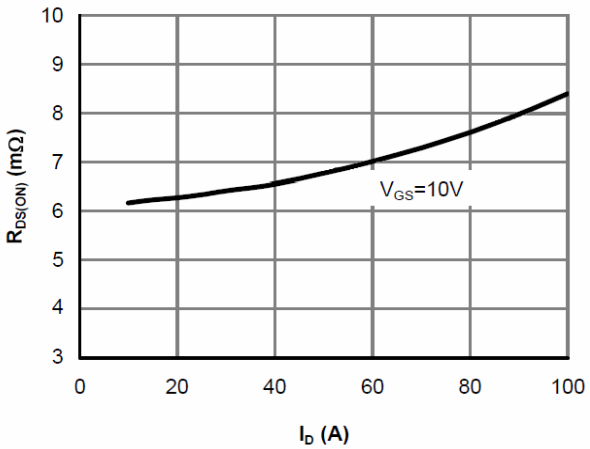


Figure6. $R_{DS(ON)}$ vs Junction Temperature

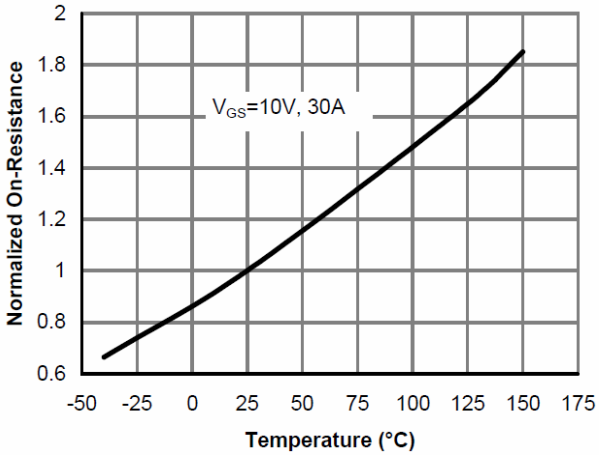


Figure7. BV_{DSS} vs Junction Temperature

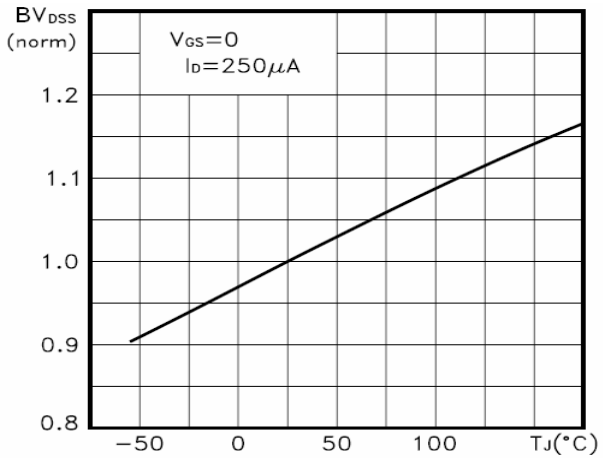


Figure8. $V_{GS(th)}$ vs Junction Temperature

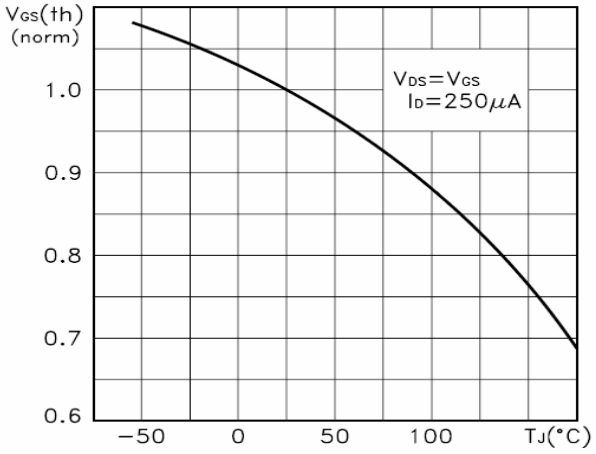


Figure9. Gate charge waveforms

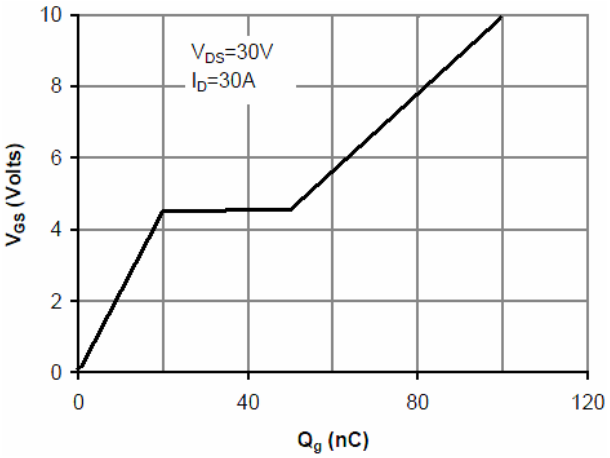


Figure10. Capacitance