Description

The VSM58P02 uses advanced trench technology and design to provide excellent $R_{DS(on)}$ with low gate charge. It can be used in a wide variety of applications.

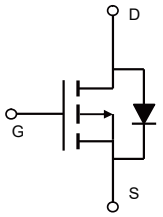
General Features

- V_{DS} = -20V,I_D =-58A
  $R_{DS(on)}$ < 5.6mΩ @ V_{GS}=-4.5V
  $R_{DS(on)}$ < 8.2mΩ @ V_{GS}=-2.5V
- High density cell design for ultra low $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Load switch
- Battery protection

DFN3x3



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM58P02	VSM58P02-D33	DFN3x3	Ø330mm	12mm	5000units

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	±12	V
Drain Current-Continuous	I_D	-58	A
Drain Current-Continuous(100℃)	I_D (100℃)	-43	A
Pulsed Drain Current (T_C=25℃)	I_{DM}	-232	A
Maximum Power Dissipation	P_D	37	W
Derating factor		0.296	W/℃
Single pulse avalanche energy(Note 1)	E_{AS}	164	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case	$R_{\theta JC}$	3.38	℃/W

Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	60	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

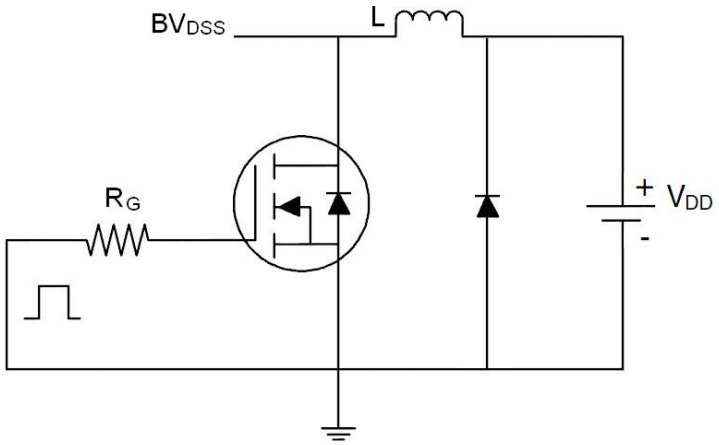
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-20	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-20V,V_{GS}=0V	-	-	-1	uA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±12V,V_{DS}=0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-0.4	-0.65	-1	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-4.5V, I_D=-20A	-	4.5	5.6	mΩ
		V_{GS}=-2.5V, I_D=-20A	-	6.1	8.2	
Forward Transconductance	g_{FS}	V_{DS}=-10V,I_D=-50A	-	7	-	S
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=-10V,V_{GS}=0V, F=1.0MHz	-	4307.4	-	pF
Output Capacitance	C_{oss}		-	594.7	-	pF
Reverse Transfer Capacitance	C_{rss}		-	549.1	-	pF
Switching Characteristics (Note 3)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-10V,R_L=0.5Ω, V_{GS}=-4.5V,R_{GEN}=3Ω	-	13	-	nS
Turn-on Rise Time	t_r		-	59	-	nS
Turn-off Delay Time	$t_{d(off)}$		-	230	-	nS
Turn-off Fall Time	t_f		-	150	-	nS
Total Gate Charge	Q_g	V_{DS}=-10V,I_D=-20A, V_{GS}=-4.5V	-	58.6	-	nC
Gate-Source Charge	Q_{gs}		-	5.8	-	nC
Gate-Drain Charge	Q_{gd}		-	15.7	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=-20A	-	-	-1.2	V
Diode Forward Current	I_S		-	-	-58	A
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F = 20A di/dt = -100A/μs	-	150	-	nS
Reverse Recovery Charge	Qrr		-	220	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

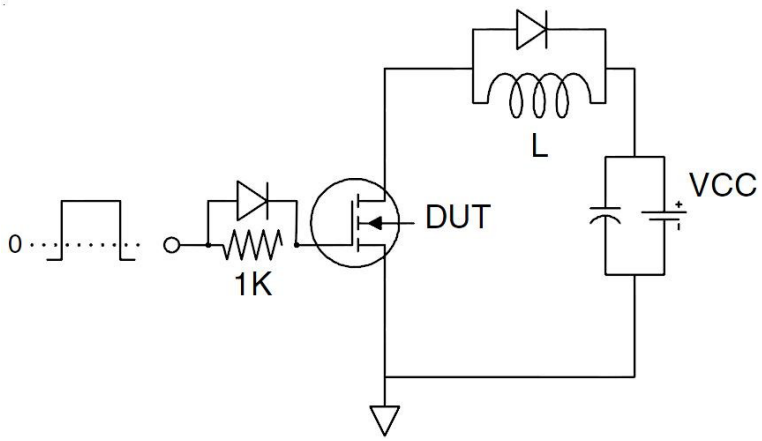
1. EAS condition : Tj=25℃,V_{DD}=-10V,V_G=-10V,L=0.5mH,Rg=25Ω.
2. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it.
3. Guaranteed by design, not subject to production.
4. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

Test Circuit

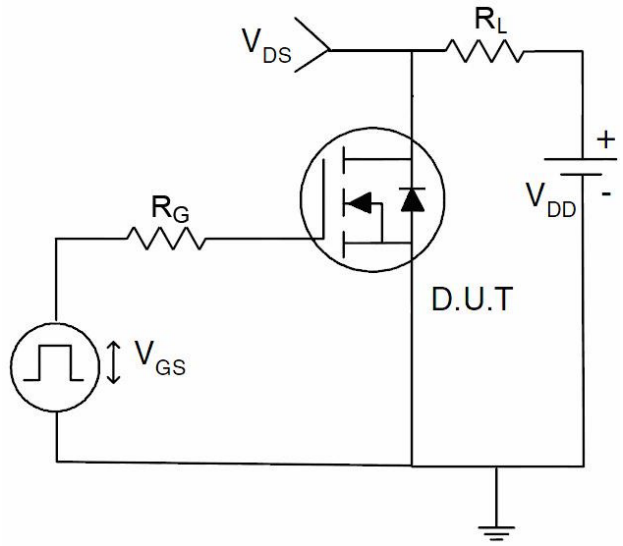
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

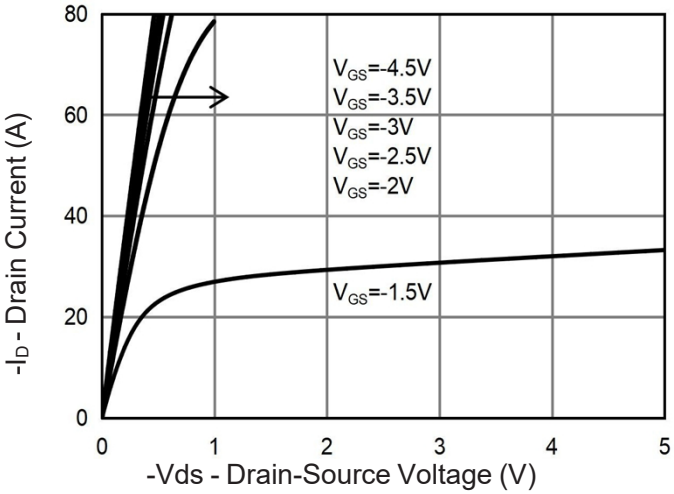


Figure 1 Output Characteristics

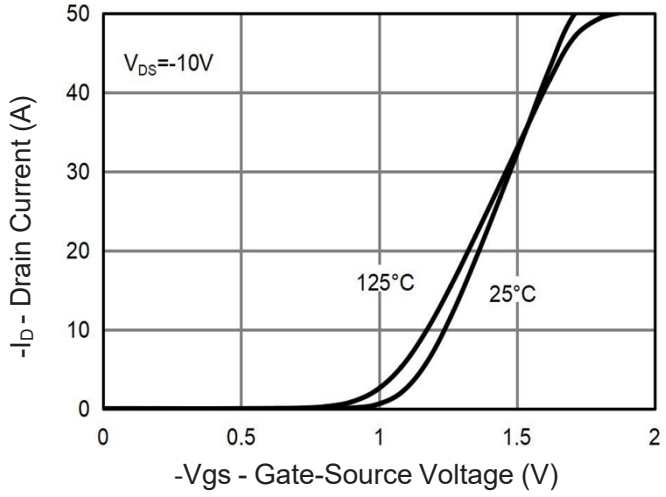


Figure 2 Transfer Characteristics

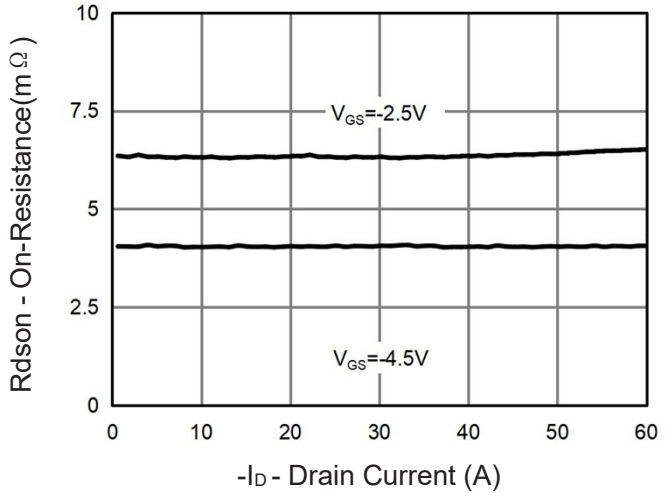


Figure 3 Rdson vs Drain Current

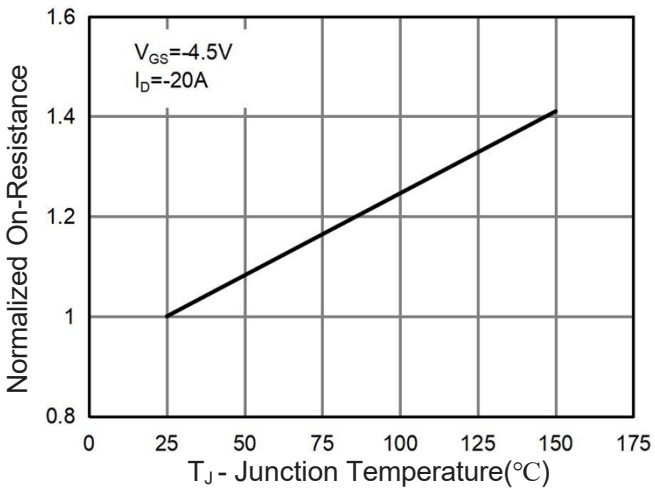


Figure 4 Rdson vs Junction Temperature

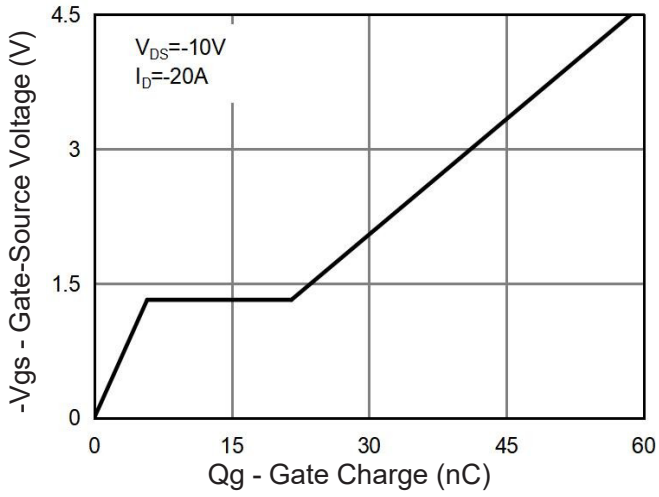


Figure 5 Gate Charge

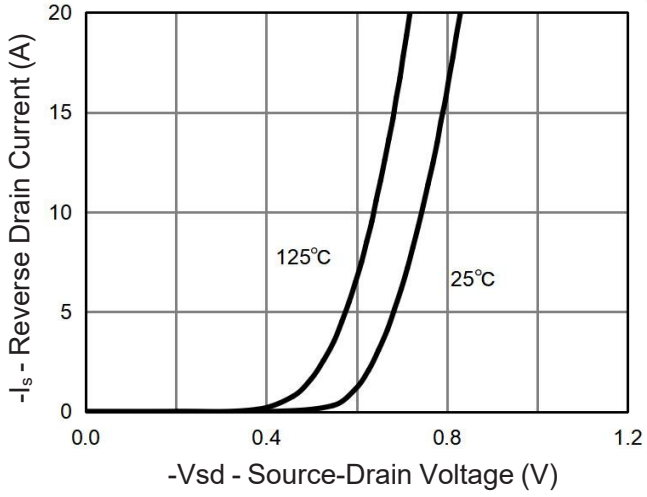


Figure 6 Source- Drain Diode Forward

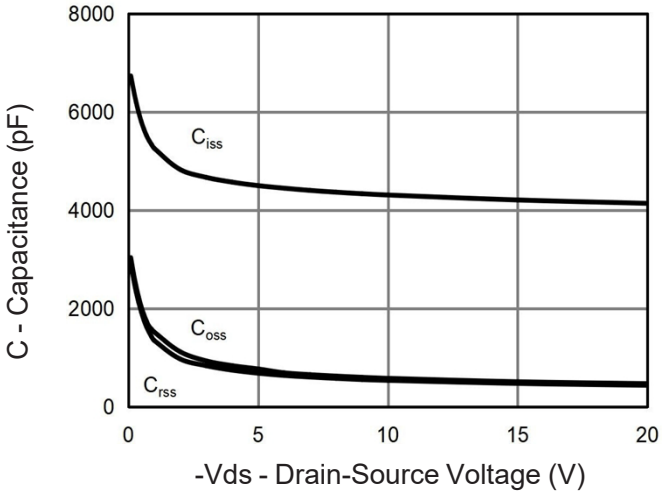


Figure 7 Capacitance vs Vds

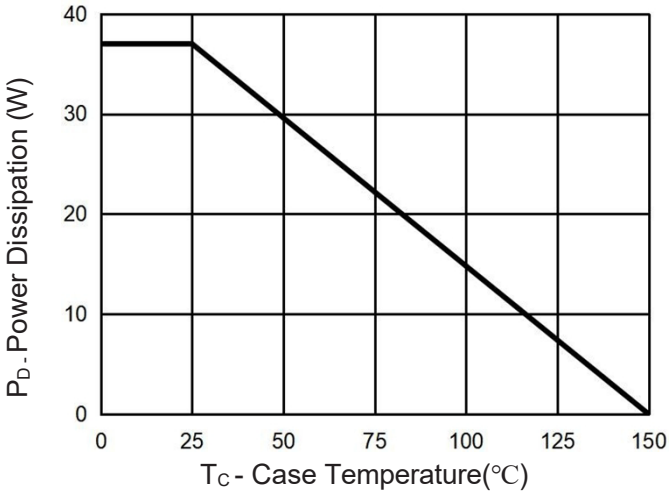


Figure 9 Power De-rating

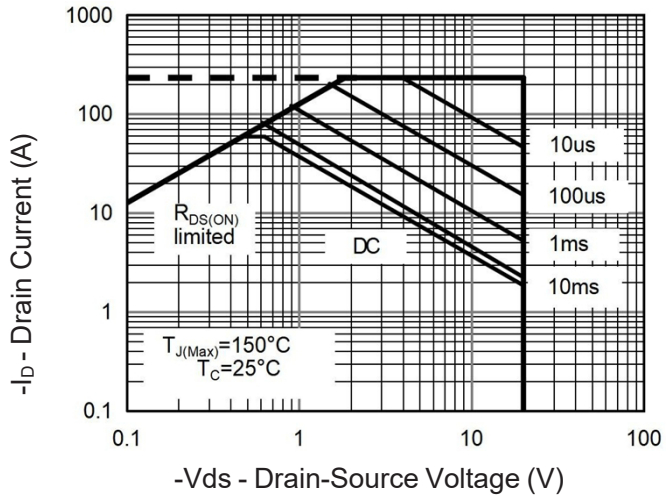


Figure 8 Safe Operation Area(Note 4)

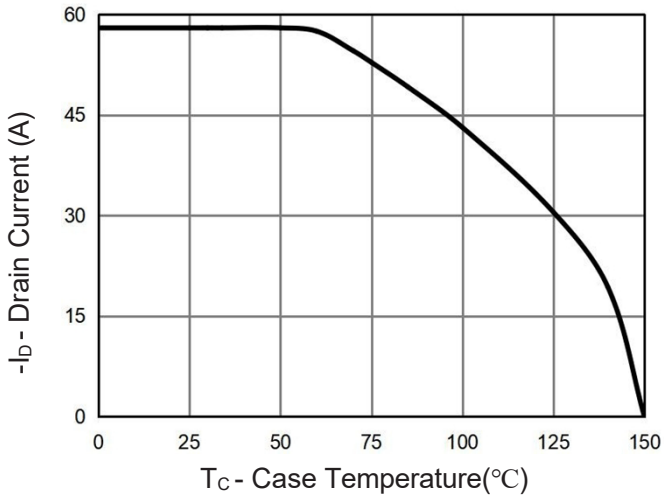


Figure10 Drain Current De-rating

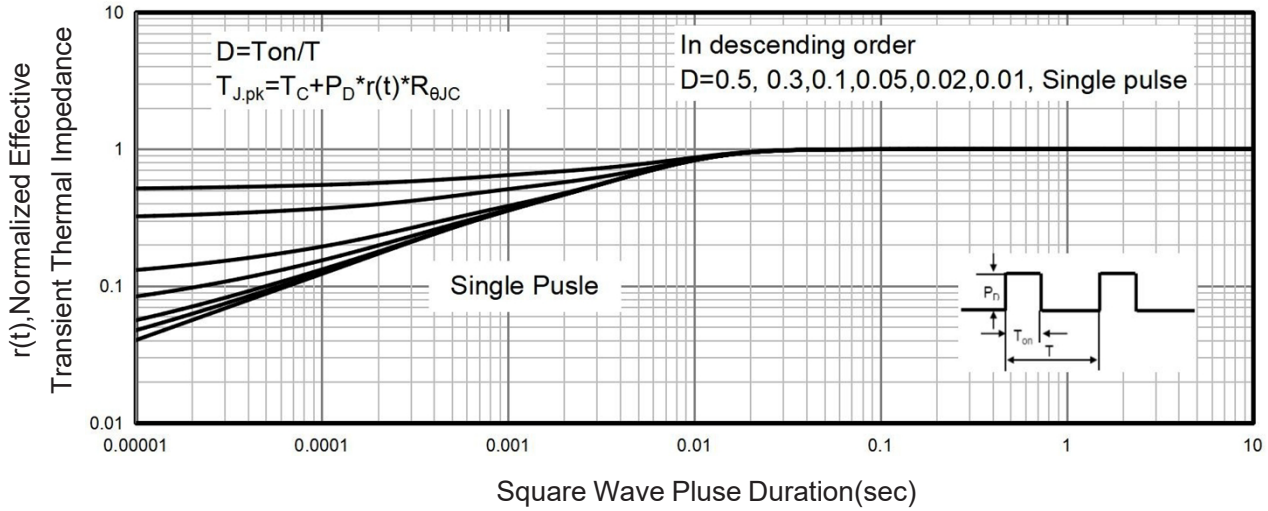


Figure 11 Normalized Maximum Transient Thermal Impedance