Description

The VSM200P02 uses advanced trench technology and design to provide excellent RDS(ON) with low gate charge. It can be used in a wide variety of applications.

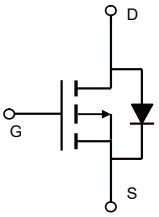
General Features

- V_{DS} = -20 V,I_D = -200 A
  $R_{DS(ON)}$ < 1.5 mΩ @ V_{GS}=-4.5V
  $R_{DS(ON)}$ < 2 mΩ @ V_{GS}=-2.5V
- High density cell design for ultra low $R_{ds(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Power switching applications
- Hard switched and high frequency circuits
- Uninterruptible power supply

DFN5x6



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM200P02	VSM200P02-D56	DFN5x6	Ø330mm	12mm	5000units

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	±12	V
Drain Current-Continuous	I_D	-200	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	-145	A
Pulsed Drain Current	I_{DM}	-800	A
Maximum Power Dissipation	P_D	113	W
Derating factor		0.909	W/℃
Single pulse avalanche energy (Note 1)	E_{AS}	256	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case	$R_{\theta JC}$	1.1	℃/W
Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	50	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

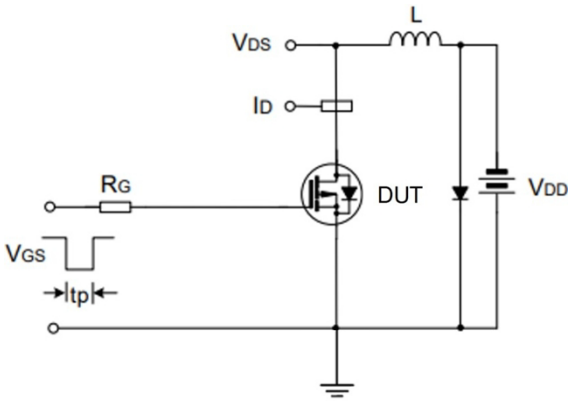
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-20	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-20V,V_{GS}=0V	-	-	-1	uA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±12V,V_{DS}=0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-0.3	-0.65	-1	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-4.5V, I_D=-20A	-	1.1	1.5	mΩ
		V_{GS}=-2.5V, I_D=-20A	-	1.5	2	
Forward Transconductance	g_{FS}	V_{DS}=-5V,I_D=-24A	-	80	-	S
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=-10V,V_{GS}=0V, F=1.0MHz	-	14582	-	pF
Output Capacitance	C_{oss}		-	1704	-	pF
Reverse Transfer Capacitance	C_{rss}		-	1434	-	pF
Switching Characteristics (Note 3)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-10V,I_D=-20A, V_{GS}=-4.5V,R_{GEN}=3Ω	-	15	-	nS
Turn-on Rise Time	t_r		-	123	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	200	-	nS
Turn-Off Fall Time	t_f		-	60	-	nS
Total Gate Charge	Q_g	V_{DS}=-10V,I_D=-20A, V_{GS}=-4.5V	-	174	-	nC
Gate-Source Charge	Q_{gs}		-	20	-	nC
Gate-Drain Charge	Q_{gd}		-	38	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=-20A	-	-	-1.2	V
Diode Forward Current	I_S		-	-	-200	A
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F =-20A di/dt =-100A/μs	-	66	-	nS
Reverse Recovery Charge	Qrr		-	100	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

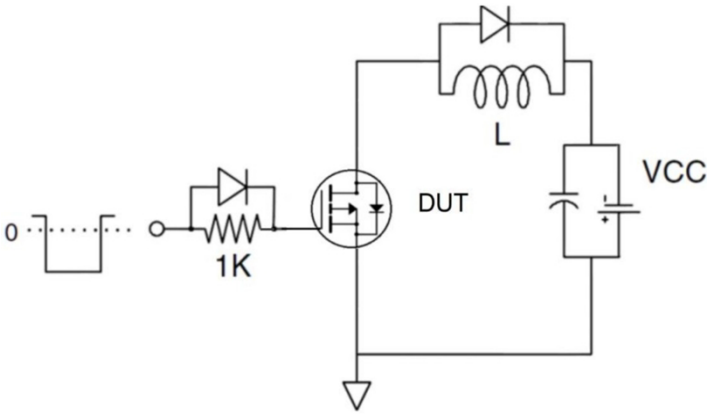
1. EAS condition : Tj=25℃,V_{DD}=-20V,V_G=-10V,L=0.5mH,Rg=25Ω.
2. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it.
3. Guaranteed by design, not subject to production.
4. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

Test Circuit

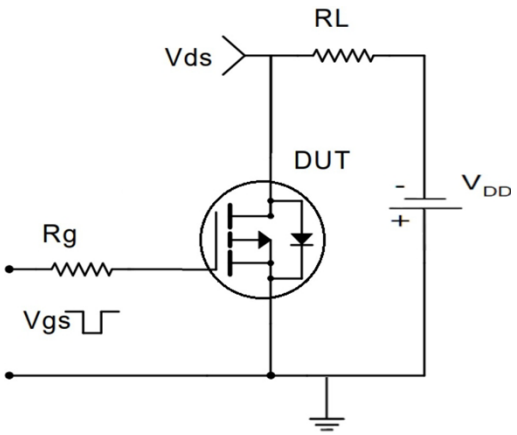
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

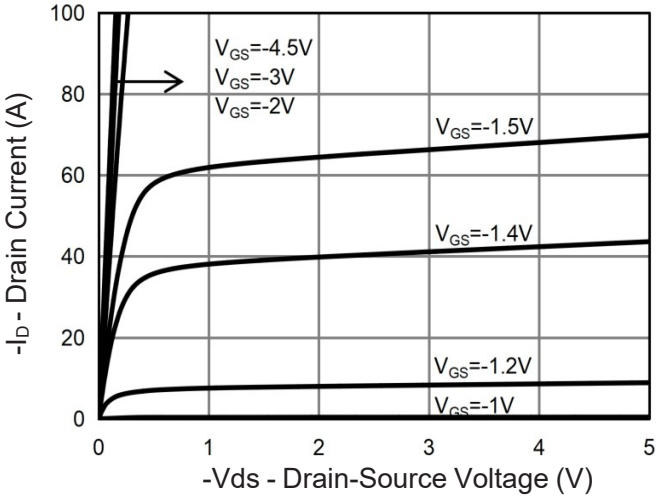


Figure 1 Output Characteristics

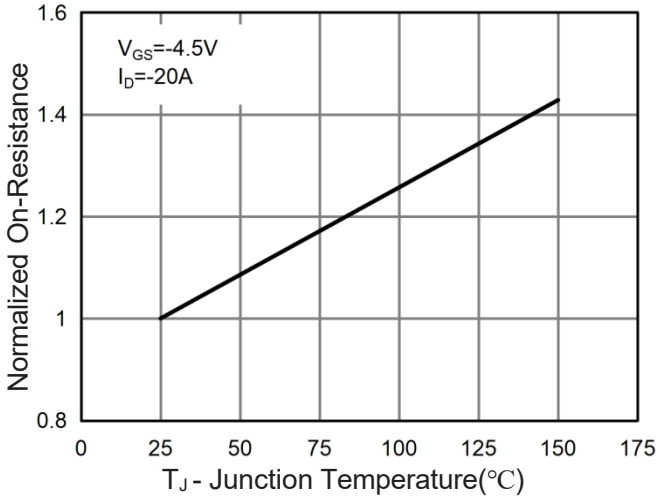


Figure 4 Rdson vs Junction Temperature

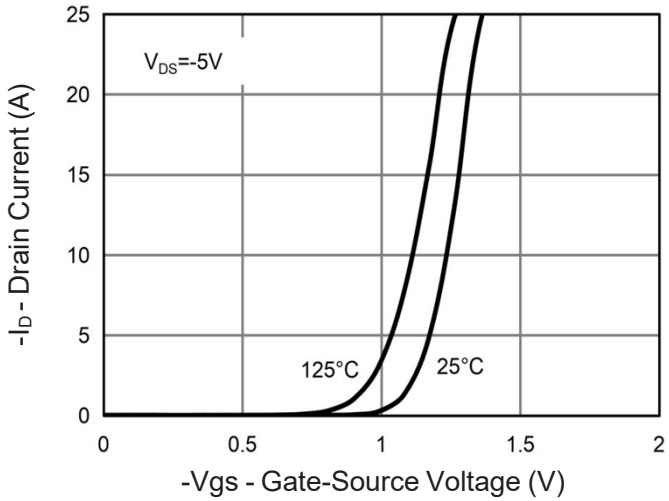


Figure 2 Transfer Characteristics

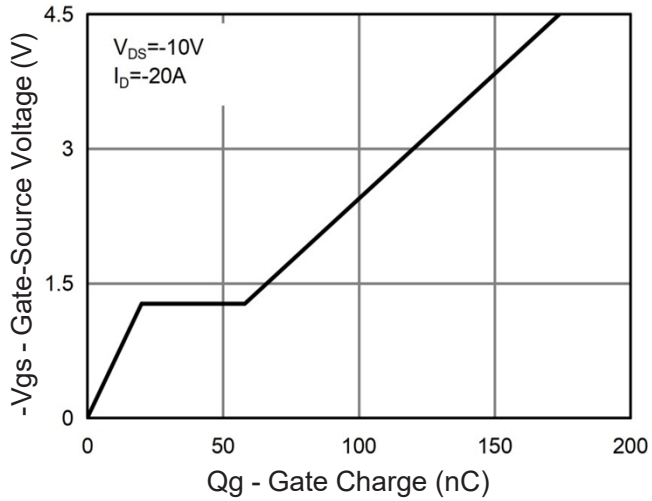


Figure 5 Gate Charge

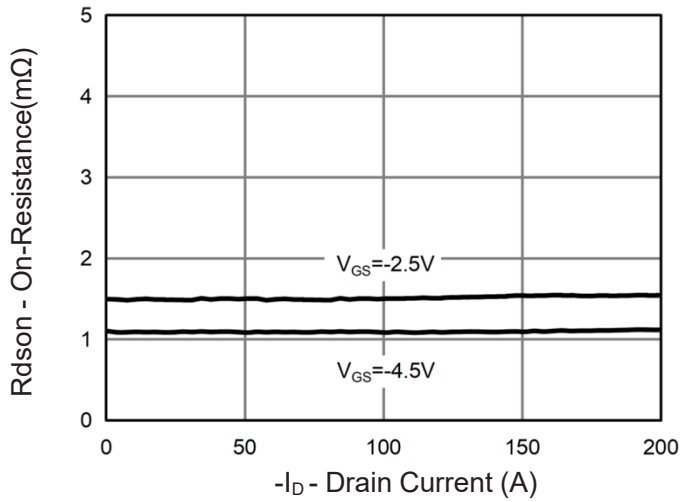


Figure 3 Rdson vs Drain Current

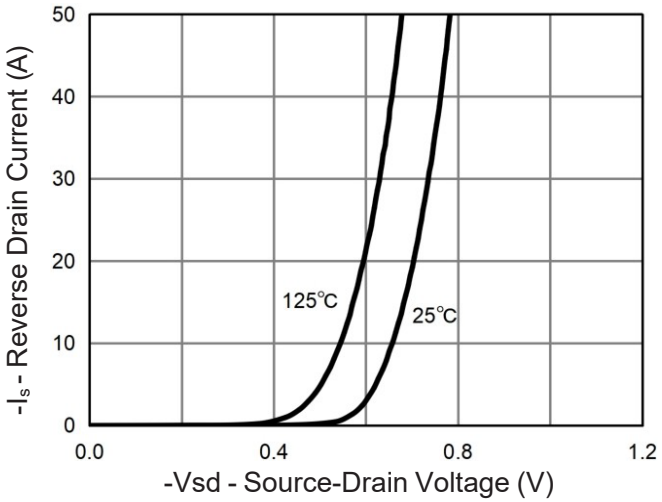


Figure 6 Source-Drain Diode Forward

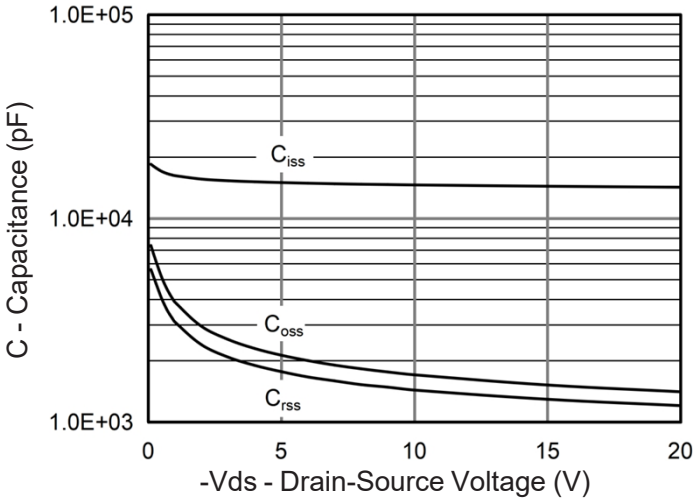


Figure 7 Capacitance vs Vds

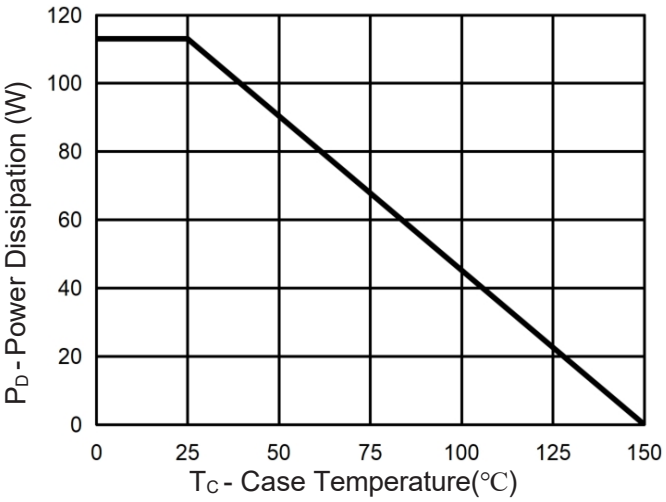


Figure 9 Power De-rating

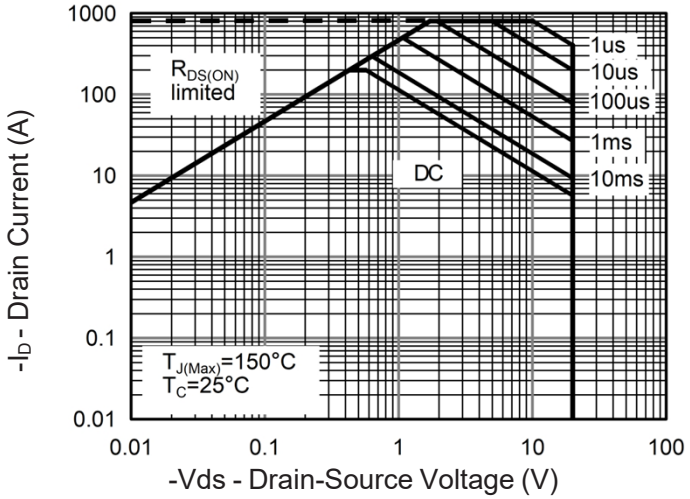


Figure 8 Safe Operation Area (Note 4)

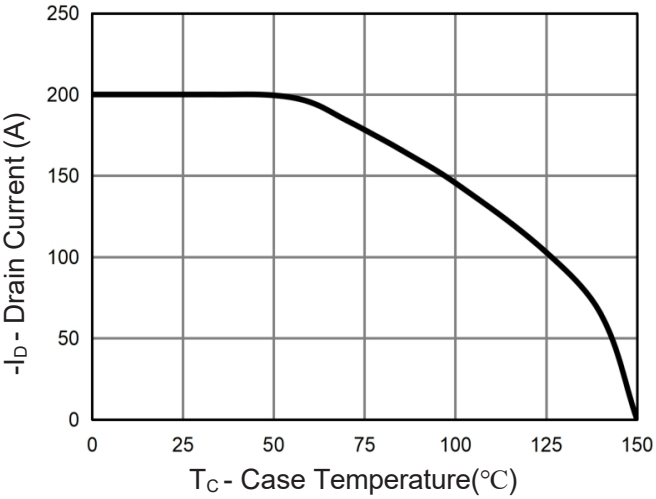


Figure10 Drain Current De-rating

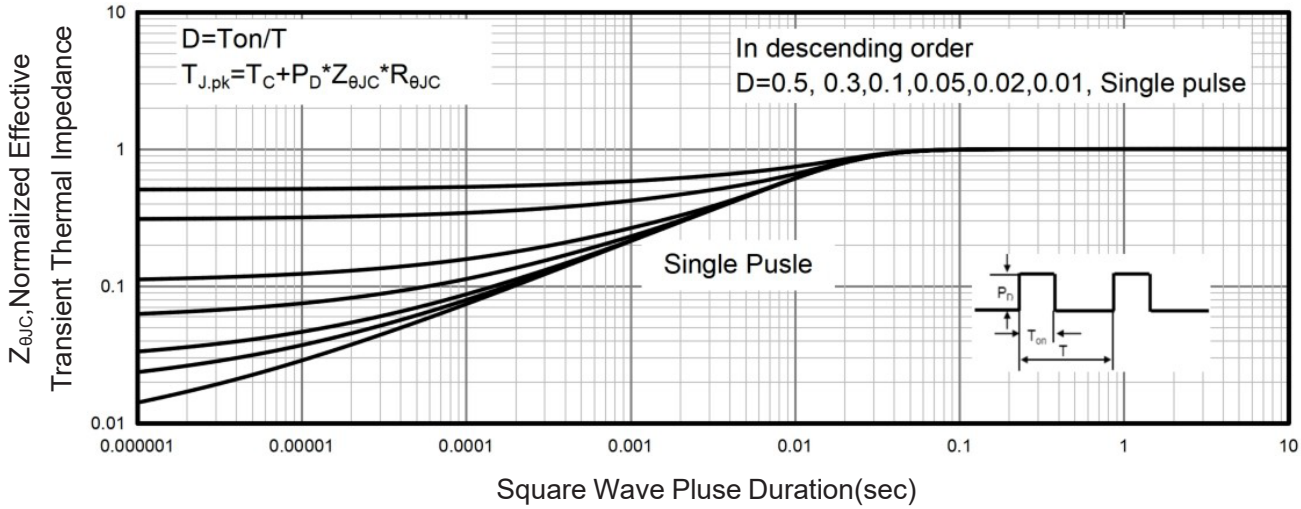


Figure 11 Normalized Maximum Transient Thermal Impedance