Description

The VSM60P03 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

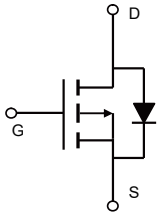
General Features

- V_{DS} =-30V,I_D =-60A
  $R_{DS(ON)}$ < 4.1mΩ @ V_{GS}=-10V
  $R_{DS(ON)}$ < 7.0mΩ @ V_{GS}=-4.5V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Battery and loading switching

DFN5x6



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM60P03	VSM60P03-D56	DFN5x6	Ø330mm	12mm	5000 units

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	-60	A
Pulsed Drain Current	I_{DM}	-240	A
Maximum Power Dissipation	P_D	100	W
Derating factor		0. 8	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	980	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case(Note 2)	$R_{\theta JC}$	1.25	℃/W

Electrical Characteristics (TC=25℃unless otherwise noted)

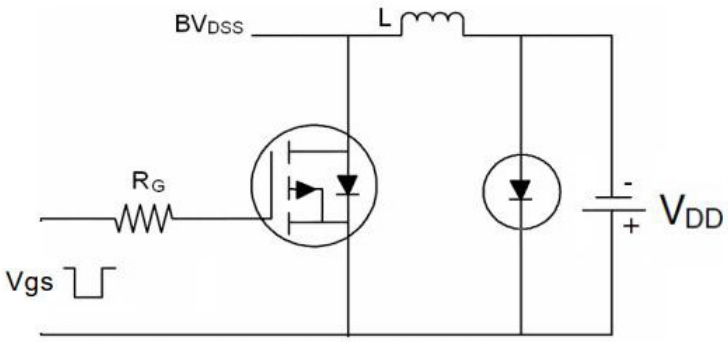
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-30	-33	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-1.1	-1.6	-2.1	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-30A	-	3.2	4.1	mΩ
		V_{GS}=-4.5V, I_D=-30A	-	4.5	7.0	mΩ
Forward Transconductance	g_{FS}	V_{DS}=-5V,I_D=-30A	-	20	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=-15V,V_{GS}=0V, F=1.0MHz	-	8469	-	pF
Output Capacitance	C_{oss}		-	1157	-	pF
Reverse Transfer Capacitance	C_{rss}		-	988	-	pF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-15V,I_D=-30A V_{GS}=-10V,R_{GEN}=6Ω	-	20	-	nS
Turn-on Rise Time	t_r		-	18	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	95	-	nS
Turn-Off Fall Time	t_f		-	30	-	nS
Total Gate Charge	Q_g	V_{DS}=-15V,I_D=-30A, V_{GS}=-10V	-	118.7	-	nC
Gate-Source Charge	Q_{gs}		-	16.1	-	nC
Gate-Drain Charge	Q_{gd}		-	30.7	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=-30A	-	-0.85	-1.2	V
Diode Forward Current (Note 2)	I_S		-	-	-60	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF = -30A di/dt = 100A/μs (Note3)	-	-	47	nS
Reverse Recovery Charge	Qrr		-	-	78	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

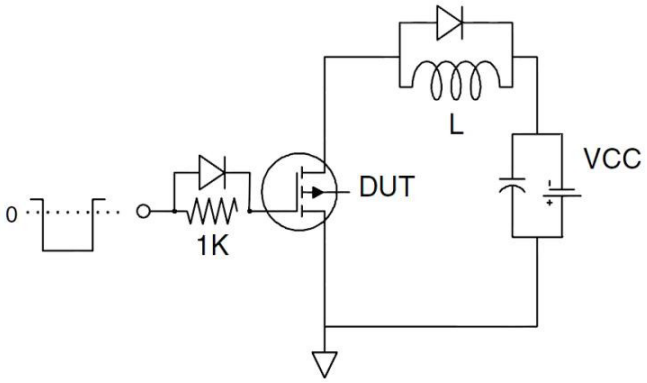
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition：Tj=25℃,V_{DD}=-15V,V_G=-10V,L=0.5mH,Rg=25Ω

Test Circuit

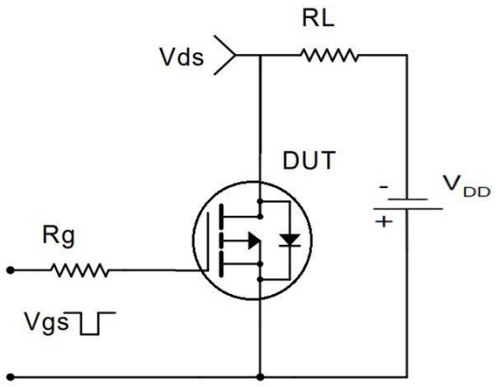
1) E_{AS} Test Circuit



2） Gate charge test Circuit



3） Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

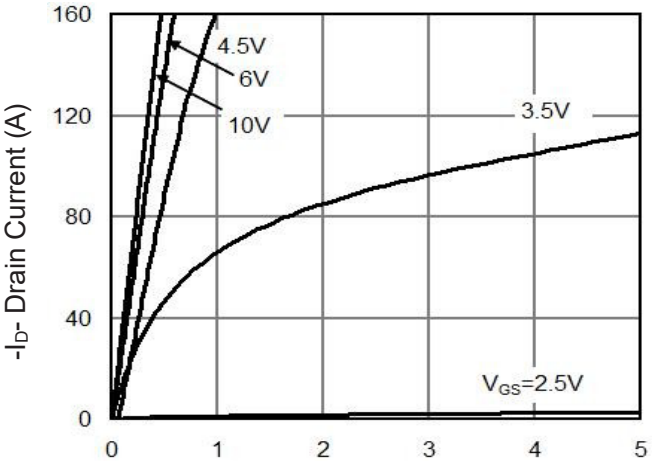


Figure 1 Output Characteristics

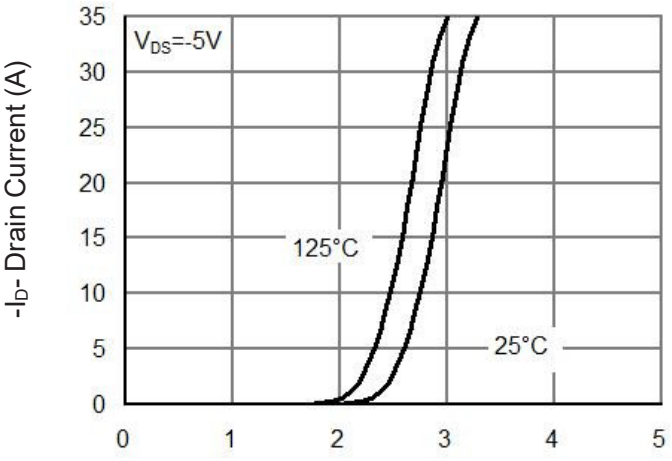


Figure 2 Transfer Characteristics

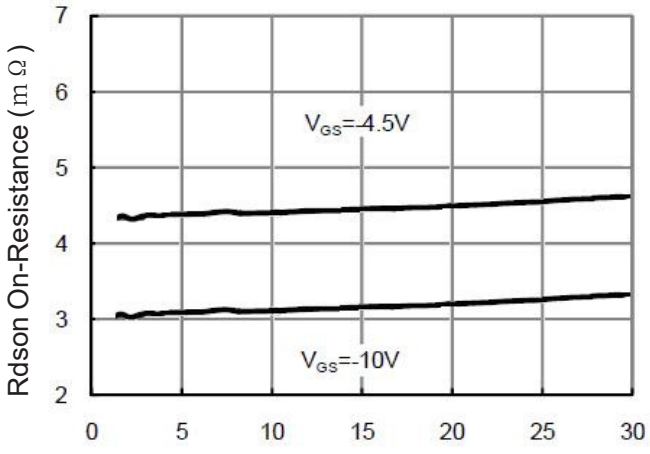


Figure 3 Rdson- Drain Current

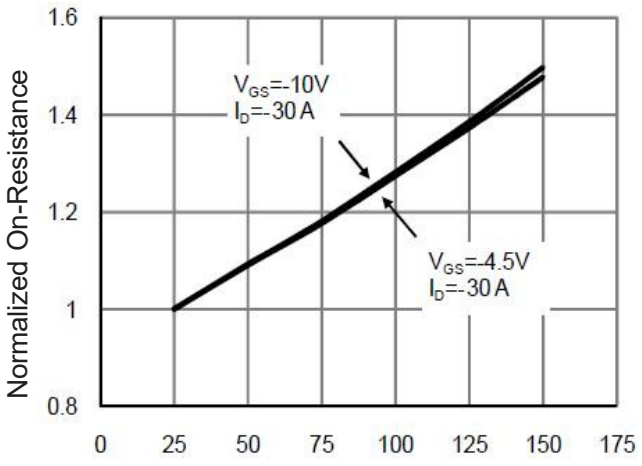


Figure 4 Rdson-Junction Temperature

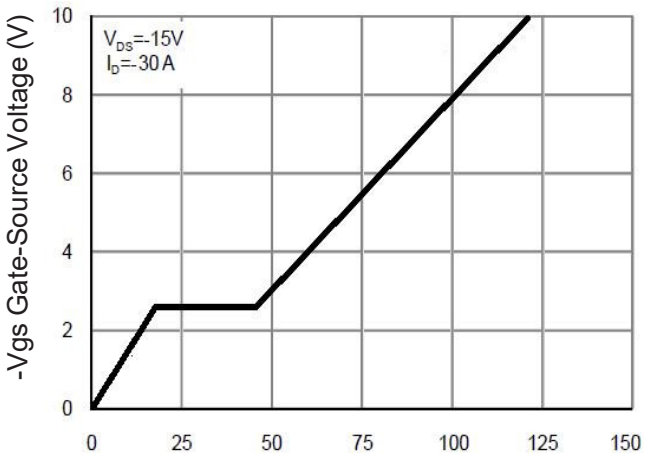


Figure 5 Gate Charge

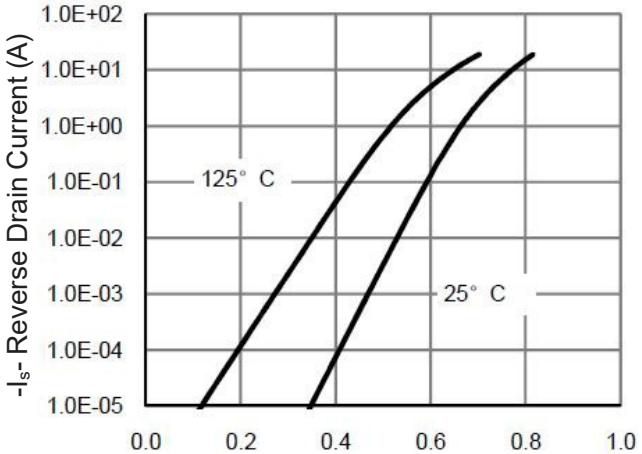


Figure 6 Source- Drain Diode Forward

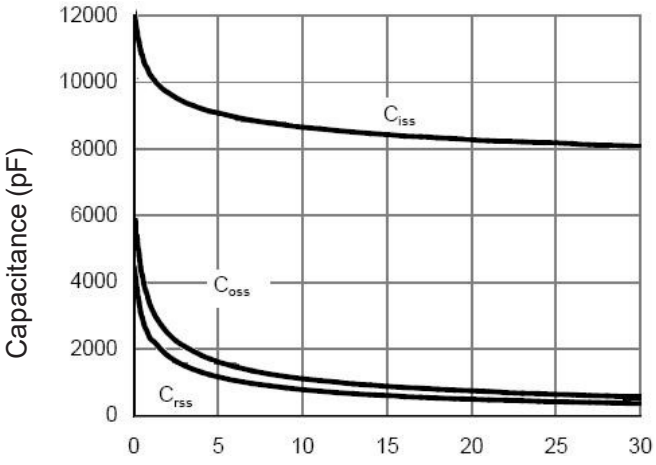


Figure 7 Capacitance vs Vds

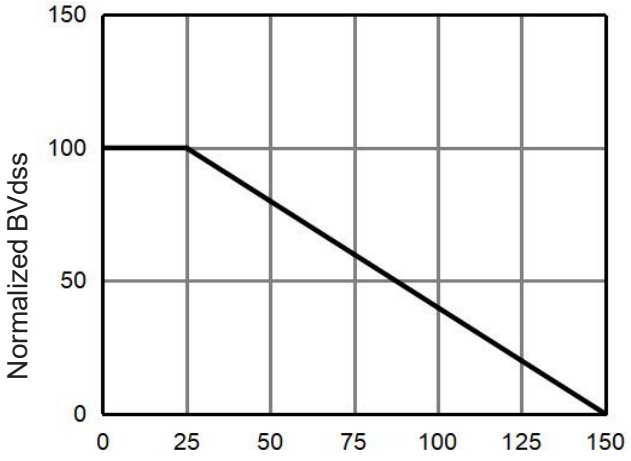


Figure 9 BV_{DSS} vs Junction Temperature

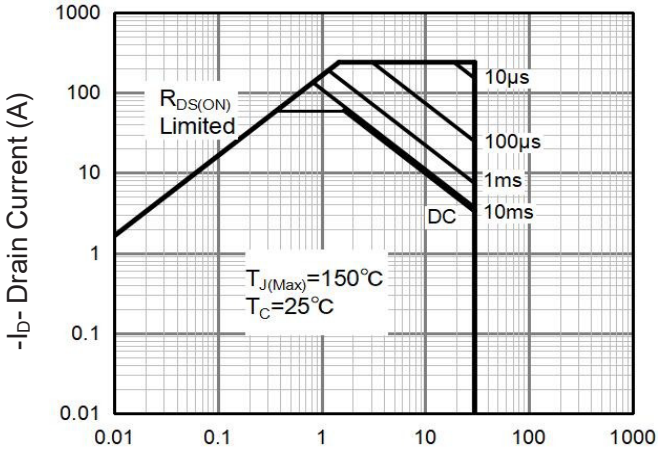


Figure 8 Safe Operation Area

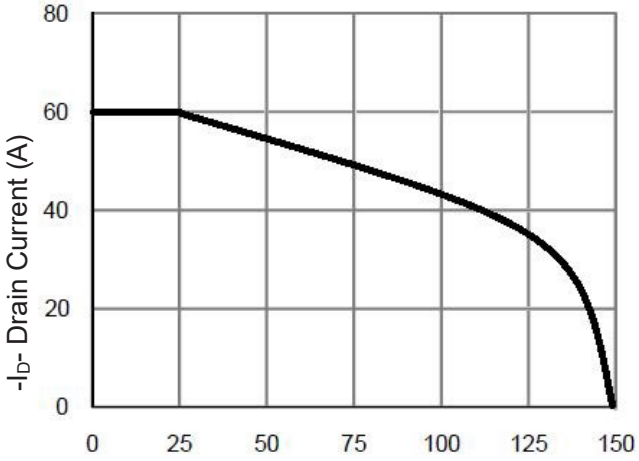


Figure 10 ID Current Derating vs Junction Temperature

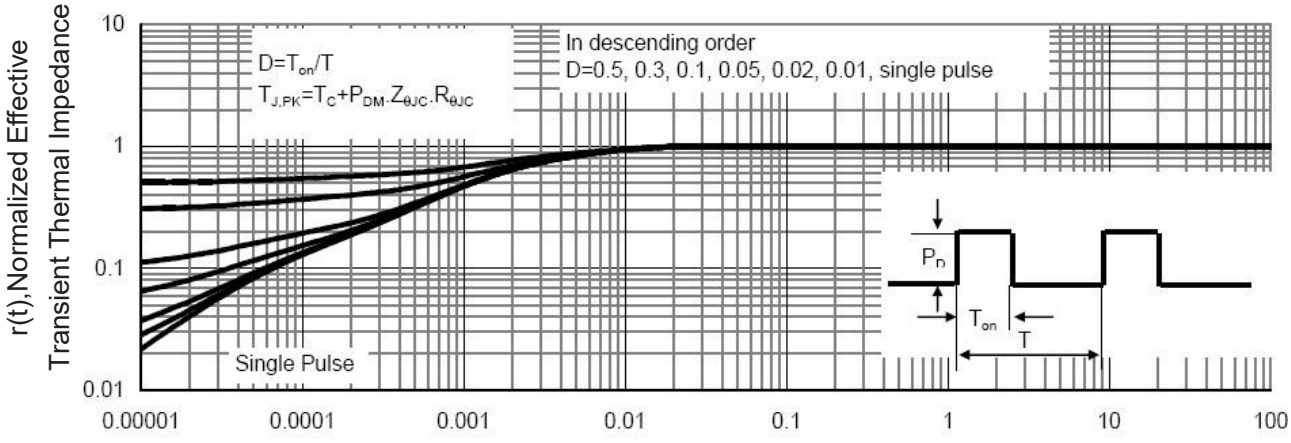


Figure 11 Normalized Maximum Transient Thermal Impedance