Description

The VSM70P06 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge .This device is well suited for high current load applications.

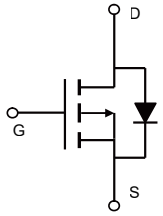
Application

- High side switch for full bridge converter
- DC/DC converter for LCD display

General Features

- V_{DS} =-60V,I_D =-70A
  $R_{DS(ON)}$=11mΩ (typical) @ V_{GS}=-10V
  $R_{DS(ON)}$=13mΩ (typical) @ V_{GS}=-4.5V
- High density cell design for ultra low Rdson
- Very low on-resistance $R_{DS(on)}$
- Good stability and uniformity with high E_{AS}
- 150 °C operating temperature
- Pb-free lead plating

DFN5x6



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM70P06	VSM70P06-D56	DFN5x6	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	-70	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	-49	A
Pulsed Drain Current(Note 1)	I_{DM}	-280	A
Maximum Power Dissipation	P_D	110	W
Derating factor		0.88	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	560	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.14	℃/W
Thermal Resistance,Junction-to-Ambient(Note 2)	$R_{\theta JA}$	50	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-60V,V_{GS}=0V	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-1.2	-1.8	-2.4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-20A	-	11	13	mΩ
		V_{GS}=-4.5V, I_D=-20A	-	13	16	mΩ
Forward Transconductance	g_{FS}	V_{DS}=-5V,I_D=-20A	-	25	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=-30V,V_{GS}=0V, F=1.0MHz	-	5604	-	PF
Output Capacitance	C_{oss}		-	356	-	PF
Reverse Transfer Capacitance	C_{rss}		-	265	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-30V, R_L=1.5Ω, V_{GS}=-10V,R_G=3Ω	-	18	-	nS
Turn-on Rise Time	t_r		-	20	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	55	-	nS
Turn-Off Fall Time	t_f		-	35	-	nS
Total Gate Charge	Q_g	V_{DS}=-30,I_D=-20A, V_{GS}=-10V	-	62.1		nC
Gate-Source Charge	Q_{gs}		-	9.3		nC
Gate-Drain Charge	Q_{gd}		-	16.8		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=-20A	-	-	-1.2	V
Diode Forward Current (Note 2)	I_S		-	-	-70	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF =- 20A di/dt = -100A/μs(Note3)	-	49	-	nS
Reverse Recovery Charge	Qrr		-	71	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.

2. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design, and the maximum temperature of150° C may be used if the PCB allows it.

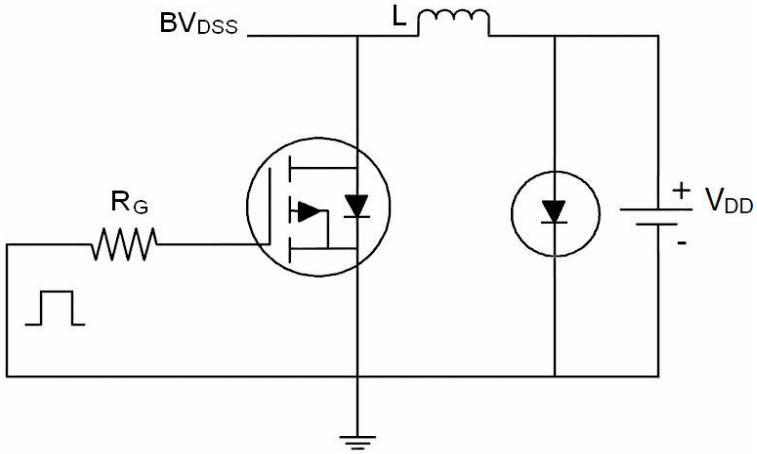
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

4. Guaranteed by design, not subject to production

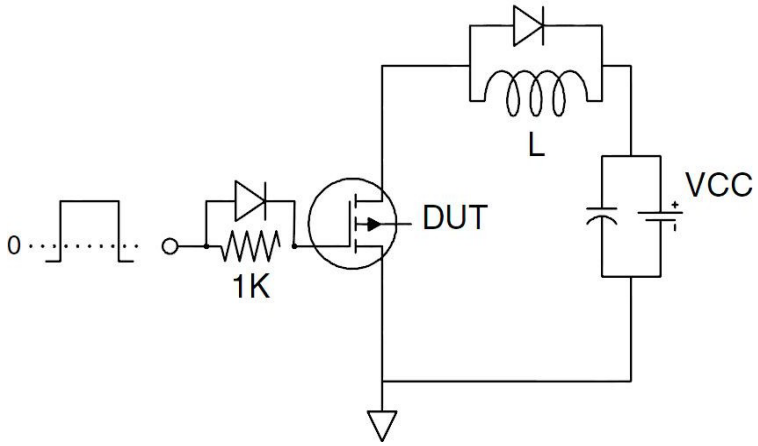
5. E_{AS} condition: Tj=25℃,V_{DD}=-30V,V_G=-10V,L=0.5mH,Rg=25Ω

Test Circuit

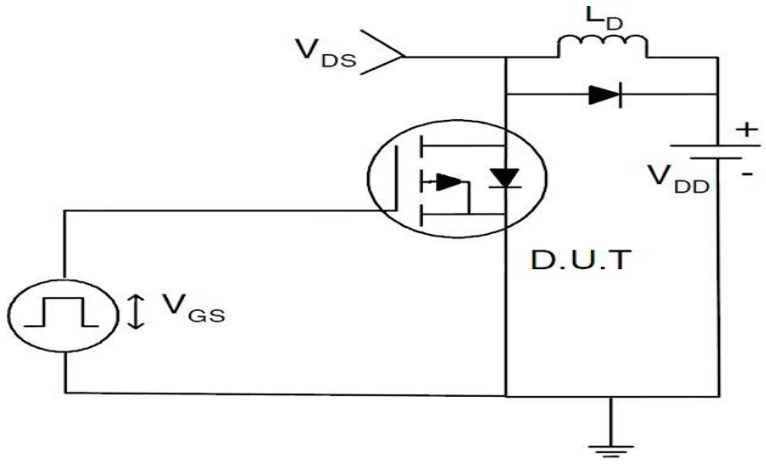
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

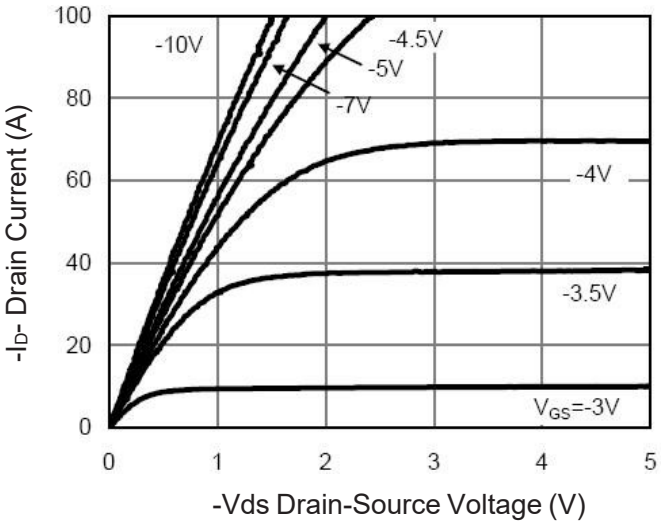


Figure 1 Output Characteristics

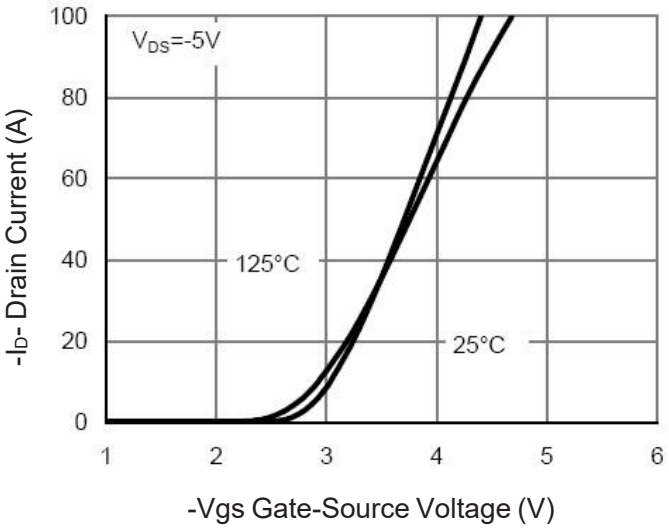


Figure 2 Transfer Characteristics

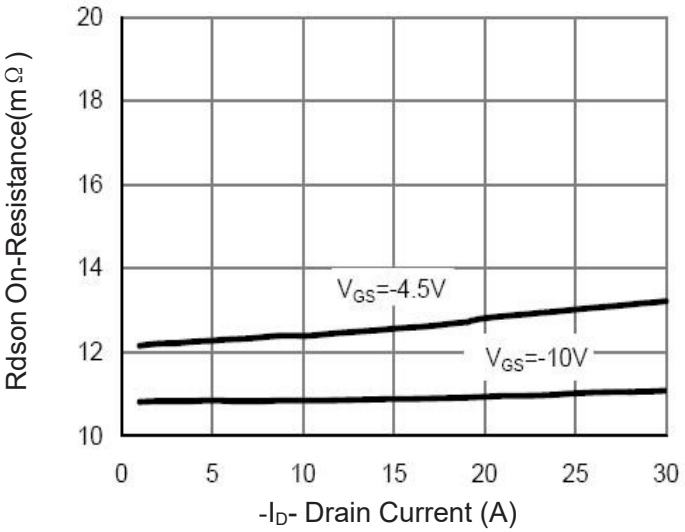


Figure 3 Rdson- Drain Current

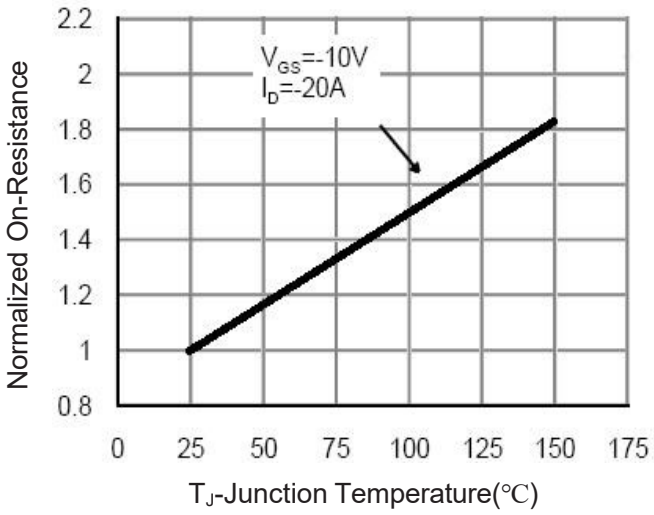


Figure 4 Rdson-Junction Temperature

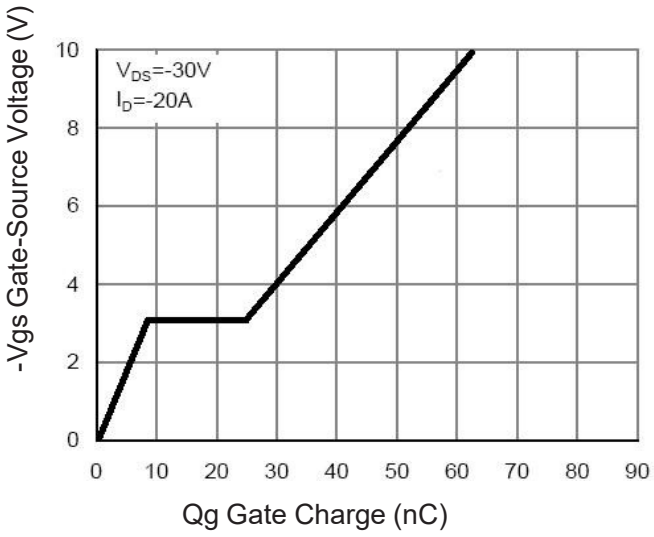


Figure 5 Gate Charge

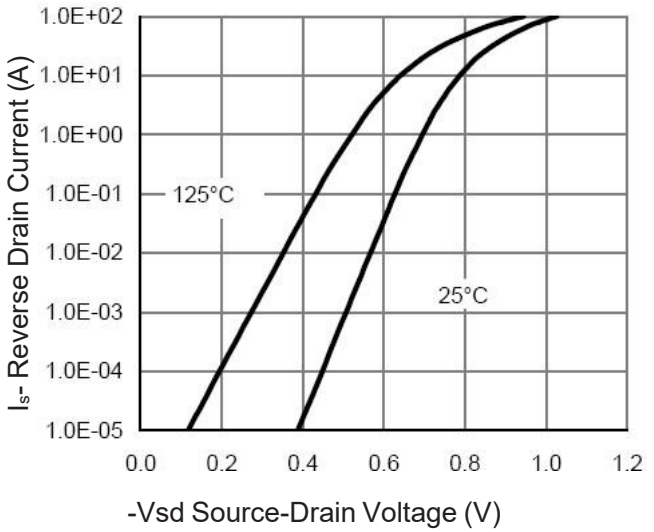


Figure 6 Source- Drain Diode Forward

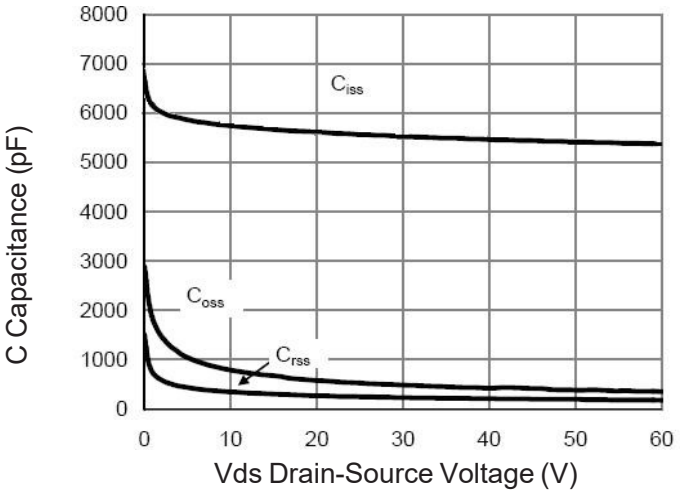


Figure 7 Capacitance vs Vds

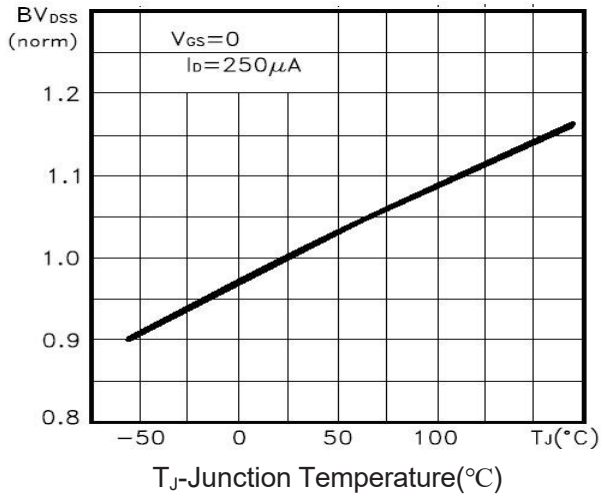


Figure 9 BV_{DSS} vs Junction Temperature

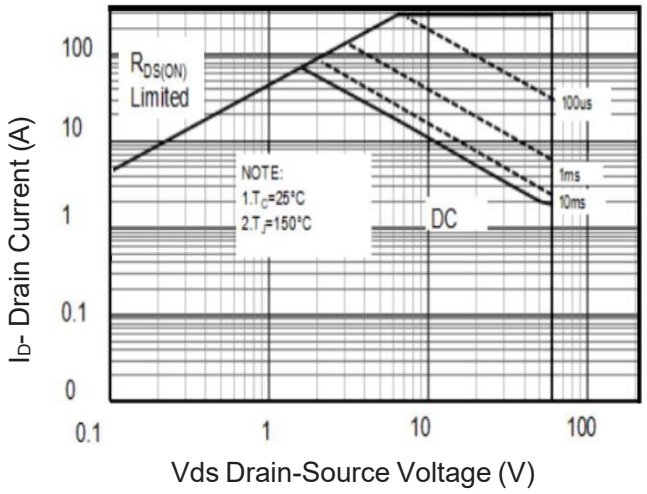


Figure 8 Safe Operation Area

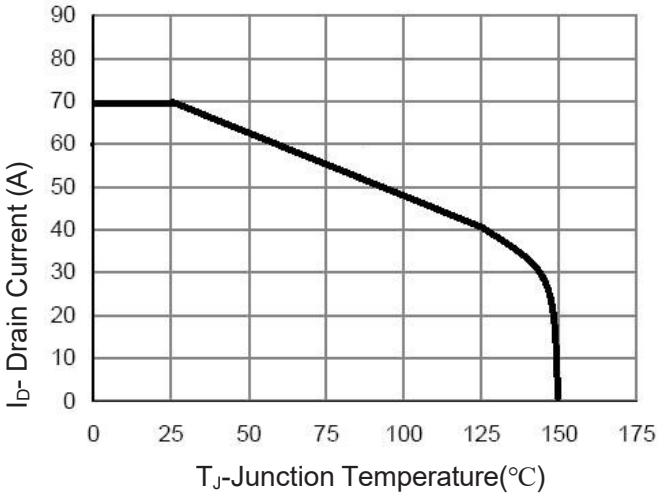


Figure 10 ID Current De-rating

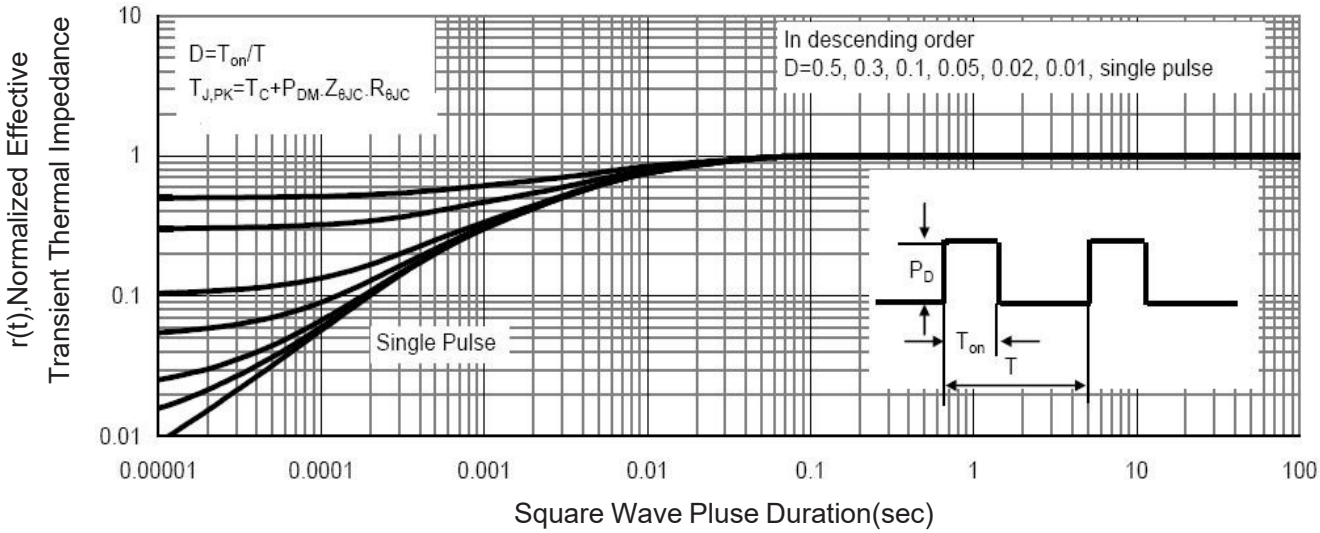


Figure 11 Normalized Maximum Transient Thermal Impedance