Description

The VSM78P40Y uses advanced trench technology and design to provide excellent $R_{DS(on)}$ with low gate charge. It can be used in a wide variety of applications.

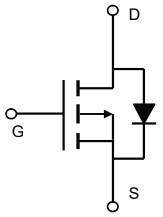
General Features

- V_{DS} = -40V,I_D =-4.3A
  $R_{DS(on)}$ < 78mΩ @ V_{GS}=-10V
  $R_{DS(on)}$ < 113mΩ @ V_{GS}=-4.5V
- High density cell design for ultra low $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

Application

- Power switching applications
- Hard switched and high frequency circuits
- Uninterruptible power supply

SOT-23-3



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM78P40Y	VSM78P40Y-S2-3	SOT-23-3	Ø180mm	8mm	3000 units

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-40	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current-Continuous	T_C=25℃	I_D	-4.8	A
	T_C=75℃		-3.7	A
	T_A=25℃		-4.3	A
	T_A=75℃		-3.3	A
Pulsed Drain Current (T_A=25℃)		I_{DM}	-17.2	A
Maximum Power Dissipation	T_C=25℃	P_D	2.5	W
	T_C=75℃		1.5	W
	T_A=25℃		2	W
	T_A=75℃		1.2	W
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case	$R_{\theta JC}$	50	℃/W
Thermal Resistance,Junction-to-Ambient (Note 1)	$R_{\theta JA}$	62.5	℃/W

Electrical Characteristics (T_A=25℃unless otherwise noted)

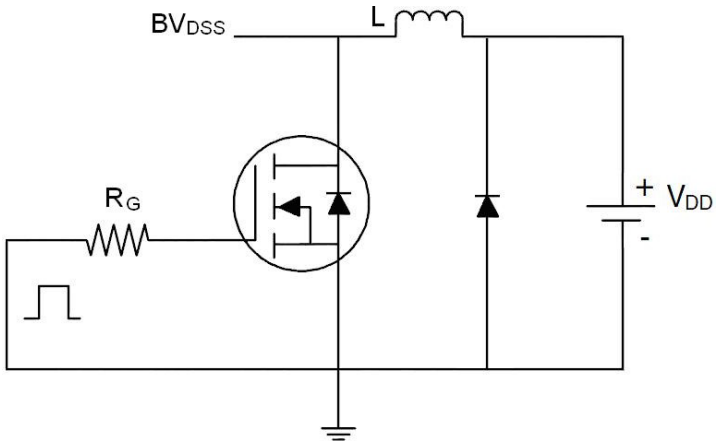
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-40V,V_{GS}=0V	-	-	-1	uA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-1.5	-1.8	-2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-5A	-	68	78	mΩ
		V_{GS}=-4.5V, I_D=-4A	-	87	113	
Forward Transconductance	g_{FS}	V_{DS}=-10V,I_D=-4.3A	-	11	-	S
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=-20V,V_{GS}=0V, F=1.0MHz	-	527.2	-	pF
Output Capacitance	C_{oss}		-	47	-	pF
Reverse Transfer Capacitance	C_{rss}		-	45.3	-	pF
Switching Characteristics (Note 2)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-20V,R_L=0.5Ω, V_{GS}=-10V,R_{GEN}=3Ω	-	14	-	nS
Turn-on Rise Time	t_r		-	32	-	nS
Turn-off Delay Time	$t_{d(off)}$		-	45	-	nS
Turn-off Fall Time	t_f		-	39	-	nS
Total Gate Charge	Q_g	V_{DS}=-20V,I_D=-5A, V_{GS}=-10V	-	12.4	-	nC
Gate-Source Charge	Q_{gs}		-	2.3	-	nC
Gate-Drain Charge	Q_{gd}		-	2.2	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=-3A	-	-	-1.2	V
Diode Forward Current	I_S		-	-	-4.3	A

Notes:

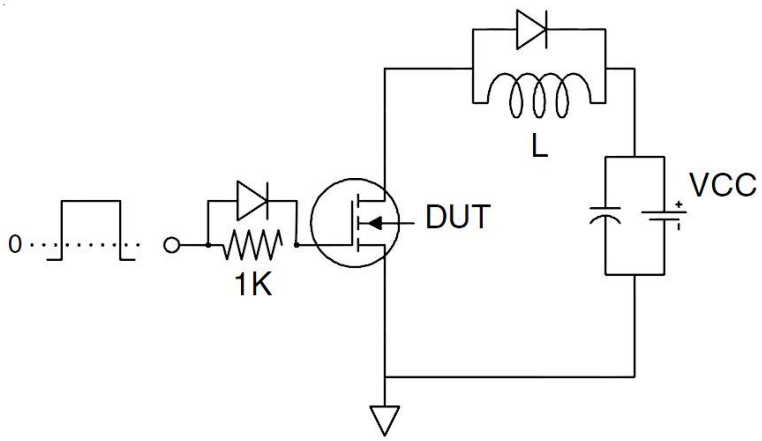
1. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it.
2. Guaranteed by design, not subject to production.
3. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

Test Circuit

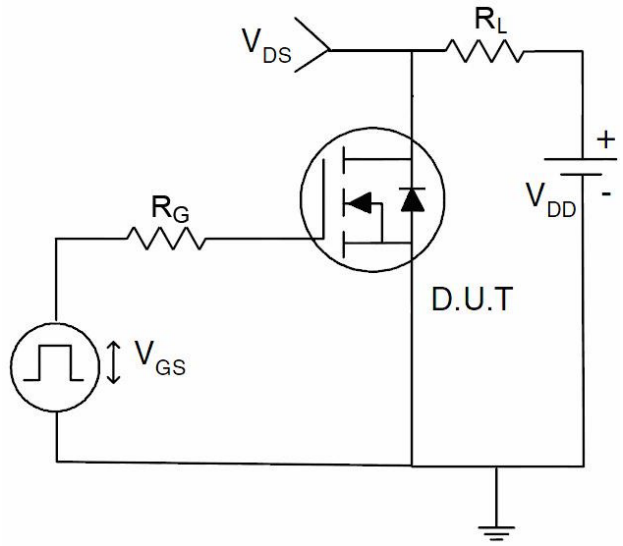
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

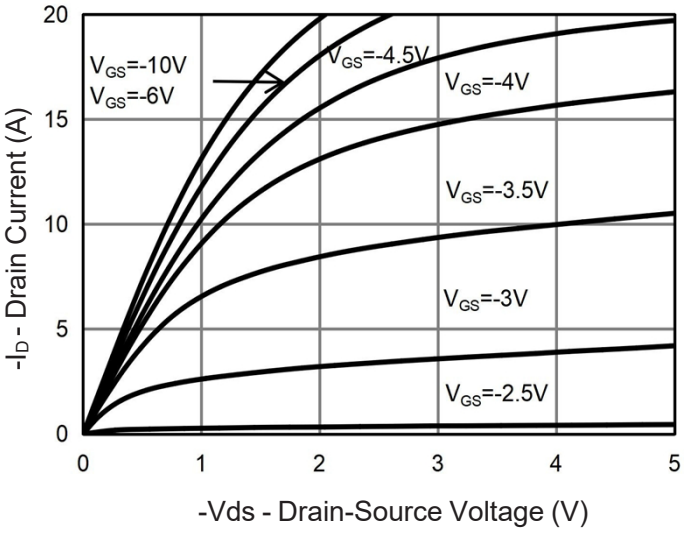


Figure 1 Output Characteristics

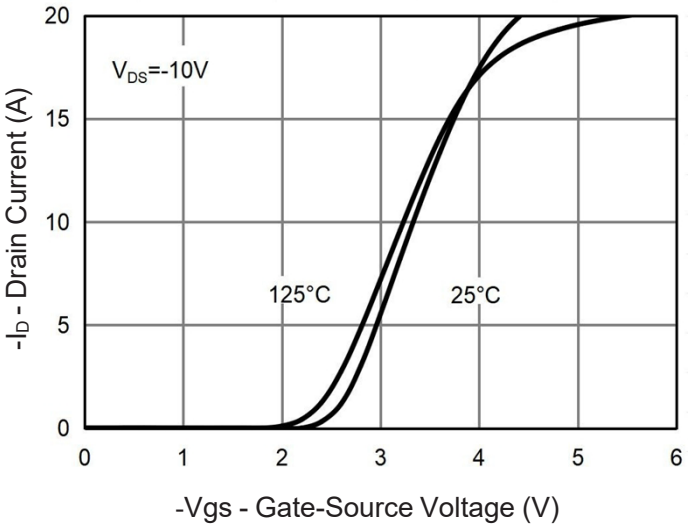


Figure 2 Transfer Characteristics

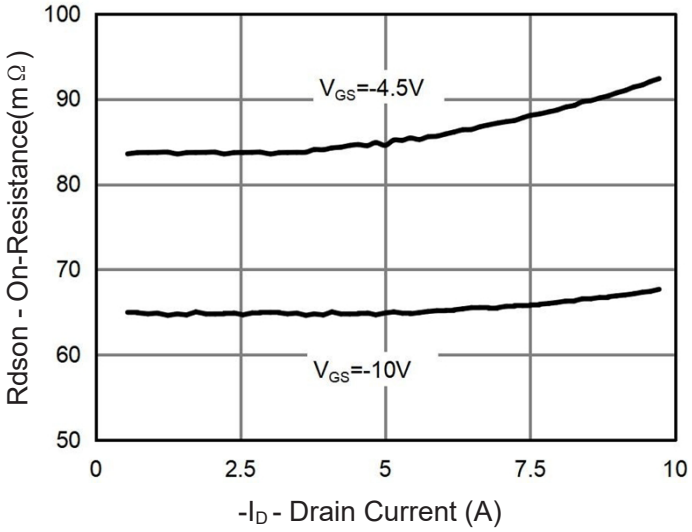


Figure 3 Rdson vs Drain Current

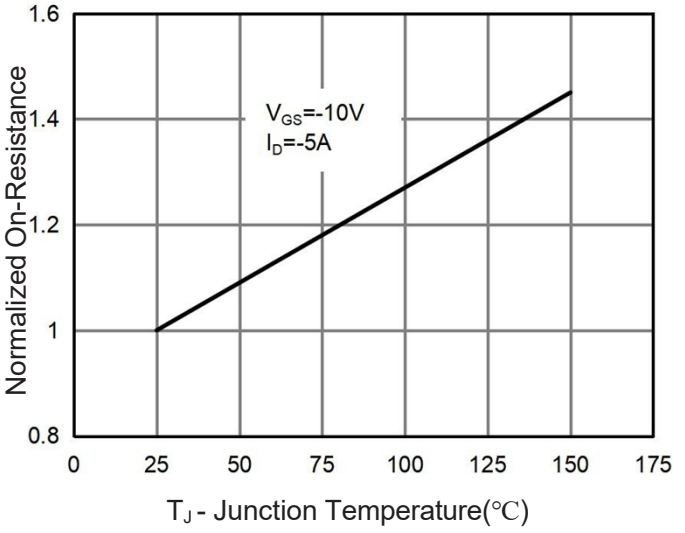


Figure 4 Rdson vs Junction Temperature

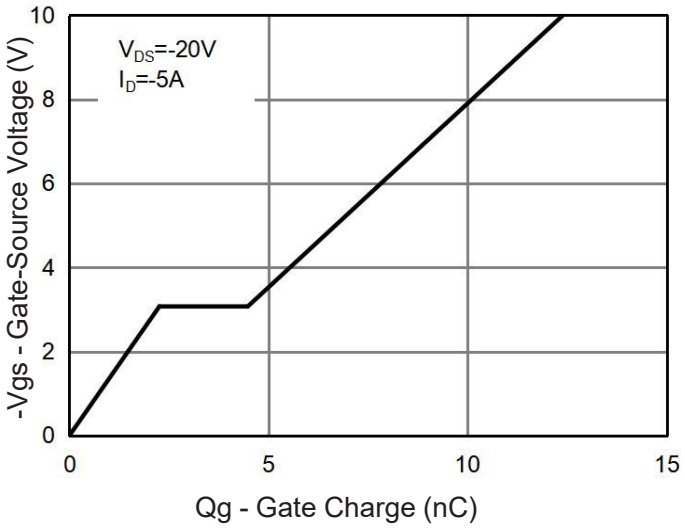


Figure 5 Gate Charge

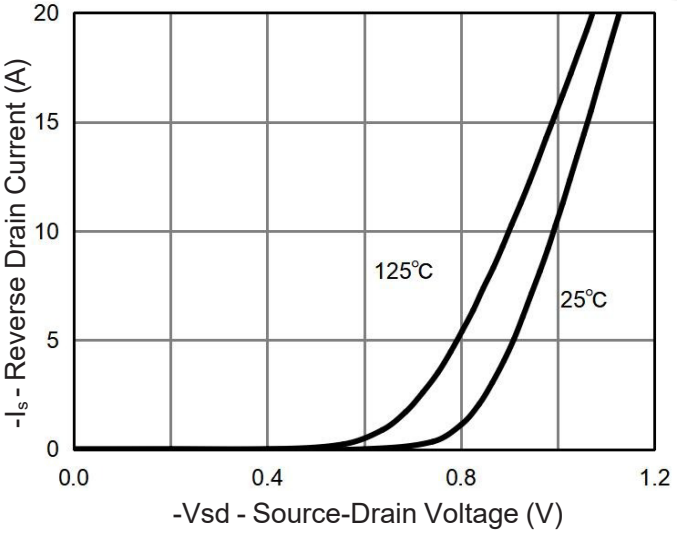


Figure 6 Source-Drain Diode Forward

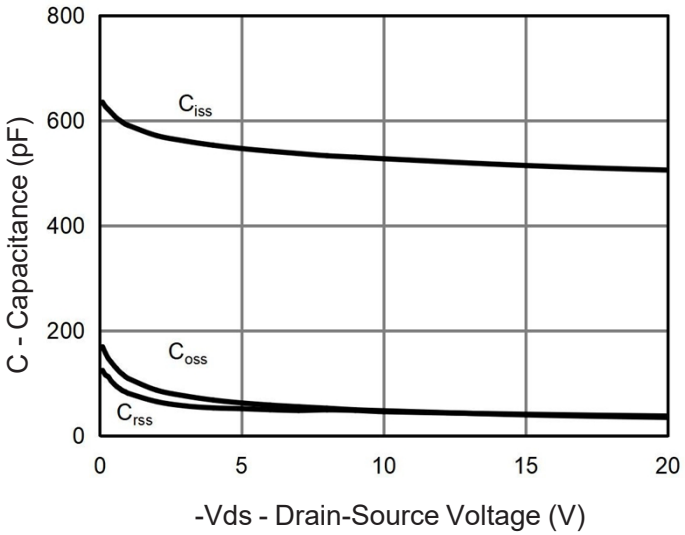


Figure 7 Capacitance vs Vds

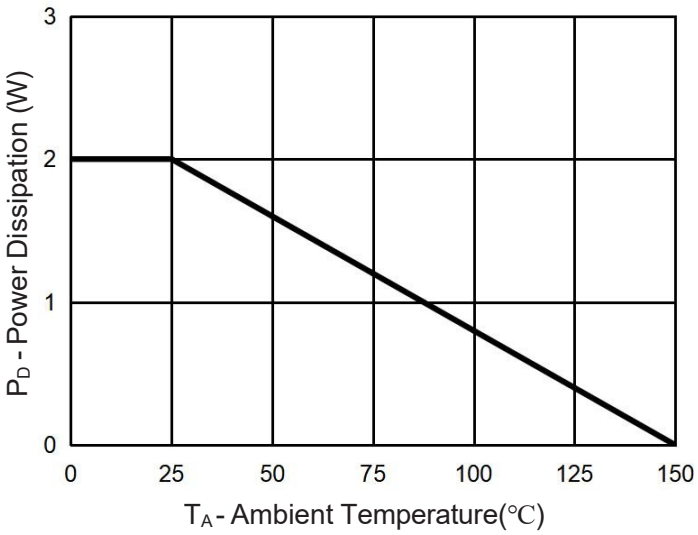


Figure 9 Power De-rating

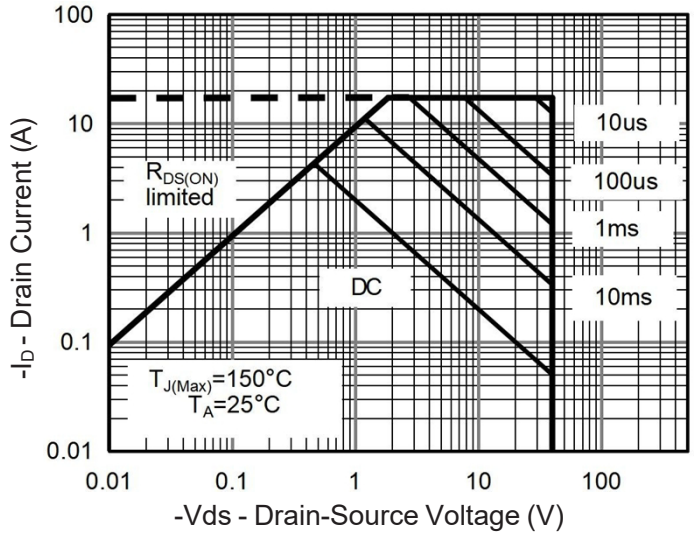


Figure 8 Safe Operation Area(Note 3)

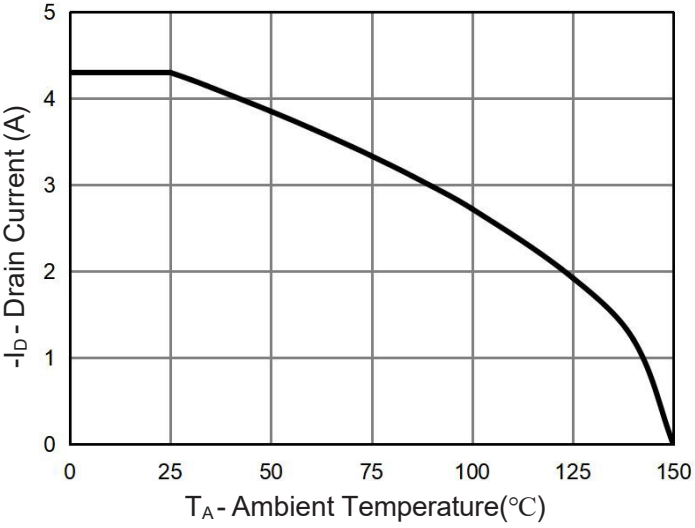


Figure10 Drain Current De-rating

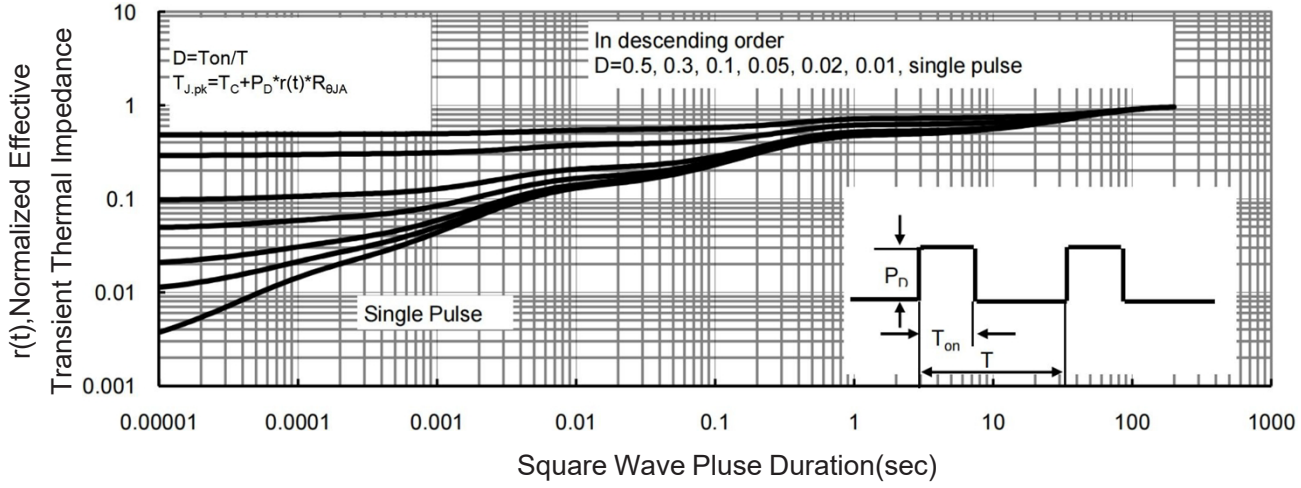


Figure 11 Normalized Maximum Transient Thermal Impedance