

Description

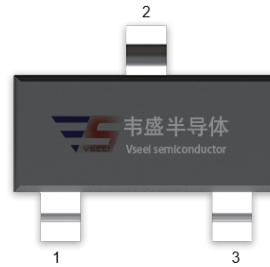
The VSM60P04SN uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge .This device is well suited for use as a load switch or in PWM applications.

General Features

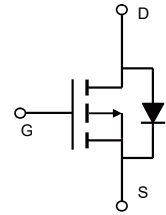
- $V_{DS} = -60V, I_D = -4A$
 $R_{DS(ON)} < 120m\Omega @ V_{GS} = -10V$
 $R_{DS(ON)} < 170m\Omega @ V_{GS} = -4.5V$
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

Application

- Load switch
- PWM application



SOT-23



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM60P04SN	VSM60P04SN-S2	SOT-23	Ø180mm	8 mm	3000 units

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-4	A
Pulsed Drain Current	I_{DM}	-12	A
Maximum Power Dissipation	P_D	1.5	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	83.3	$^\circ C/W$
Thermal Resistance, Junction-to-Lead ^(Note 2)	$R_{\theta JL}$	75	$^\circ C/W$

Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

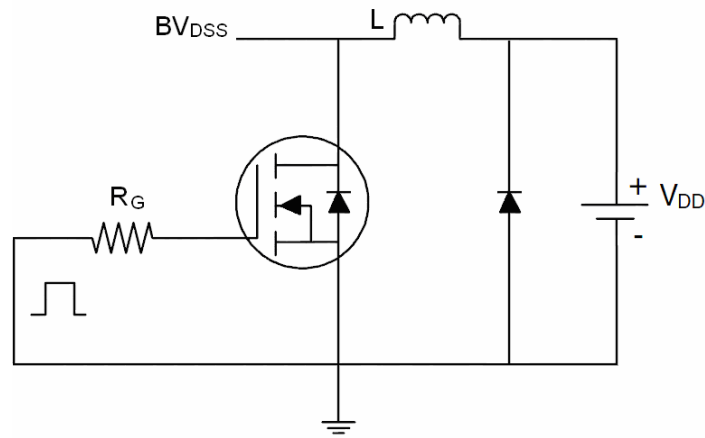
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =-250μA	-60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-60V, V _{GS} =0V	-	-	-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-1.0	-1.8	-2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-4A	-	106	120	mΩ
		V _{GS} =-4.5V, I _D =-3A	-	135	170	mΩ
Forward Transconductance	g _{FS}	V _{DS} =-5V, I _D =-4A	-	10	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =-30V, V _{GS} =0V, F=1.0MHz	-	930	-	PF
Output Capacitance	C _{oss}		-	85	-	PF
Reverse Transfer Capacitance	C _{rss}		-	35	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-30V, R _L =7.5Ω, V _{GS} =-10V, R _G =3Ω	-	8	-	nS
Turn-on Rise Time	t _r		-	4	-	nS
Turn-Off Delay Time	t _{d(off)}		-	32	-	nS
Turn-Off Fall Time	t _f		-	7	-	nS
Total Gate Charge	Q _g	V _{DS} =-30, I _D =-4A, V _{GS} =-10V	-	25	-	nC
Gate-Source Charge	Q _{gs}		-	3	-	nC
Gate-Drain Charge	Q _{gd}		-	7	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =-4A	-		-1.2	V
Diode Forward Current (Note 2)	I _S		-	-	-4	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F =- 4A	-	25		nS
Reverse Recovery Charge	Q _{rr}	di/dt = -100A/μs ^(Note3)	-	31		nC

Notes:

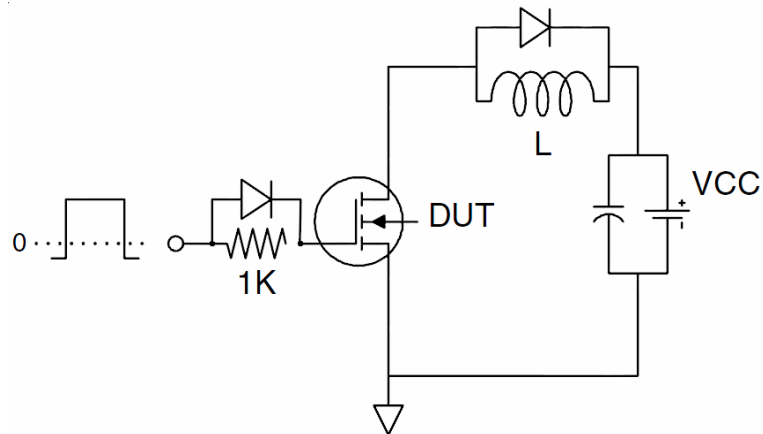
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The value in any given application depends on the user's specific board design. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

Test Circuit

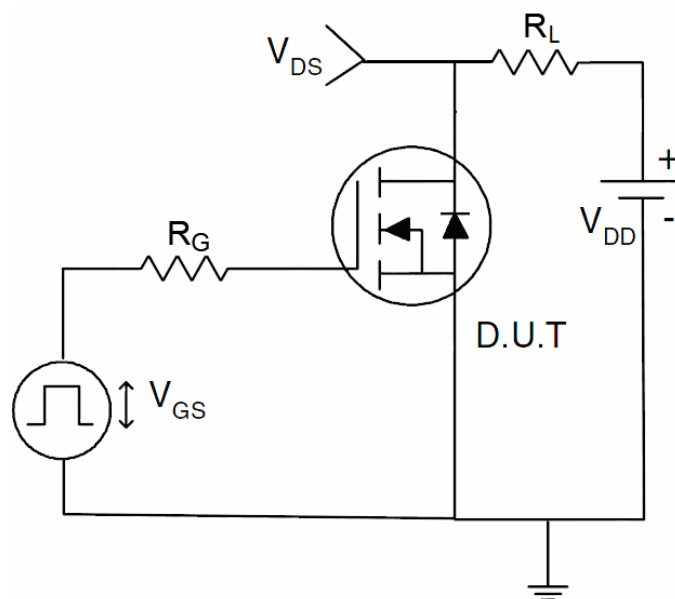
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

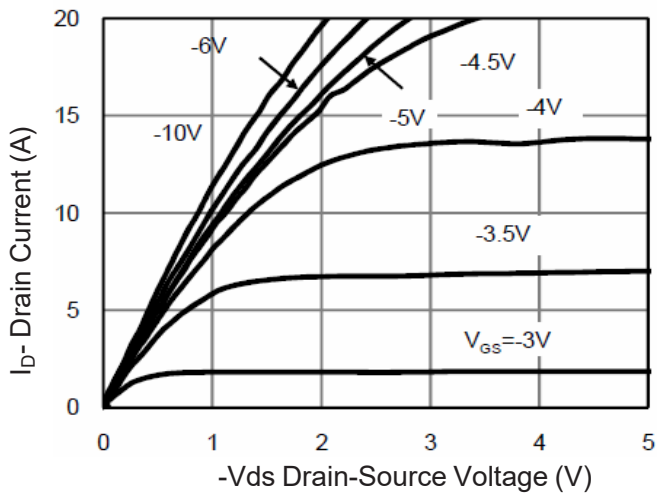


Figure 1 Output Characteristics

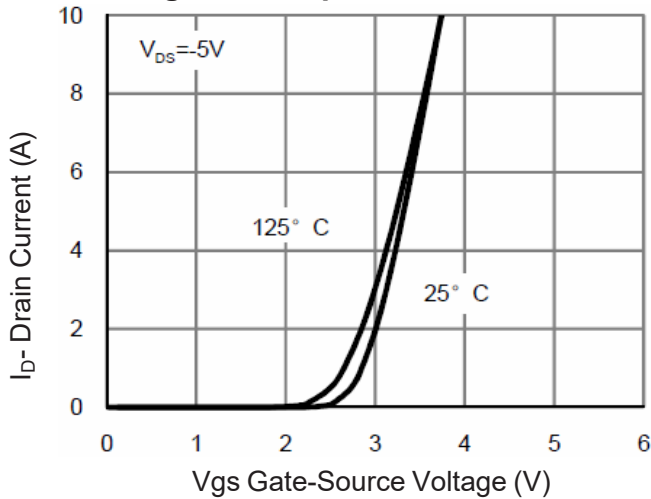


Figure 2 Transfer Characteristics

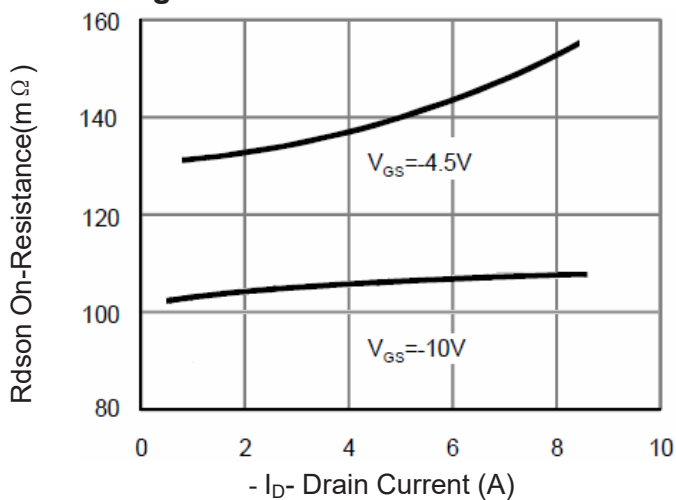


Figure 3 $R_{DS(on)}$ - Drain Current

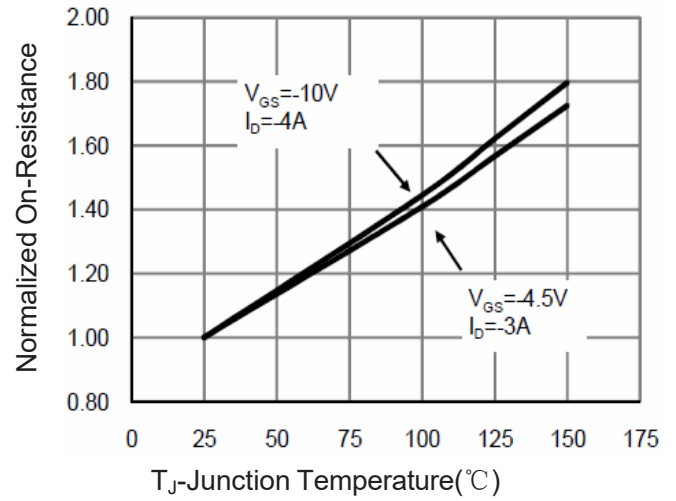


Figure 4 $R_{DS(on)}$ -Junction Temperature

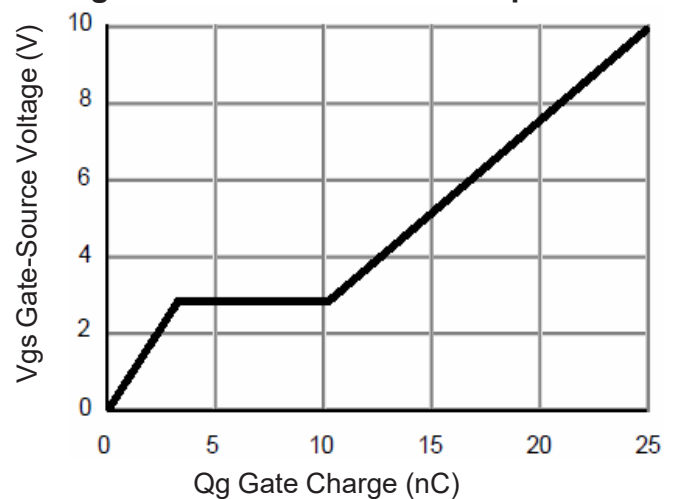


Figure 5 Gate Charge

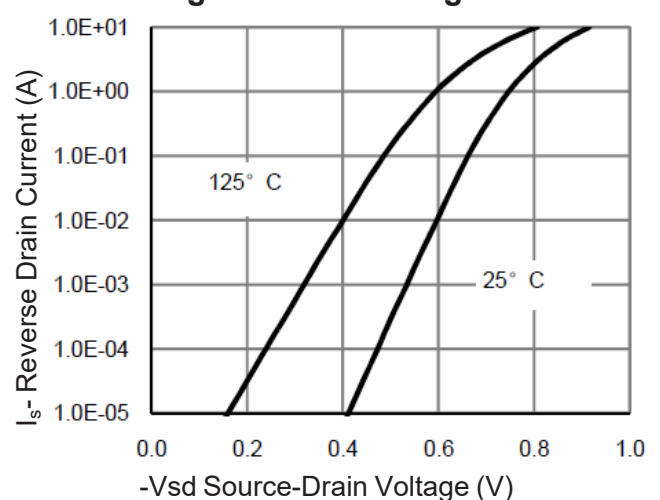
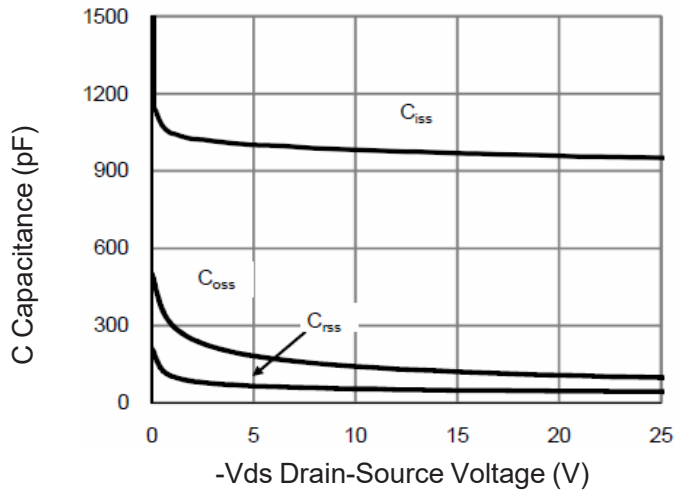
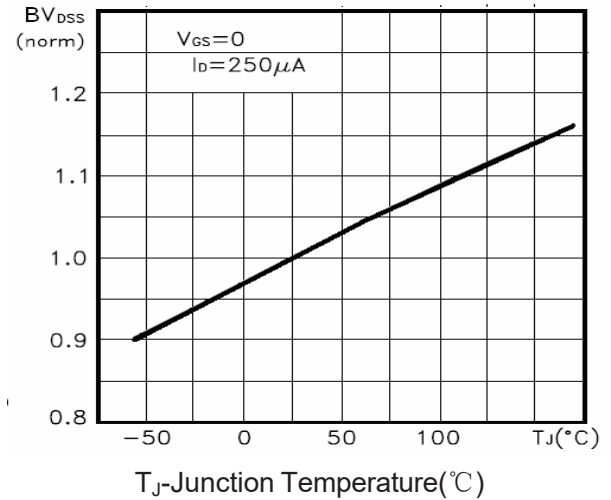
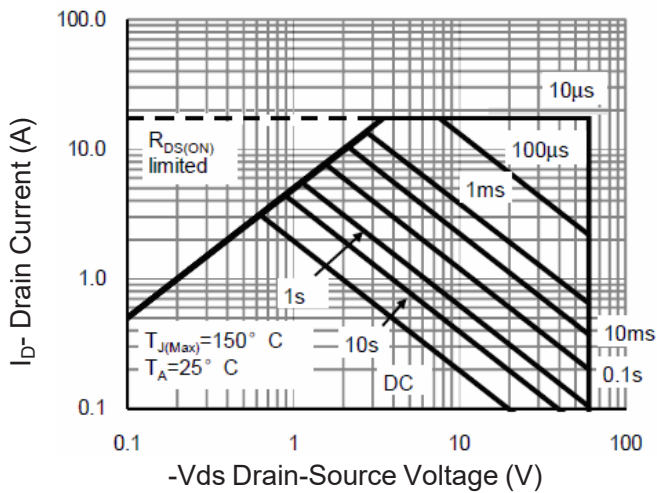
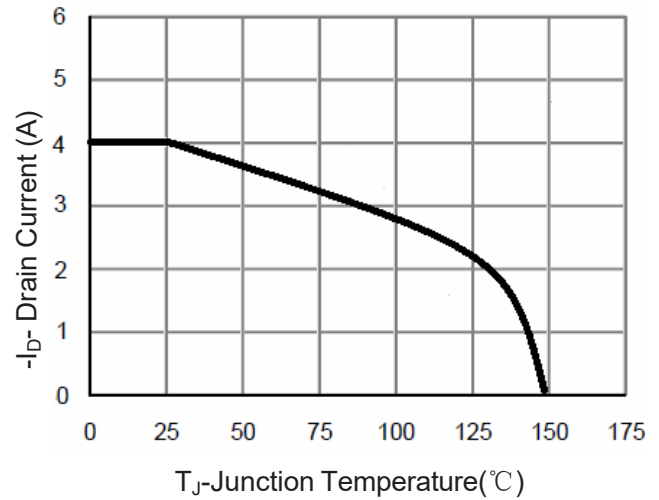
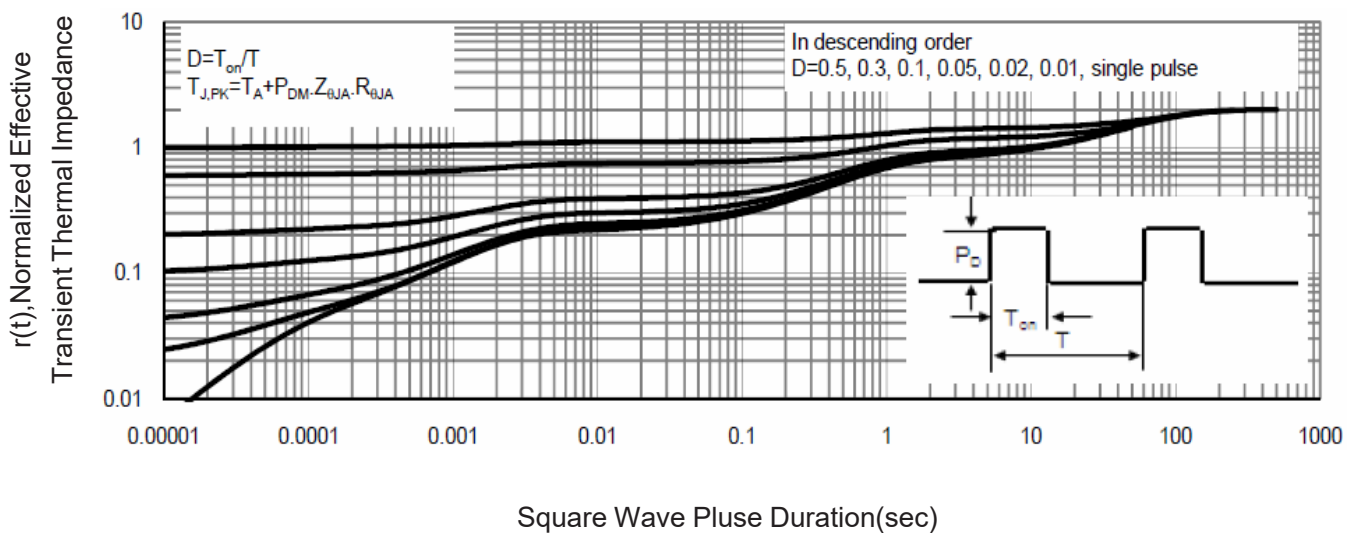


Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 BV_{DSS} vs Junction Temperature

Figure 8 Safe Operation Area

Figure 10 I_D Current De-rating

Figure 11 Normalized Maximum Transient Thermal Impedance