

Description

The VSM90P60EY uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. It is ESD protected.

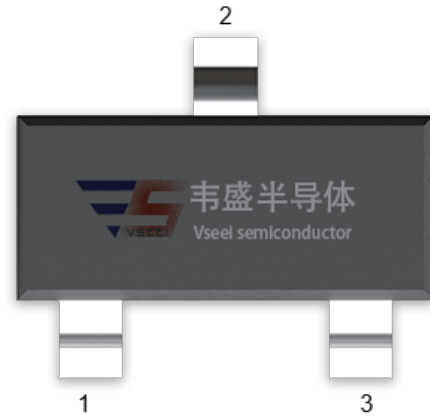
General Features

- $V_{DS} = -60V, I_D = -3A$
 $R_{DS(ON)} < 105m\Omega @ V_{GS} = -10V$ (Typ: 88mΩ)
 $R_{DS(ON)} < 115m\Omega @ V_{GS} = -4.5V$ (Typ: 98mΩ)
ESD Rating: 3000V HBM

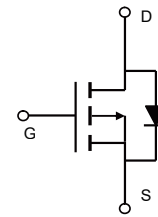
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

Application

- Load switch
- PWM application



SOT-23



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM90P60EY	VSM90P60EY-S2	SOT-23	-	-	-

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-3	A
Drain Current-Continuous($T_A = 100^\circ C$)	$I_D(100^\circ C)$	-2.2	A
Pulsed Drain Current	I_{DM}	-12	A
Maximum Power Dissipation	P_D	-1.5	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JA}$	83.3	$^\circ C/W$
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Electrical Characteristics ($T_A = 25^\circ C$ unless otherwise noted)

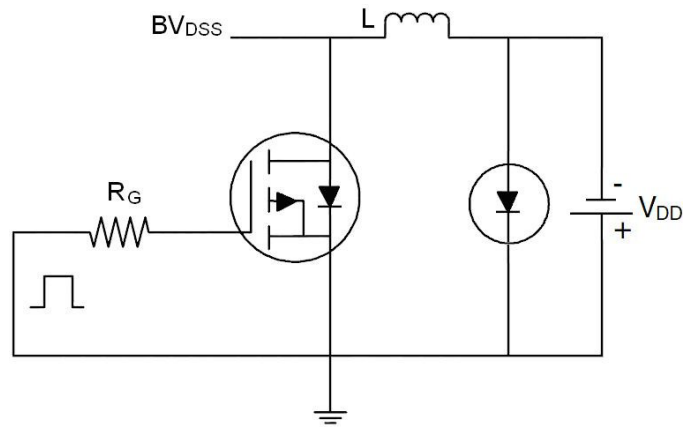
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =-250μA	-60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-60V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±10	μA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-1.1	-1.6	-2.1	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-3A	-	88	105	mΩ
		V _{GS} =-4.5V, I _D =-3A	-	98	115	mΩ
Forward Transconductance	g _{FS}	V _{DS} =-20V, I _D =-3A	-	8	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =-30V, V _{GS} =0V, F=1.0MHz	-	662.2	-	PF
Output Capacitance	C _{OSS}		-	39.9	-	PF
Reverse Transfer Capacitance	C _{rSS}		-	35.7	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-30V, R _L =10Ω V _{GS} =-10V, R _{GEN} =3Ω	-	7	-	nS
Turn-on Rise Time	t _r		-	4	-	nS
Turn-Off Delay Time	t _{d(off)}		-	28	-	nS
Turn-Off Fall Time	t _f		-	6	-	nS
Total Gate Charge	Q _g	V _{DS} =-30V, I _D =-3A, V _{GS} =-10V	-	17	-	nC
Gate-Source Charge	Q _{gs}		-	2.4	-	nC
Gate-Drain Charge	Q _{gd}		-	3.3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _s =-3A	-	-	-1.2	V
Diode Forward Current (Note 2)	I _s	-	-	-	-3	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F =-3A di/dt = 100A/μs ^(Note3)	-	27	-	nS
Reverse Recovery Charge	Q _{rr}		-	32	-	nC

Notes:

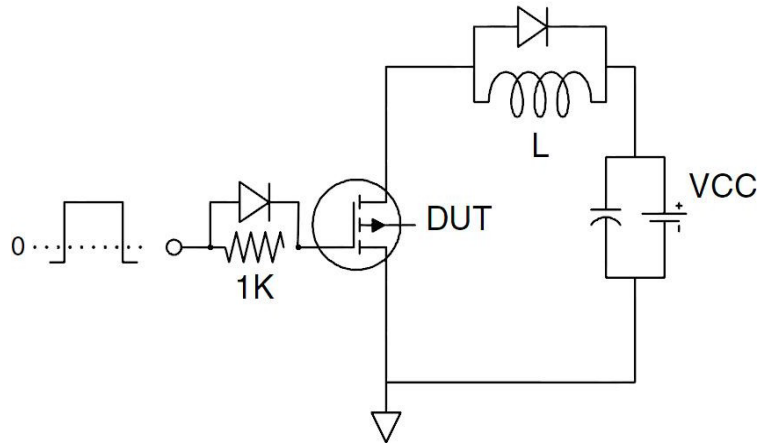
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^\circ C, V_{DD}=-30V, V_G=-10V, L=0.5mH, R_g=25\Omega$

Test Circuit

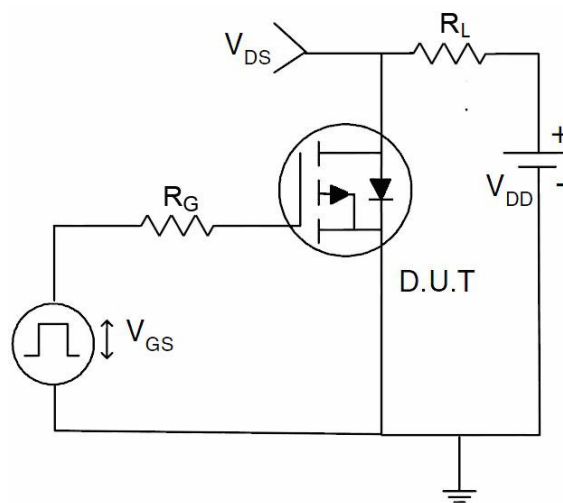
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

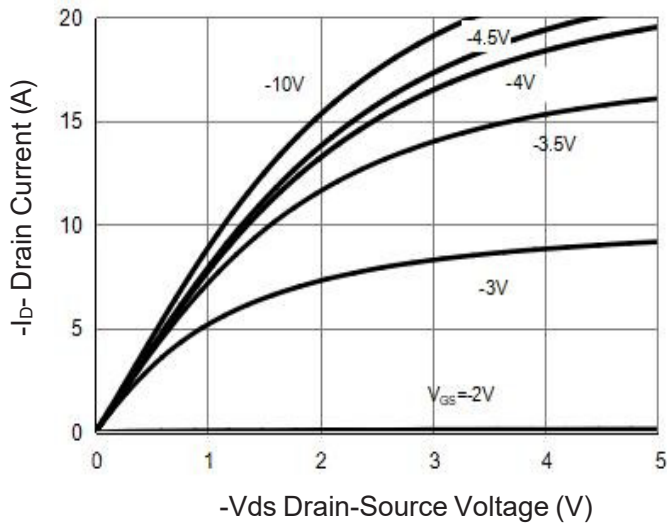


Figure 1 Output Characteristics

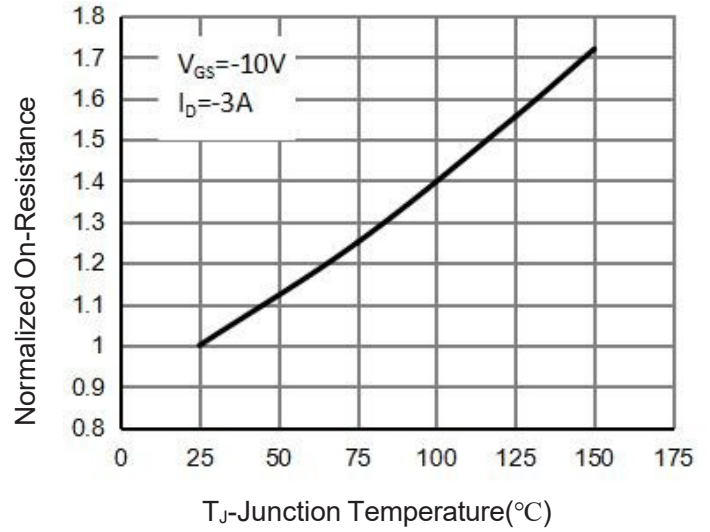


Figure 4 Rdson-Junction Temperature

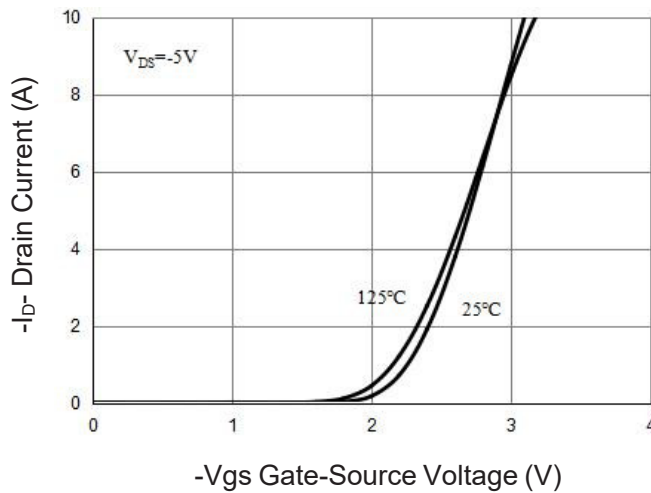


Figure 2 Transfer Characteristics

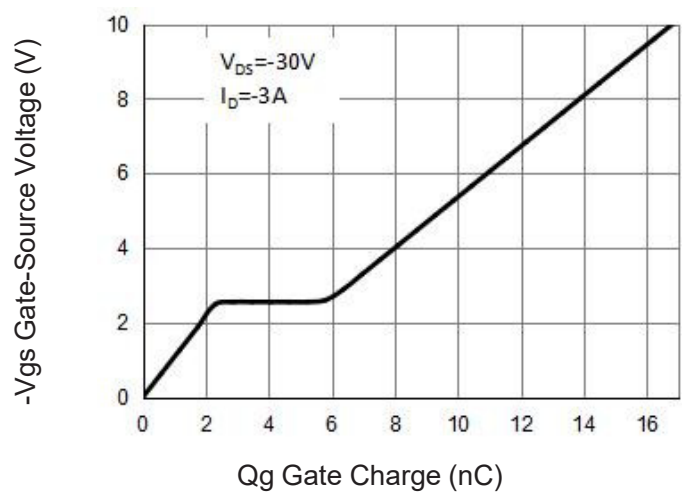


Figure 5 Gate Charge

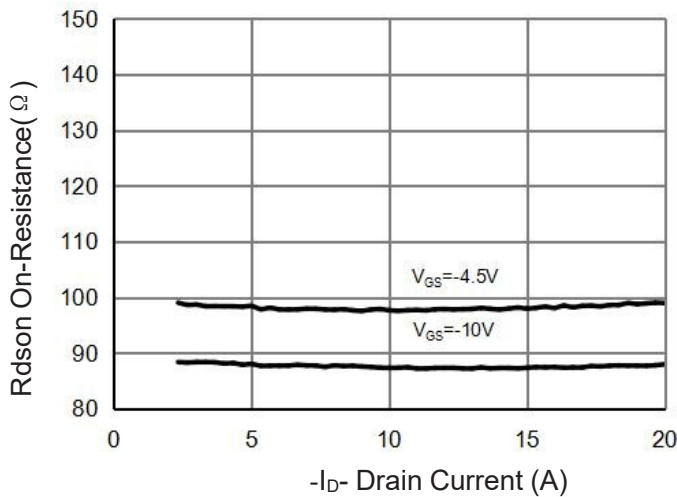


Figure 3 Rdson- Drain Current

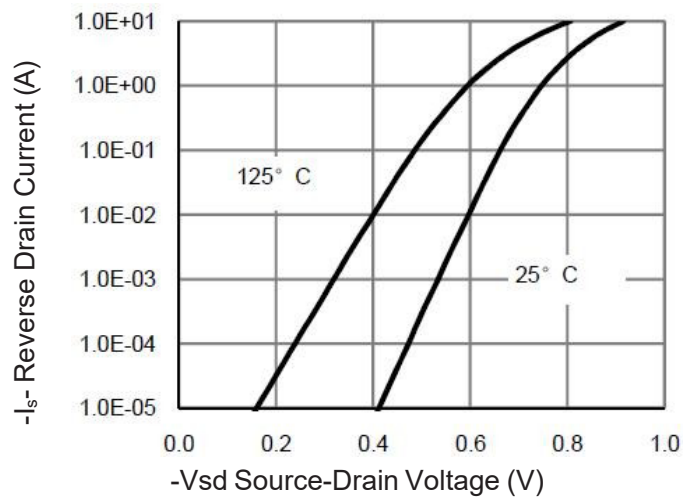
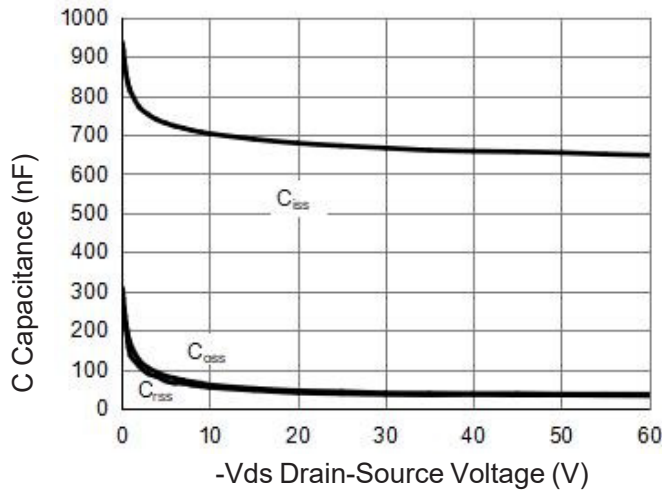
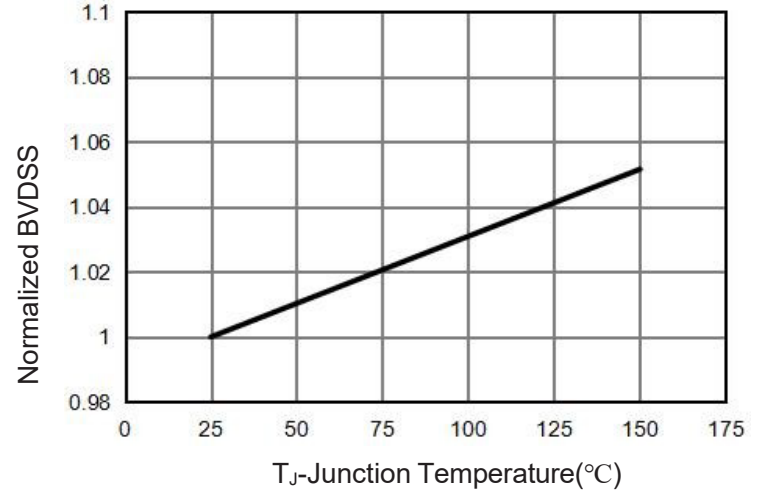
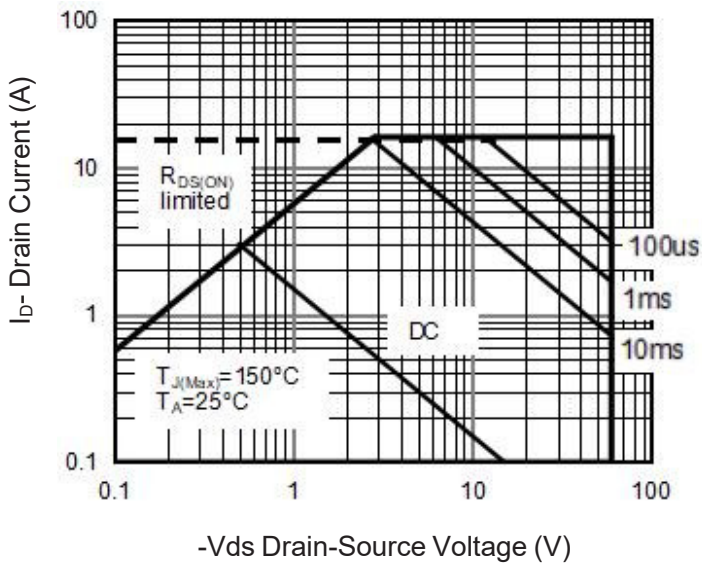
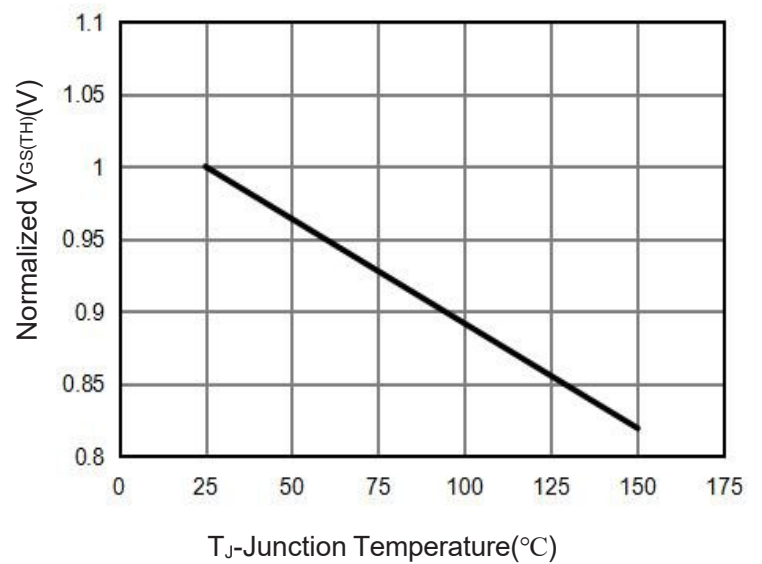
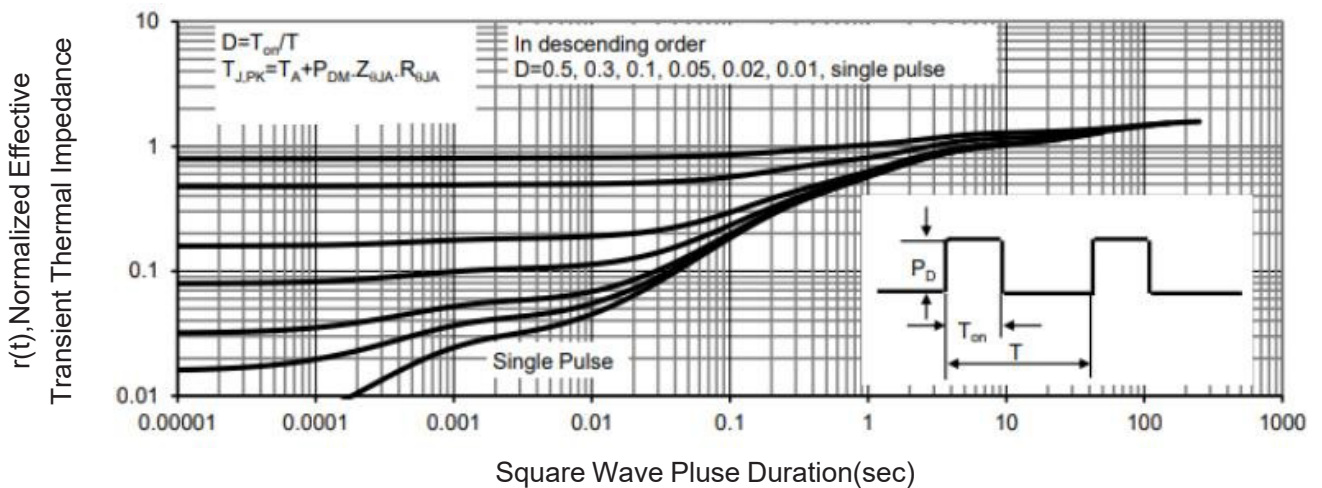


Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 Drain Current vs Case Temperature

Figure 8 Safe Operation Area

Figure 10 Power De-rating

Figure 11 Normalized Maximum Transient Thermal Impedance