

Description

The VSM12P06 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is well suited for high current load applications.

General Features

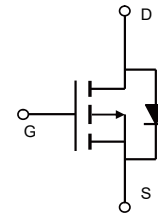
- $V_{DS} = -60V, I_D = -12A$
 $R_{DS(ON)} < 100m\Omega @ V_{GS} = -10V$
 $R_{DS(ON)} < 125m\Omega @ V_{GS} = -4.5V$
- High density cell design for ultra low $R_{DS(ON)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- High side switch for full bridge converter
- DC/DC converter for LCD display



TO-252



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM12P06	VSM12P06-T2	TO-252	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-12	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	-8.5	A
Pulsed Drain Current	I_{DM}	-30	A
Maximum Power Dissipation	P_D	60	W
Derating factor		0.4	W/ $^\circ C$
Single pulse avalanche energy (Note 5)	E_{AS}	50	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	2.5	$^{\circ}\text{C/W}$
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

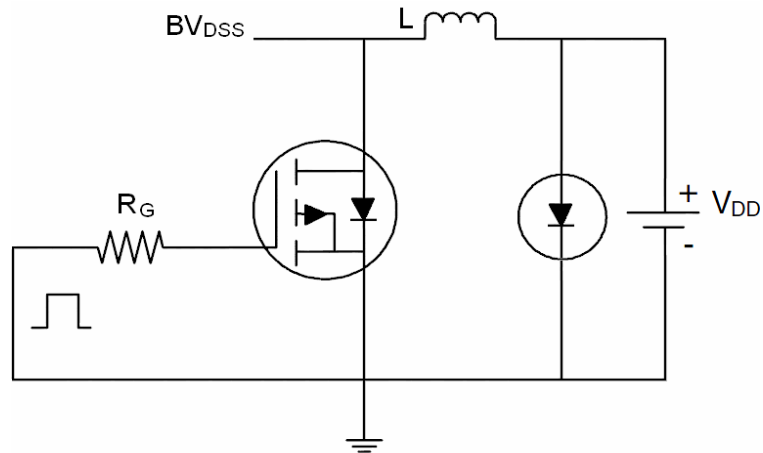
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-60V, V_{GS}=0V$	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-1.5	-2.2	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-12A$	-	84	100	m Ω
		$V_{GS}=-4.5V, I_D=-8A$	-	100	125	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=-5V, I_D=-12A$	-	10	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{iss}	$V_{DS}=-30V, V_{GS}=0V,$ $F=1.0MHz$	-	1630.7	-	PF
Output Capacitance	C_{oss}		-	90.6	-	PF
Reverse Transfer Capacitance	C_{rss}		-	77.3	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-30V, R_L=1.5\Omega,$ $V_{GS}=-10V, R_G=3\Omega$	-	11	-	nS
Turn-on Rise Time	t_r		-	14	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	33	-	nS
Turn-Off Fall Time	t_f		-	13	-	nS
Total Gate Charge	Q_g	$V_{DS}=-30, I_D=-12A,$ $V_{GS}=-10V$	-	37.6		nC
Gate-Source Charge	Q_{gs}		-	4.3		nC
Gate-Drain Charge	Q_{gd}		-	7.2		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=-12A$	-		-1.2	V
Diode Forward Current (Note 2)	I_S		-	-	-12	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}C, I_F = -12A$ $di/dt = -100A/\mu s^{(Note3)}$	-	35		nS
Reverse Recovery Charge	Q_{rr}		-	38		nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

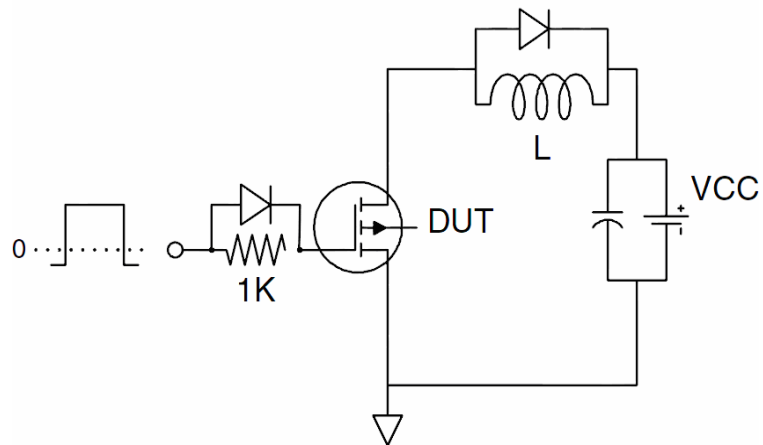
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. E_{AS} condition: $T_J=25^{\circ}\text{C}, V_{DD}=-20V, V_G=-10V, L=1\text{mH}, R_g=25\Omega$

Test Circuit

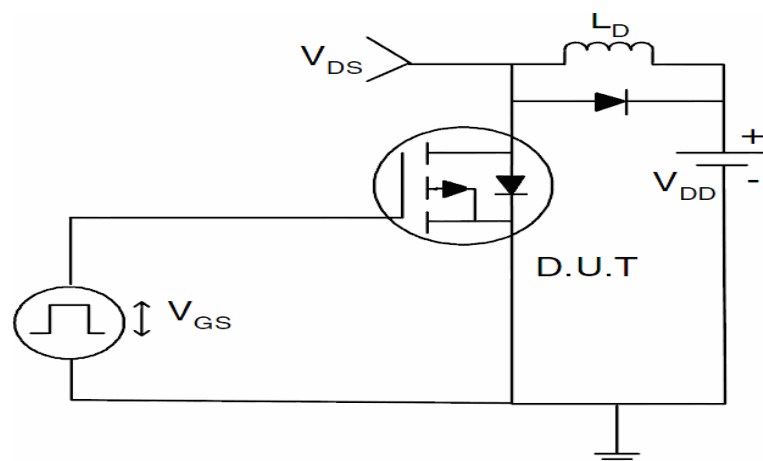
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

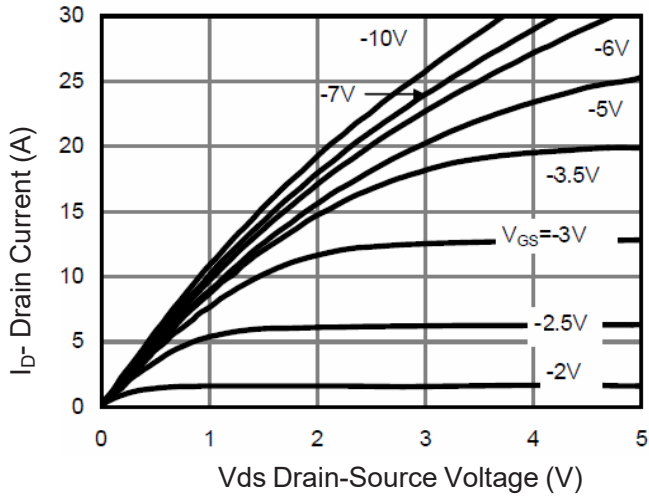


Figure 1 Output Characteristics

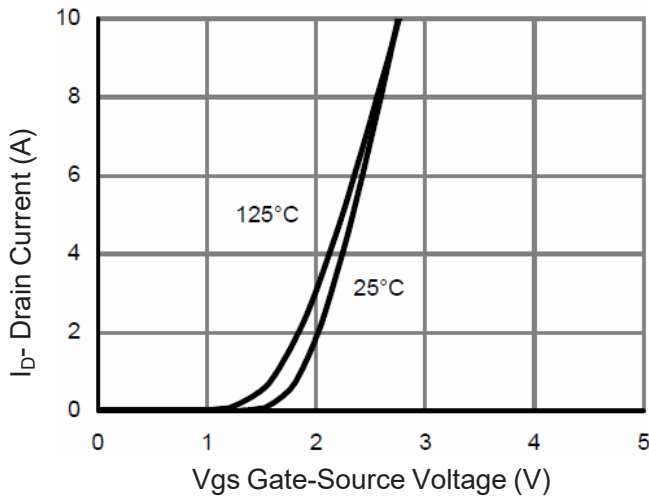


Figure 2 Transfer Characteristics

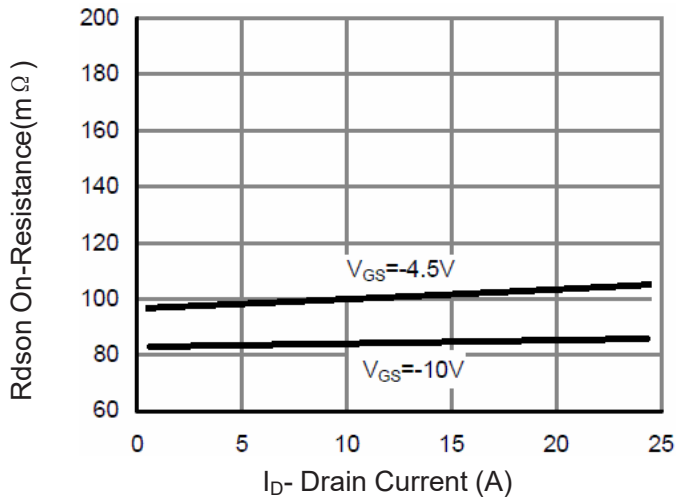


Figure 3 $R_{DS(on)}$ - Drain Current

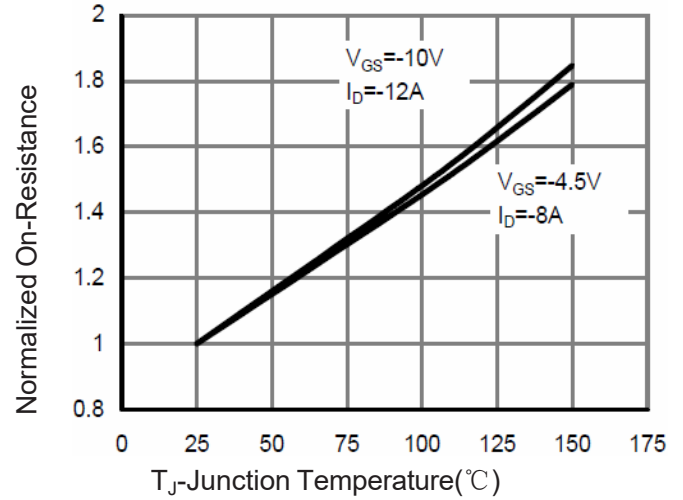


Figure 4 $R_{DS(on)}$ -Junction Temperature

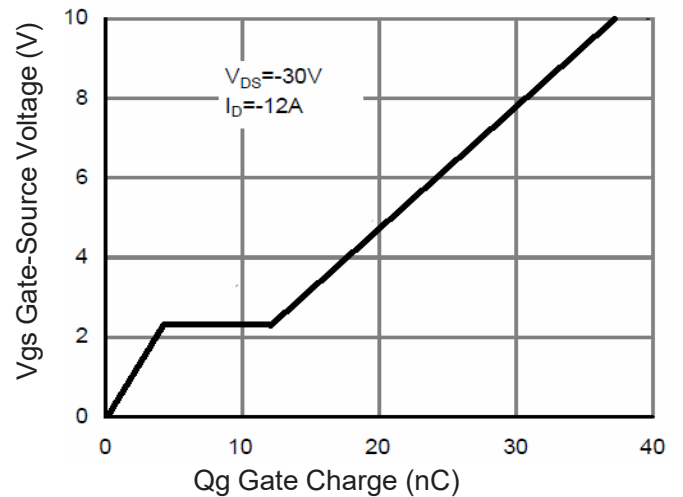


Figure 5 Gate Charge

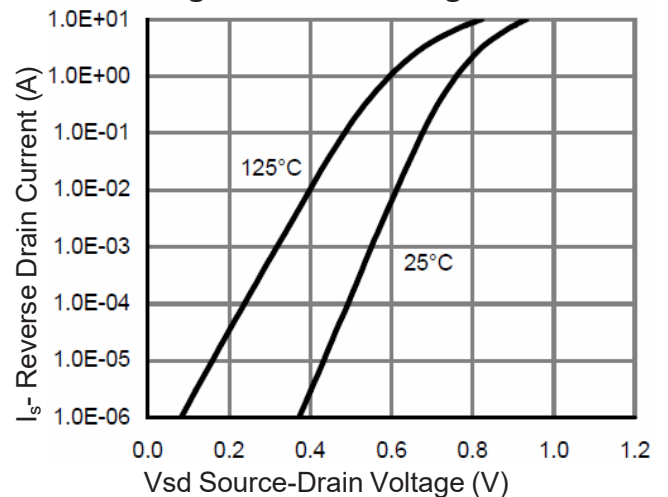
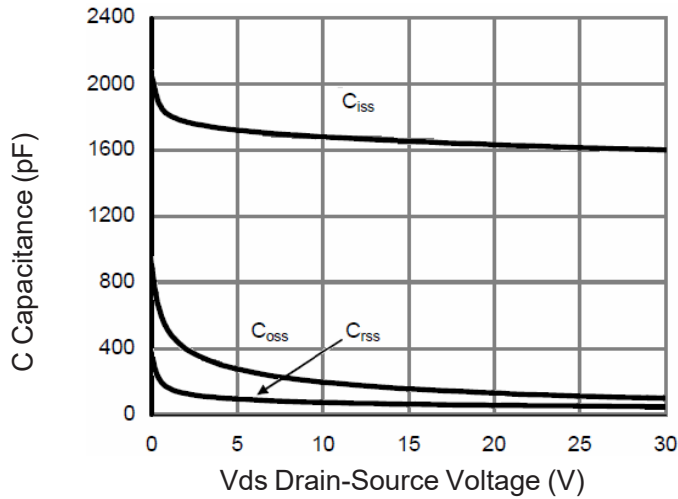
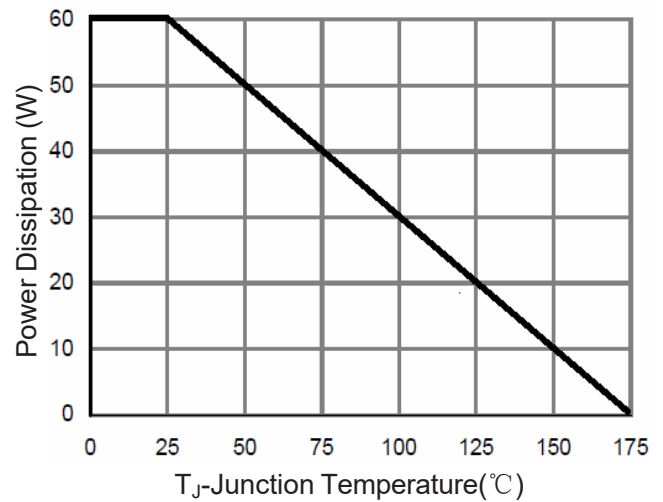
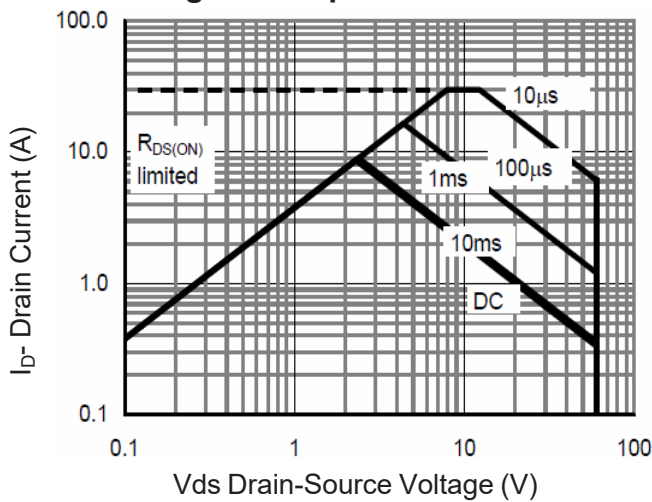
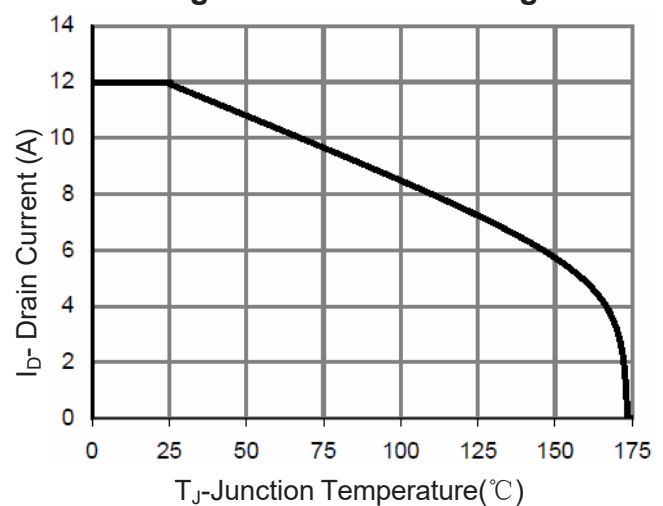
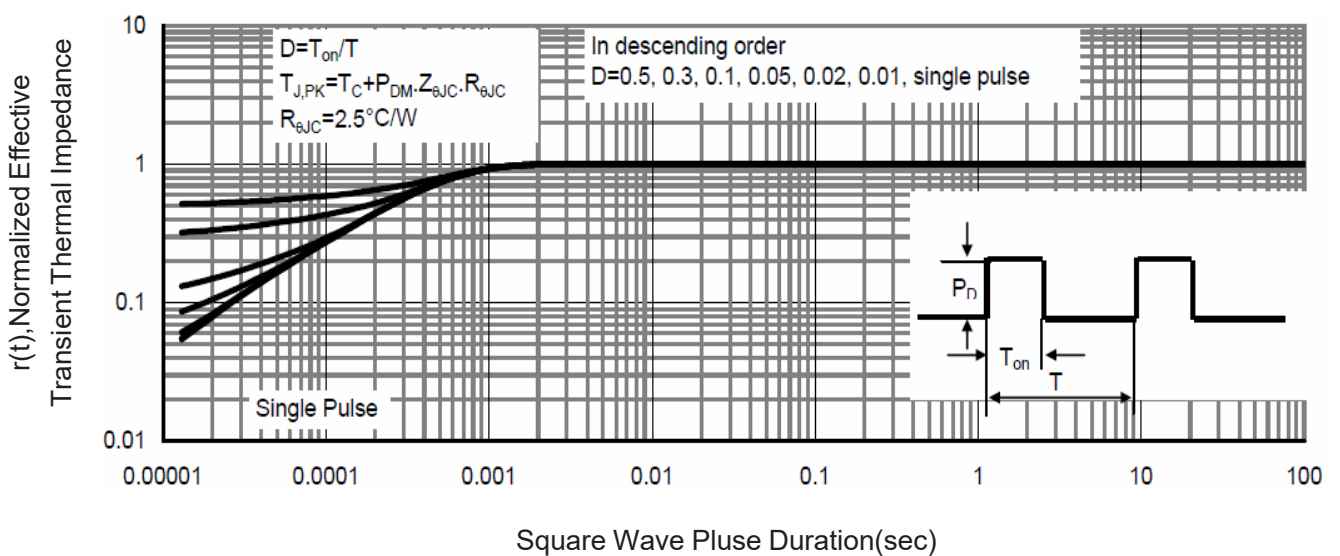


Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 Power De-rating

Figure 8 Safe Operation Area

Figure 10 ID Current De-rating

Figure 11 Normalized Maximum Transient Thermal Impedance