## Description

The VSM15P10 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

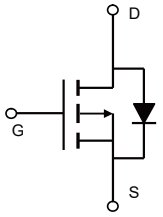
## General Features

- $V_{DS}$ =-100V,$I_D$ =-15A
  $R_{DS(ON)}$ <170mΩ @ $V_{GS}$=-10V (Typ:144mΩ)
  $R_{DS(ON)}$ <185mΩ @ $V_{GS}$=-4.5V (Typ:155mΩ)
- Super high dense cell design
- Advanced trench process technology
- Reliable and rugged
- High density cell design for ultra low On-Resistance

## Application

- Portable equipment and battery powered systems


TO-252




Schematic

## Package Marking and Ordering Information

| Device Marking | Device | Device Package | Reel Size | Tape width | Quantity |
|---|---|---|---|---|---|
| VSM15P10 | VSM15P10-T2 | TO-252 | - | - | - |

## Absolute Maximum Ratings ($T_C$=25℃unless otherwise noted)

| Parameter | Symbol | Limit | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | -100 | V |
| Gate-Source Voltage | $V_{GS}$ | ±20 | V |
| Drain Current-Continuous | $I_D$ | -15 | A |
| Drain Current-Continuous($T_C$=100℃) | $I_D$ (100℃) | -11 | A |
| Pulsed Drain Current | $I_{DM}$ | -60 | A |
| Maximum Power Dissipation | $P_D$ | 85 | W |
| Single pulse avalanche energy (Note 5) | $E_{AS}$ | 64 | mJ |
| Derating factor | | 0.57 | W/℃ |
| Operating Junction and Storage Temperature Range | $T_J$,$T_{STG}$ | -55 To 175 | ℃ |

## Thermal Characteristic

| | | | |
|---|---|---|---|
| Thermal Resistance,Junction-to-Case (Note 2) | $R_{\theta JC}$ | 1.76 | ℃/W |
| Thermal Resistance,Junction-to-Ambient | $R_{\theta JA}$ | 50 | ℃/W |

## Electrical Characteristics ($T_C$=25℃unless otherwise noted)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$=0V $I_D$=-250μA | -100 | - | - | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$=-100V,$V_{GS}$=0V | - | - | 1 | μA |
| Gate-Body Leakage Current | $I_{GSS}$ | $V_{GS}$=±20V,$V_{DS}$=0V | - | - | ±100 | nA |
| **On Characteristics** (Note 3) | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$,$I_D$=-250μA | -1.3 | -1.9 | -2.5 | V |
| Drain-Source On-State Resistance | $R_{DS(ON)}$ | $V_{GS}$=-10V, $I_D$=-12A | - | 144 | 170 | mΩ |
| | | $V_{GS}$=-4.5V, $I_D$=-12A | - | 155 | 185 | mΩ |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$=-18V,$I_D$=-12A | - | 33 | - | S |
| **Dynamic Characteristics** (Note4) | | | | | | |
| Input Capacitance | $C_{lss}$ | $V_{DS}$=-50V,$V_{GS}$=0V, F=1.0MHz | - | 1835 | - | pF |
| Output Capacitance | $C_{oss}$ | | - | 43.7 | - | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 39.8 | - | pF |
| **Switching Characteristics** (Note 4) | | | | | | |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}$=-50V,$I_D$=-15A $V_{GS}$=-10V,$R_{GEN}$=2Ω | - | 6 | - | nS |
| Turn-on Rise Time | $t_r$ | | - | 3 | - | nS |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 40 | - | nS |
| Turn-Off Fall Time | $t_f$ | | - | 25 | - | nS |
| Total Gate Charge | $Q_g$ | $V_{DS}$=-50V,$I_D$=-12A, $V_{GS}$=-10V | - | 36.6 | - | nC |
| Gate-Source Charge | $Q_{gs}$ | | - | 6.56 | - | nC |
| Gate-Drain Charge | $Q_{gd}$ | | - | 7.7 | - | nC |
| **Drain-Source Diode Characteristics** | | | | | | |
| Diode Forward Voltage (Note 3) | $V_{SD}$ | $V_{GS}$=0V,$I_S$=-15A | - | - | -1.2 | V |
| Diode Forward Current (Note 2) | $I_S$ | - | - | - | -15 | A |
| Reverse Recovery Time | $t_{rr}$ | TJ = 25°C, IF =-15A di/dt = 100A/μs(Note3) | - | 69 | - | nS |
| Reverse Recovery Charge | Qrr | | - | 218 | - | nC |
| Forward Turn-On Time | $t_{on}$ | Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD) | | | | |

## Notes:

**1.** Repetitive Rating: Pulse width limited by maximum junction temperature.

**2.** The value of $R_{\theta JA}$ is measured with the device mounted on 1$in^2$ FR-4 board with 2oz. Copper, in a still air environment with $T_A$ =25° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150° C may be used if the PCB allows it.

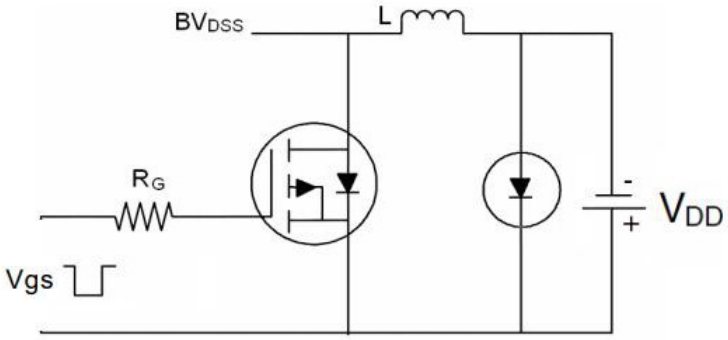
**3.** Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

**4.** Guaranteed by design, not subject to production

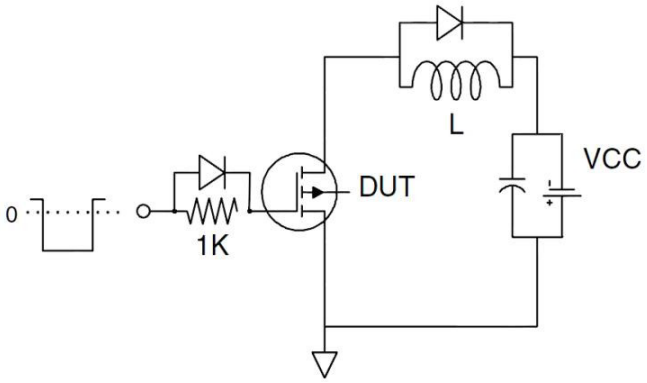
**5.** EAS condition：Tj=25℃,$V_{DD}$=-50V,$V_G$=-10V,L=0.5mH,Rg=25Ω

## Test Circuit

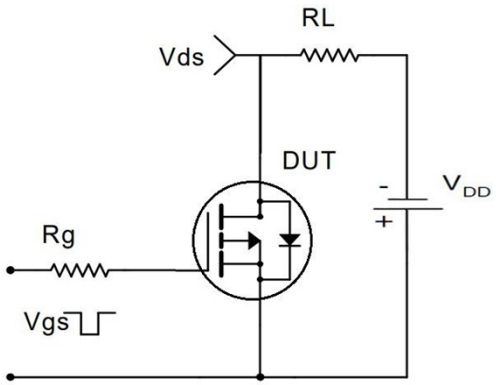
### 1） $E_{AS}$ test Circuit




### 2） Gate charge test Circuit




### 3） Switch Time Test Circuit



## Typical Electrical and Thermal Characteristics (Curves)

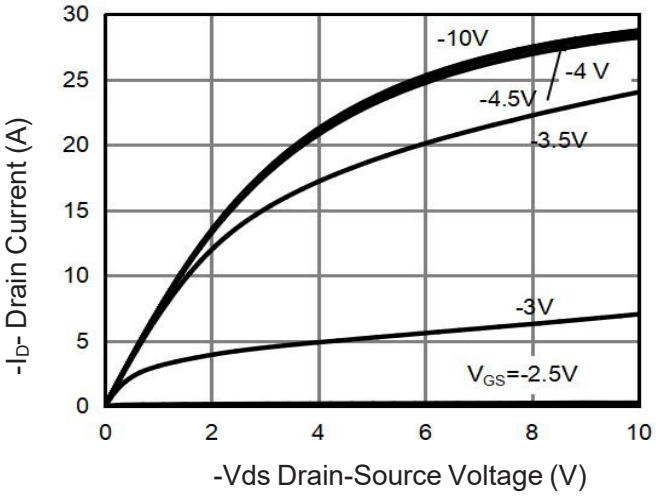



**Figure 1 Output Characteristics**

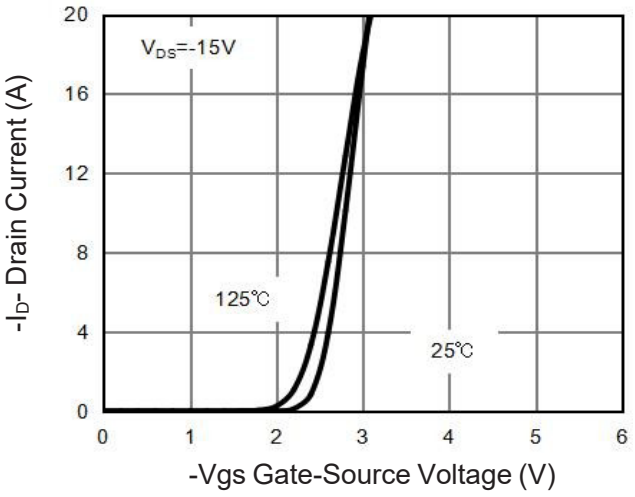



**Figure 2 Transfer Characteristics**

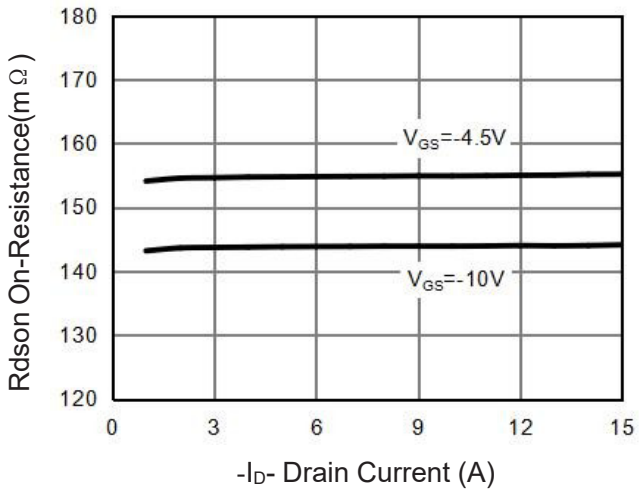



**Figure 3 Rdson- Drain Current**

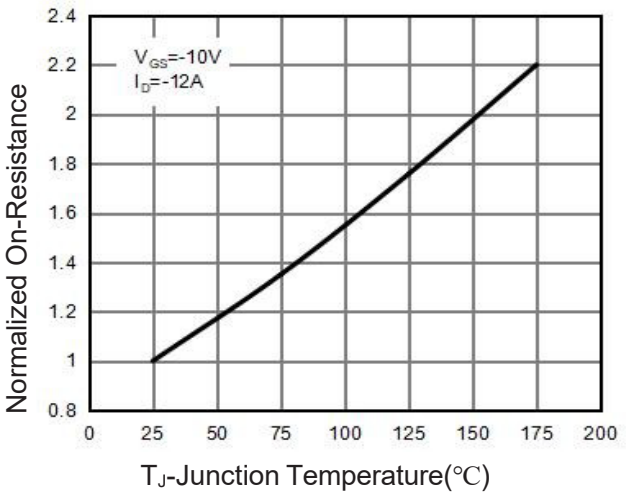



**Figure 4 Rdson-JunctionTemperature**

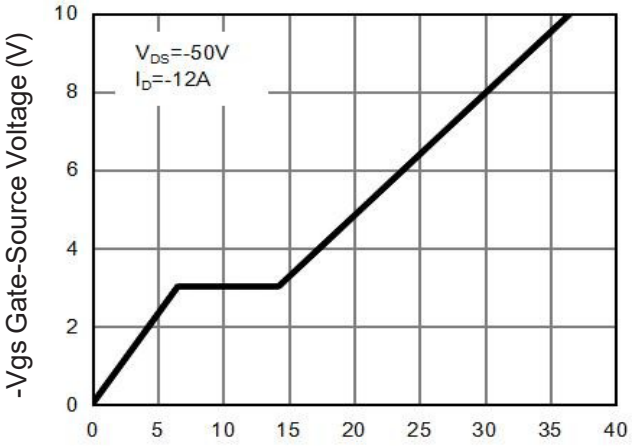



**Figure 5 Gate Charge**

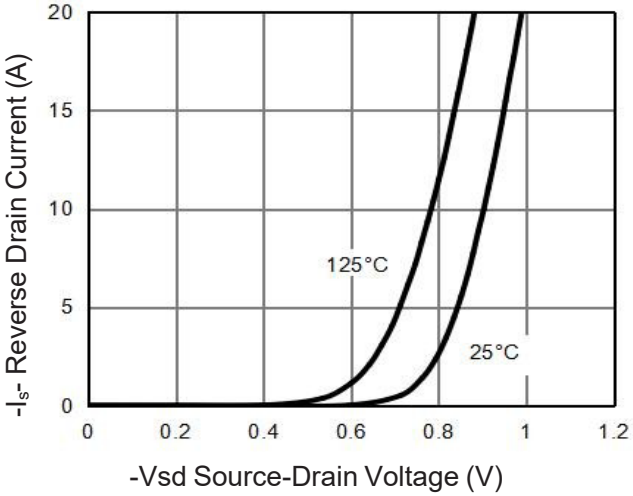



**Figure 6 Source- Drain Diode Forward**

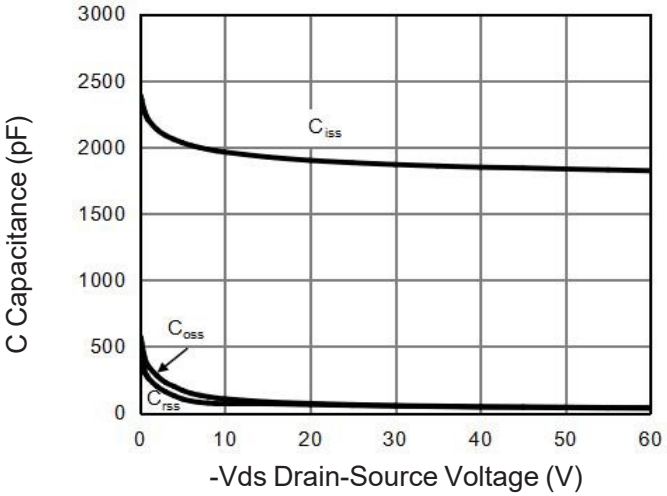



**Figure 7 Capacitance vs Vds**

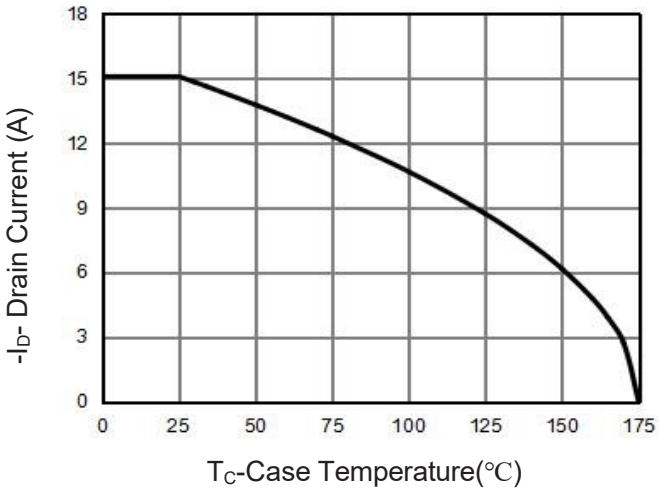



**Figure 9 Drain Current vs Case Temperature**

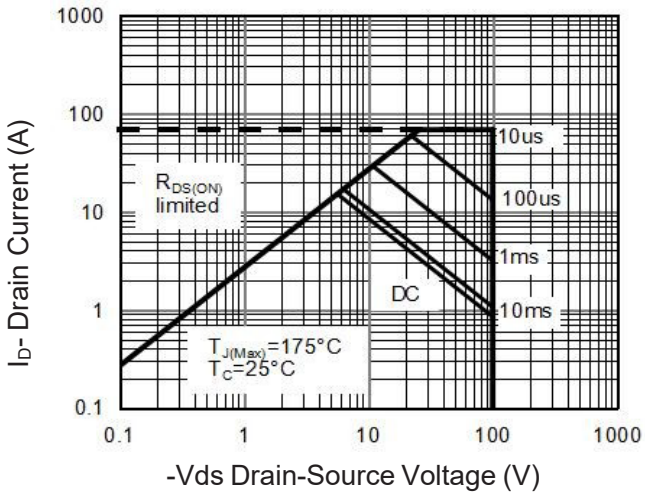



**Figure 8 Safe Operation Area**

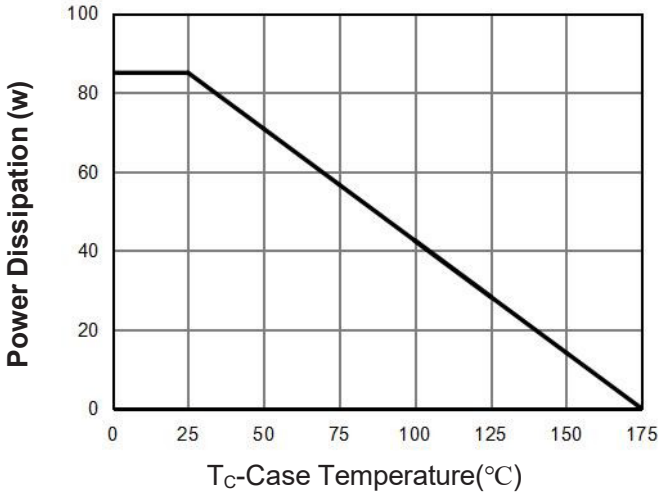



**Figure 10 Power De-rating**

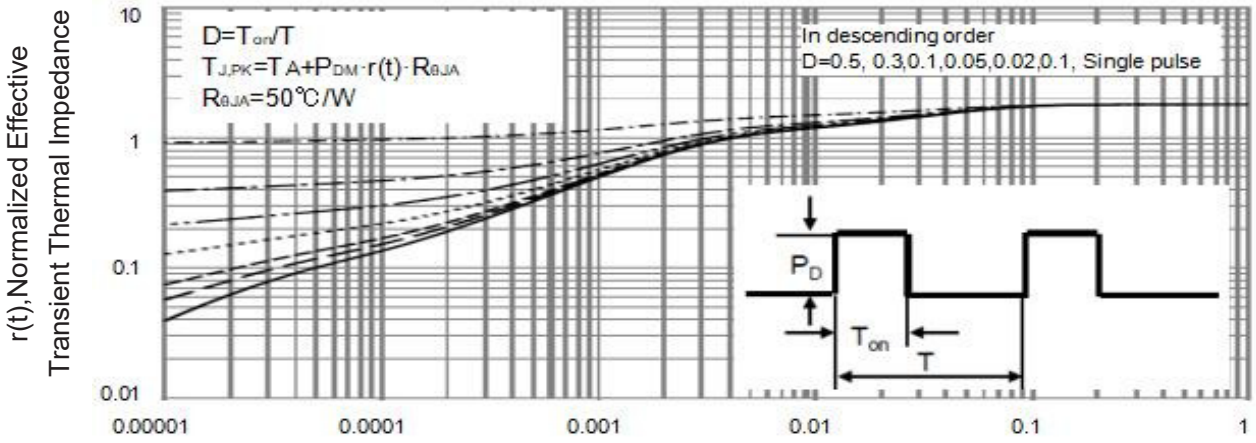



**Figure 11 Normalized Maximum Transient Thermal Impedance**