

Description

The VSM20P10 uses advanced trench technology and design to provide excellent $R_{DS(on)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

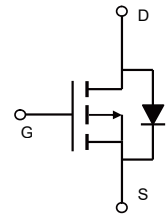
- $V_{DS} = -100\text{ V}, I_D = -20\text{ A}$
 $R_{DS(on)} < 96\text{ m}\Omega @ V_{GS} = -10\text{ V}$
 $R_{DS(on)} < 106\text{ m}\Omega @ V_{GS} = -4.5\text{ V}$
- High density cell design for ultra low $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Portable equipment and battery powered systems



TO-252



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM20P10	VSM20P10-T2	TO-252	Ø330mm	16mm	2500units

Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-20	A
Drain Current-Continuous(100°C)	$I_D(100^\circ\text{C})$	-16.5	A
Pulsed Drain Current ($T_C = 25^\circ\text{C}$)	I_{DM}	-80	A
Maximum Power Dissipation	P_D	126	W
Derating factor		0.84	W/ $^\circ\text{C}$
Single pulse avalanche energy ^(Note 1)	E_{AS}	134	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.19	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	50	$^\circ\text{C/W}$

Electrical Characteristics (T_C=25°C unless otherwise noted)

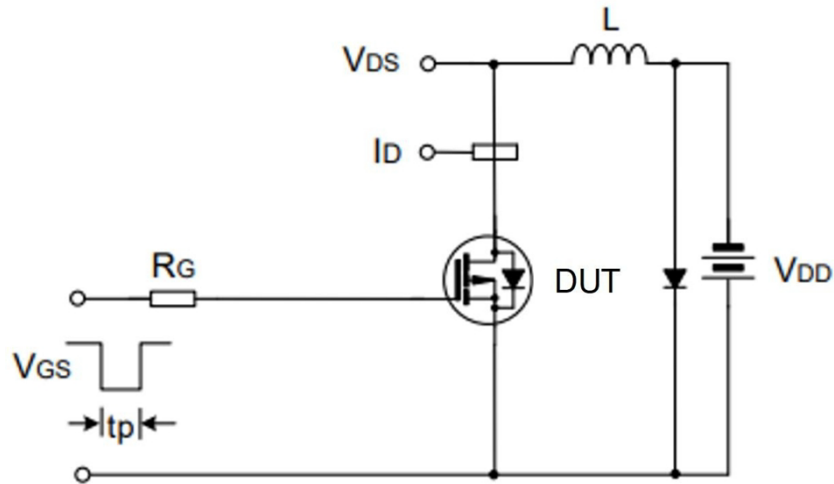
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =-250μA	-100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-100V, V _{GS} =0V	-	-	-1	uA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-1.3	-1.9	-2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-20A	-	80	96	mΩ
		V _{GS} =-4.5V, I _D =-20A	-	88	106	
Forward Transconductance	g _{FS}	V _{DS} =-10V, I _D =-20A	-	40	-	S
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} =-50V, V _{GS} =0V, F=1.0MHz	-	3233.3	-	pF
Output Capacitance	C _{oss}		-	70.5	-	pF
Reverse Transfer Capacitance	C _{rss}		-	62.8	-	pF
Switching Characteristics (Note 3)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-50V, I _D =-10A, V _{GS} =-12V, R _{GEN} =3Ω	-	12	-	nS
Turn-on Rise Time	t _r		-	15	-	nS
Turn-off Delay Time	t _{d(off)}		-	35	-	nS
Turn-off Fall Time	t _f		-	14	-	nS
Total Gate Charge	Q _g	V _{DS} =-50V, I _D =-10A, V _{GS} =-10V	-	52.2	-	nC
Gate-Source Charge	Q _{gs}		-	10	-	nC
Gate-Drain Charge	Q _{gd}		-	9.6	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _S =-20A	-	-	-1.2	V
Diode Forward Current	I _S		-	-	-20	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F =10A di/dt = -100A/μs	-	47	-	nS
Reverse Recovery Charge	Q _{rr}		-	71	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

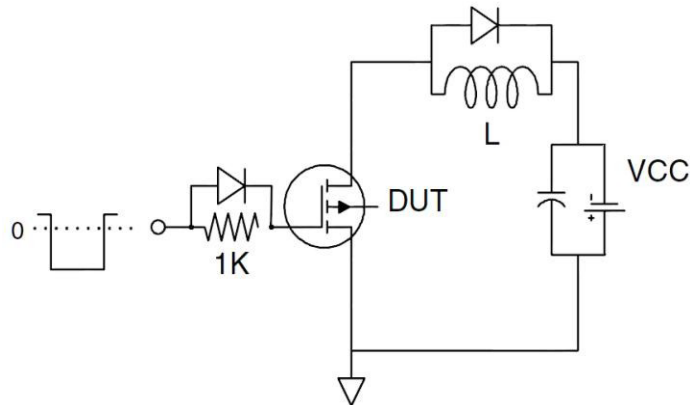
1. EAS condition : T_J=25°C, V_{DD}=-50V, V_G=-10V, L=0.5mH, R_g=25Ω.
2. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The maximum allowed junction temperature of 175°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.
3. Guaranteed by design, not subject to production.
4. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175°C. The SOA curve provides a single pulse rating.

Test Circuit

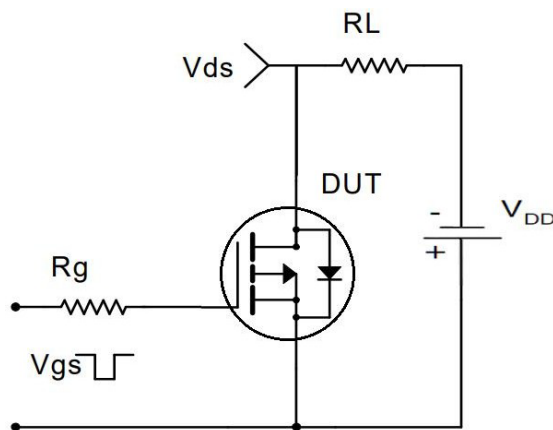
1) E_{AS} Test Circuit



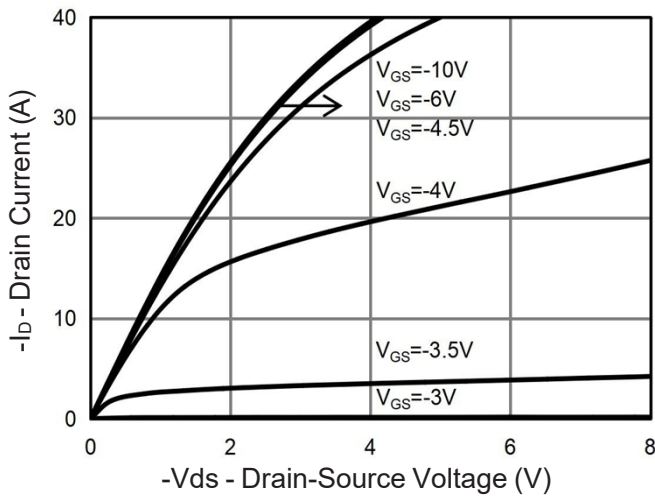
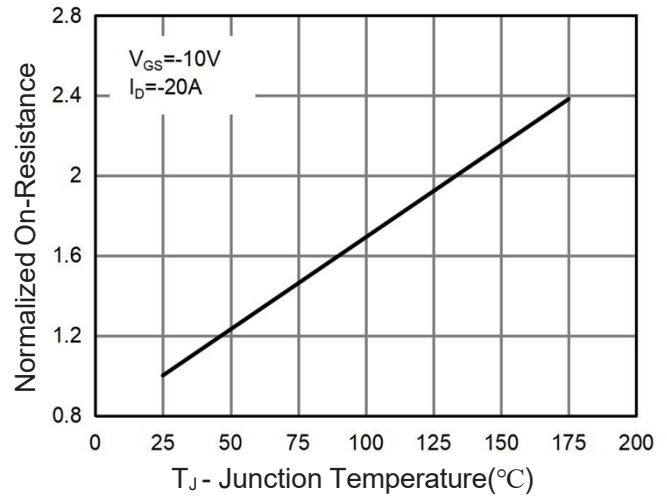
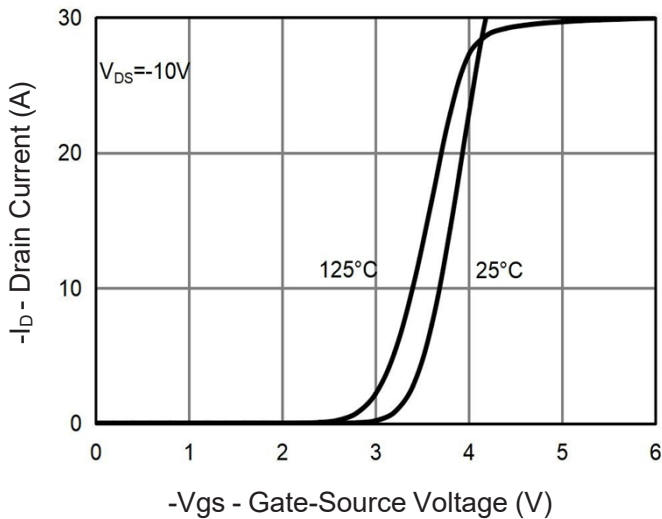
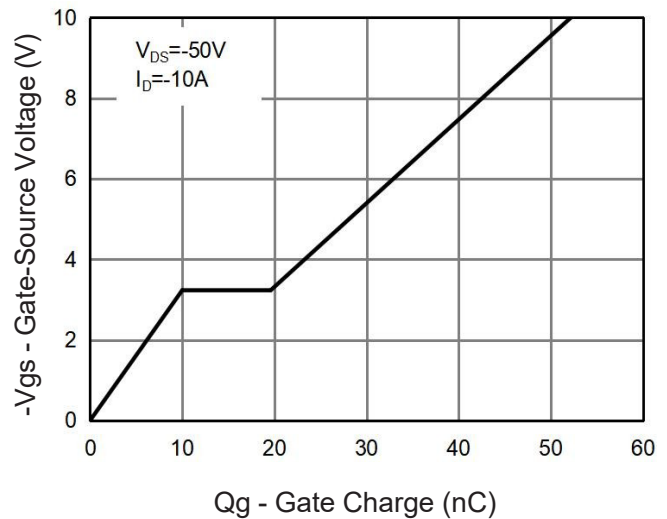
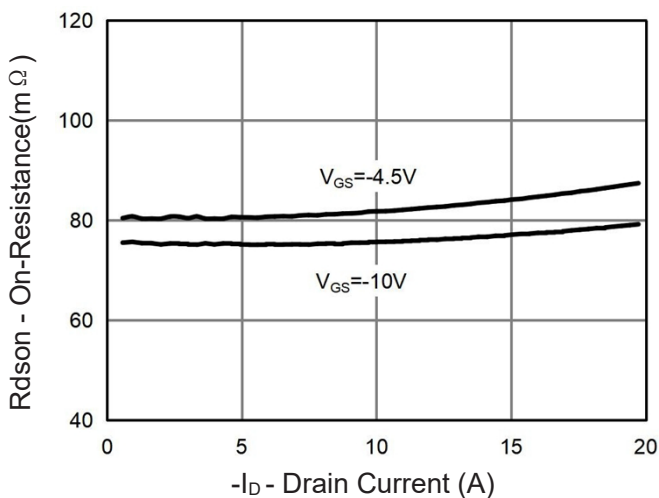
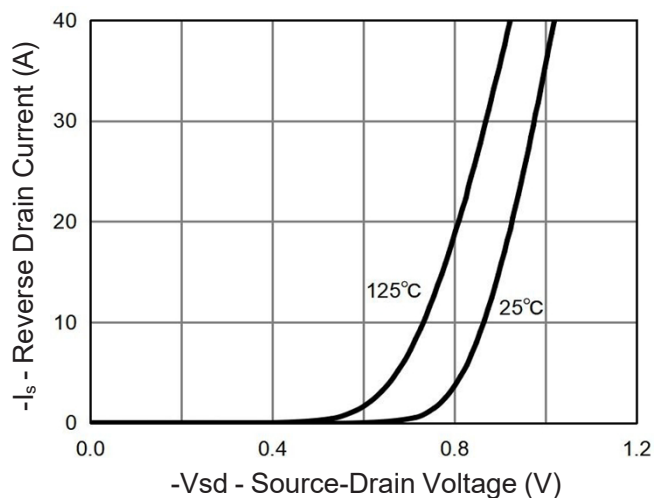
2) Gate Charge Test Circuit

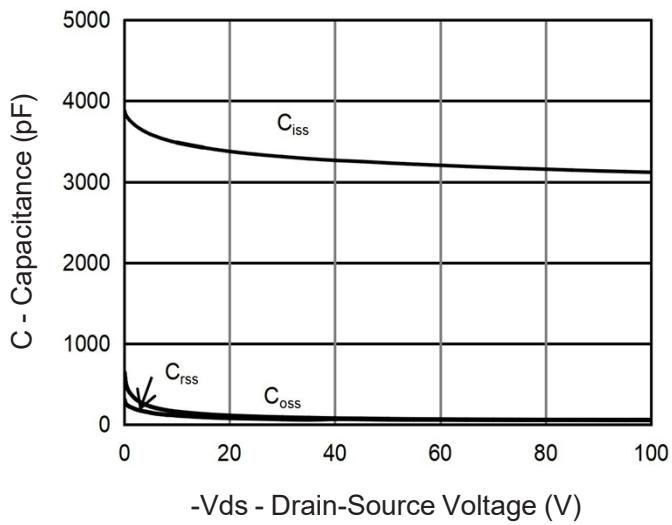
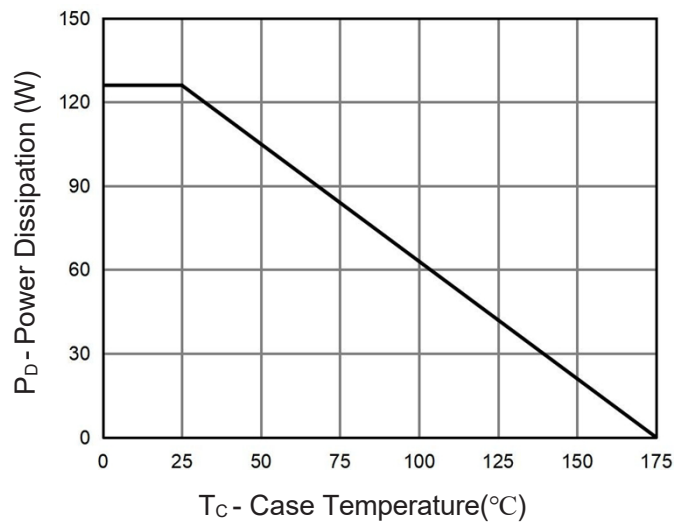
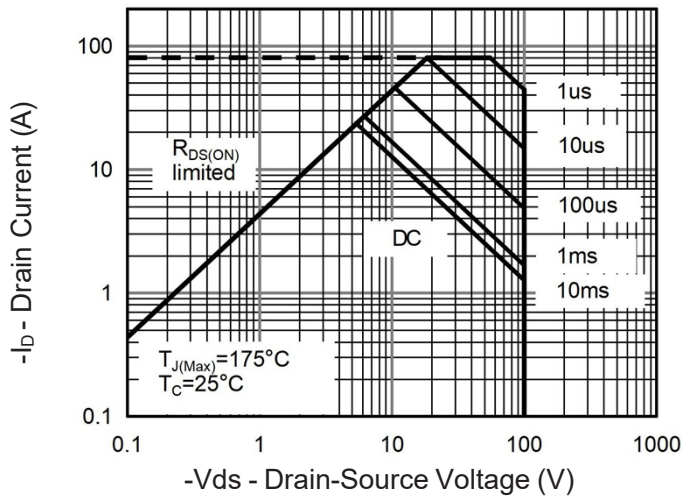
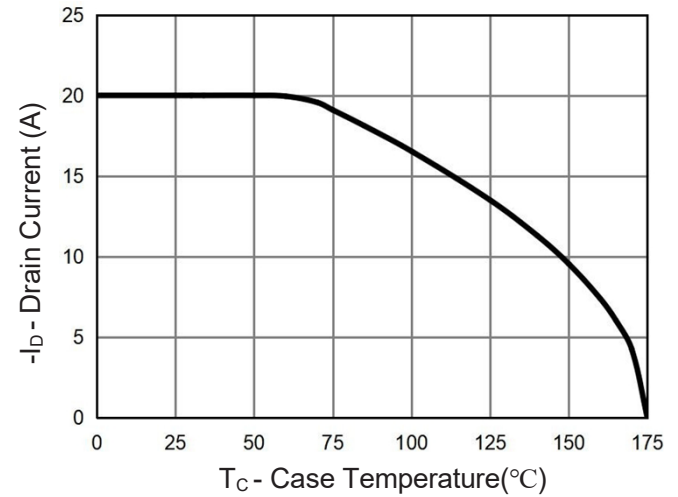
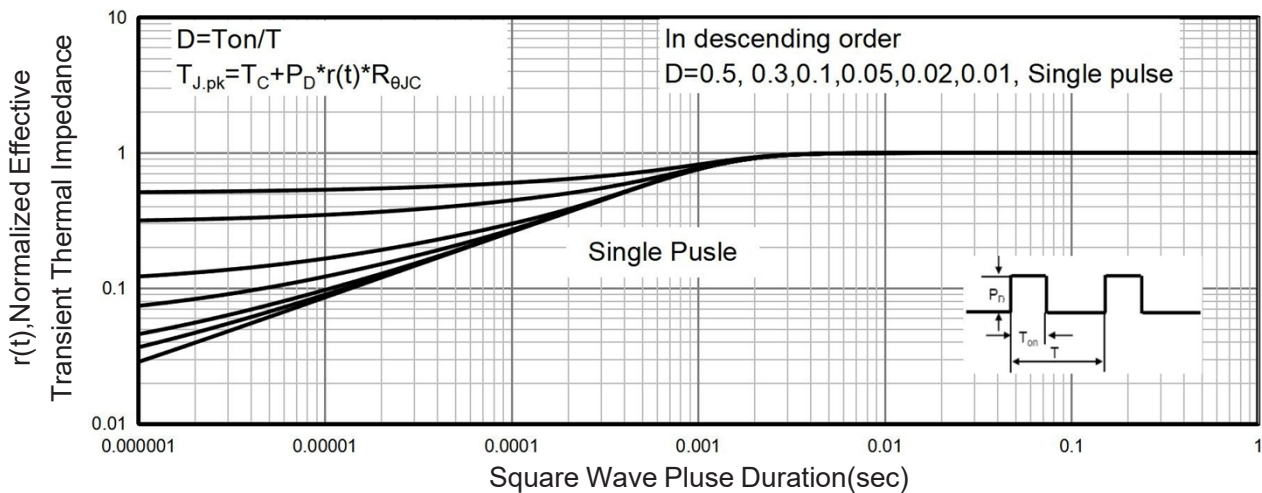


3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)


Figure 1 Output Characteristics

Figure 4 R_{DS(on)} vs Junction Temperature

Figure 2 Transfer Characteristics

Figure 5 Gate Charge

Figure 3 R_{DS(on)} vs Drain Current

Figure 6 Source-Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 Power De-rating

Figure 8 Safe Operation Area (Note 4)

Figure 10 Drain Current De-rating

Figure 11 Normalized Maximum Transient Thermal Impedance