

Description

The VSM30P05 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

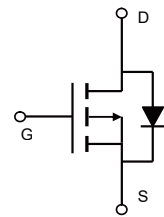
- $V_{DS} = -55V, I_D = -30A$
 $R_{DS(ON)} < 40m\Omega @ V_{GS} = -10V$
- High density cell design for ultra low $R_{ds(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



TO-252



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM30P05	VSM30P05-T2	TO-252	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-55	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-30	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	-21	A
Pulsed Drain Current	I_{DM}	110	A
Maximum Power Dissipation	P_D	65	W
Derating factor		0.43	W/ $^\circ C$
Single pulse avalanche energy (Note 5)	E_{AS}	420	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	2.3	$^\circ C/W$
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Electrical Characteristics ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

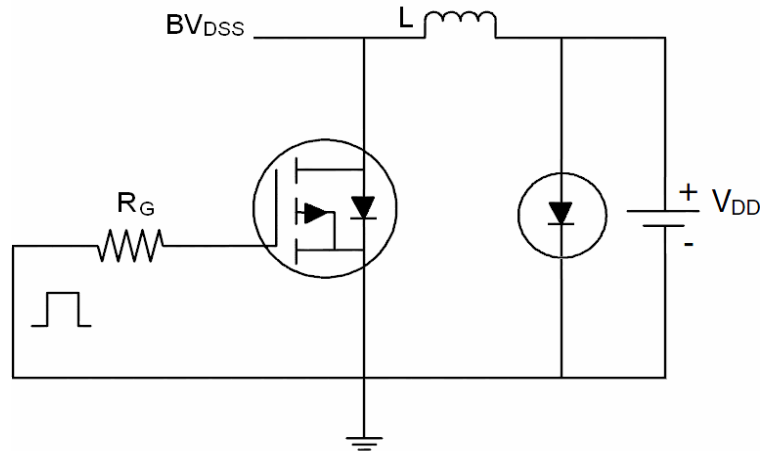
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =-250μA	-55	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-55V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =-250μA	-2	-2.6	-4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-15A	-	30	40	mΩ
Forward Transconductance	g _{FS}	V _{DS} =-25V,I _D =-16A	8	-	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{ISS}	V _{DS} =-30V,V _{GS} =0V, F=1.0MHz	-	3500	-	PF
Output Capacitance	C _{OSS}		-	240	-	PF
Reverse Transfer Capacitance	C _{RSS}		-	153	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-30V,I _D =-15A V _{GS} =-10V,R _{GEN} =3Ω	-	12	-	nS
Turn-on Rise Time	t _r		-	15	-	nS
Turn-Off Delay Time	t _{d(off)}		-	38	-	nS
Turn-Off Fall Time	t _f		-	15	-	nS
Total Gate Charge	Q _g	V _{DS} =-30V,I _D =-15A, V _{GS} =-10V	-	56	-	nC
Gate-Source Charge	Q _{gs}		-	11	-	nC
Gate-Drain Charge	Q _{gd}		-	24	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V,I _S =-15A	-	-	1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	-30	A
Reverse Recovery Time	t _{rr}	TJ = 25°C, IF = -15A	-	-	71	nS
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs ^(Note3)	-	-	170	nC

Notes:

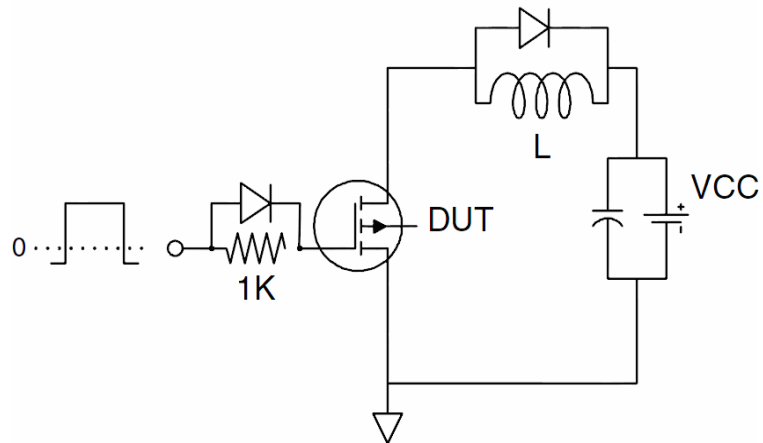
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. E_{AS} condition: $T_J=25^{\circ}\text{C}, V_{DD}=-25V, V_G=-20V, L=0.5mH, R_g=25\Omega, I_{AS}=29A$

Test Circuit

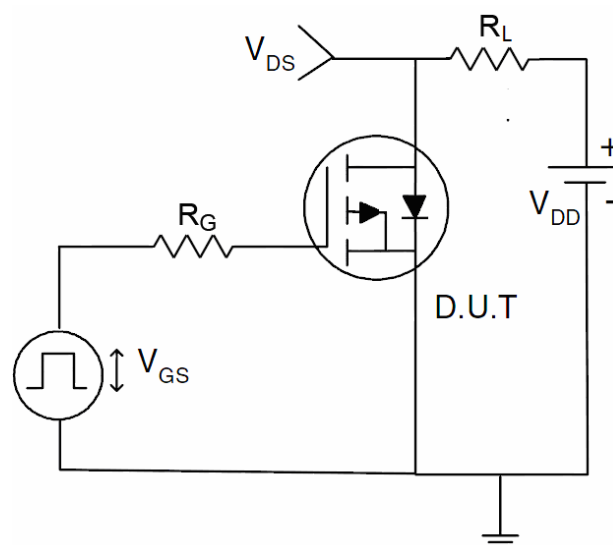
1) E_{AS} Test Circuit



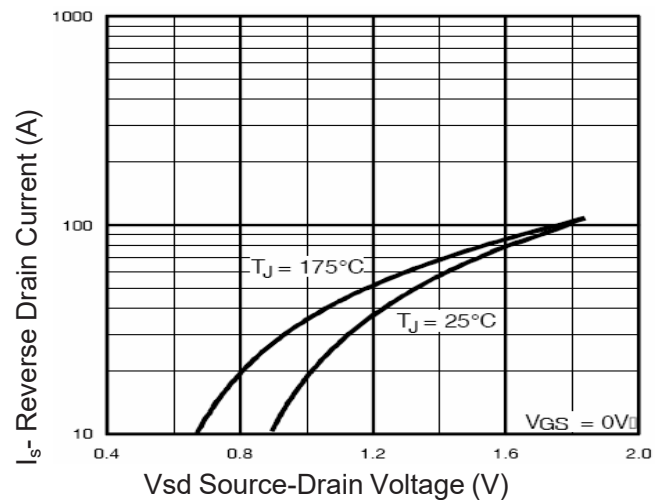
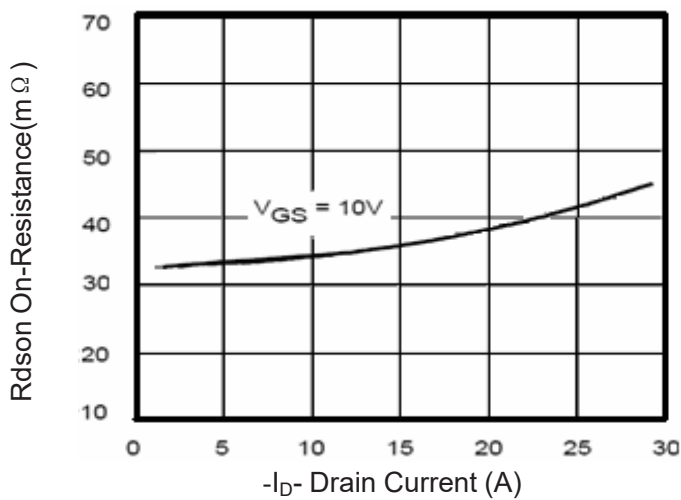
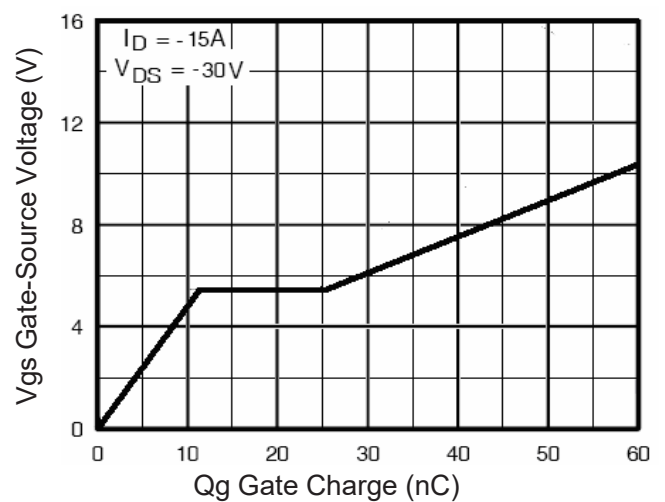
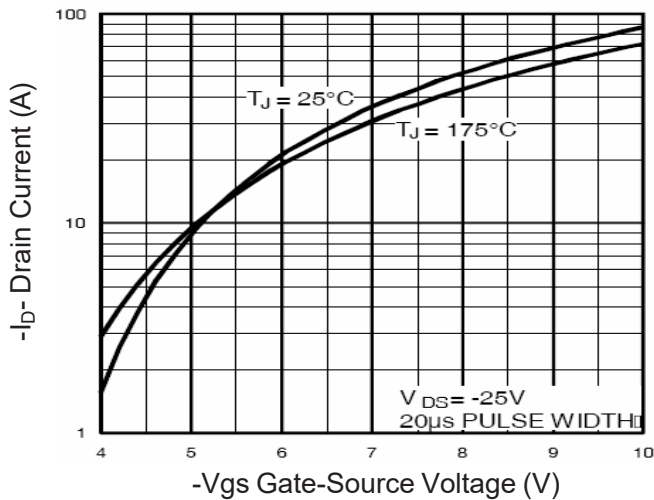
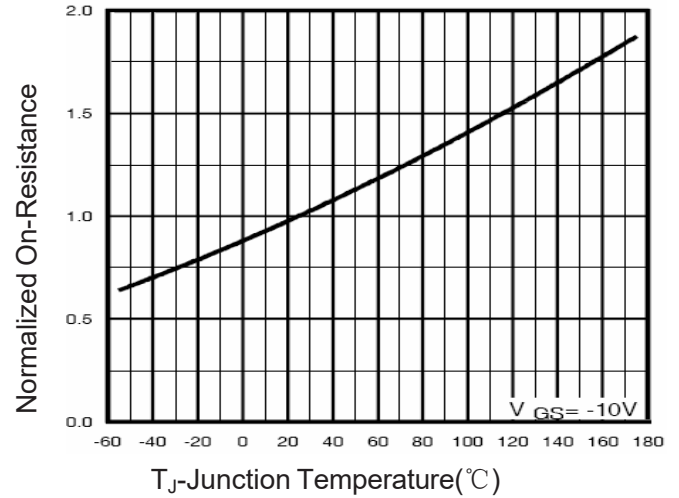
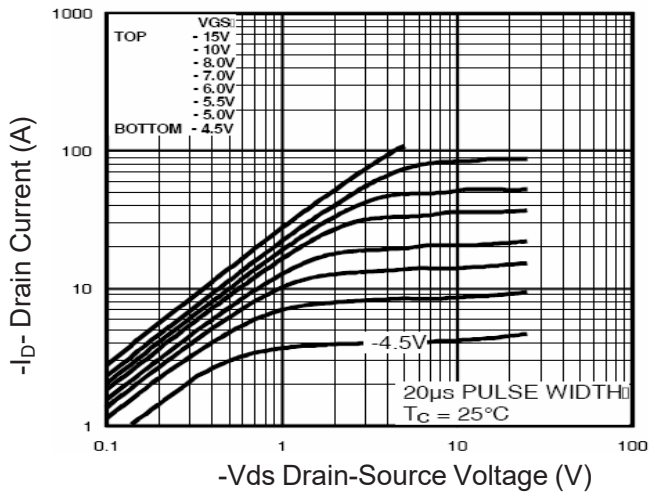
2) Gate Charge Test Circuit

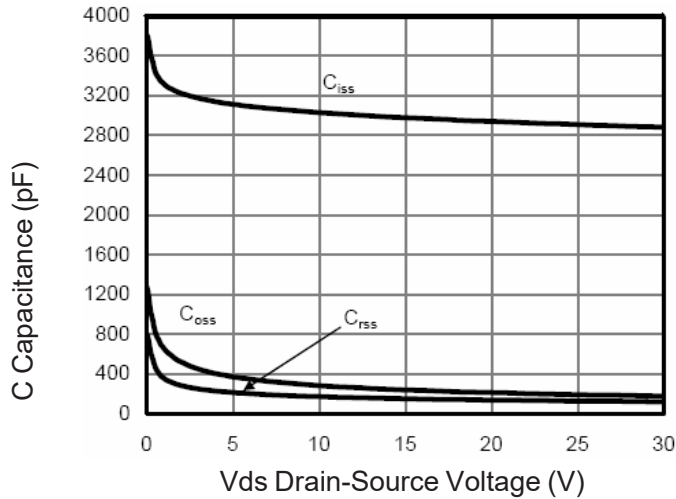
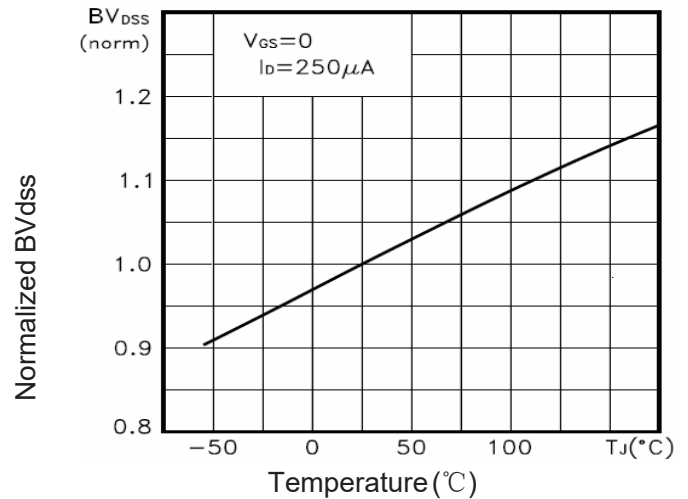
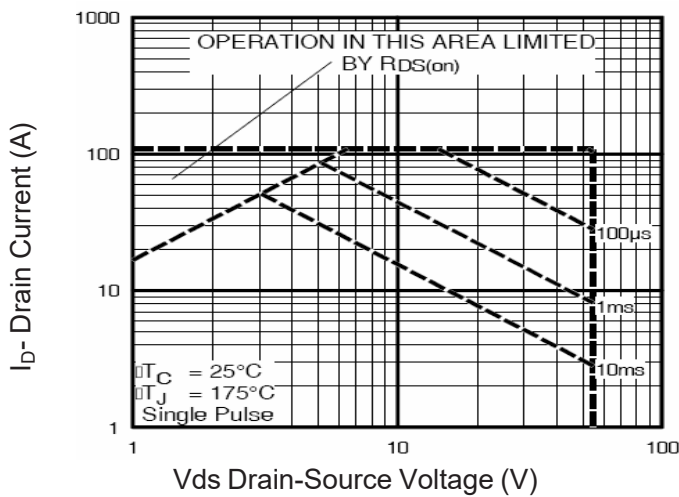
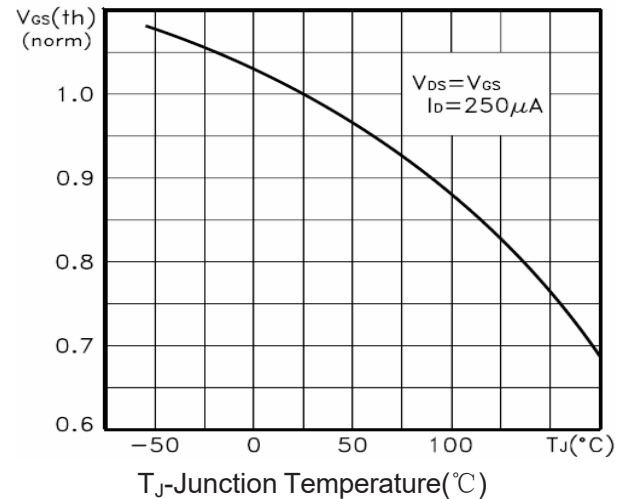
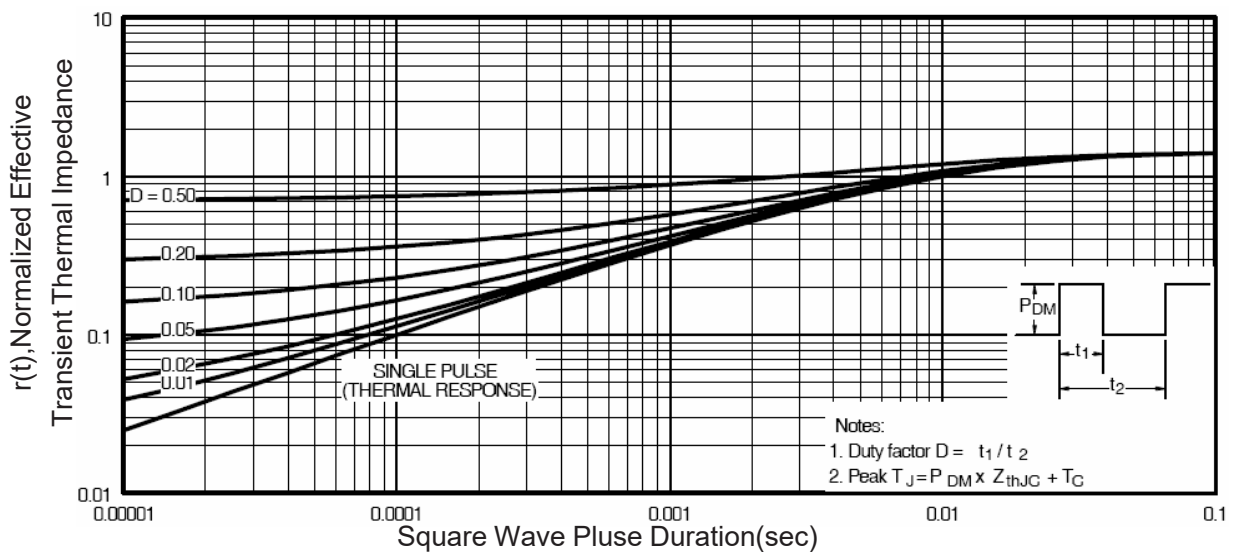


3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)




Figure 7 Capacitance vs Vds

Figure 9 BV_{DSS} vs Junction Temperature

Figure 8 Safe Operation Area

Figure 10 V_{GS(th)} vs Junction Temperature

Figure 11 Normalized Maximum Transient Thermal Impedance