

Description

The VSM20P20 uses advanced trench technology and design to provide excellent $R_{DS(on)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

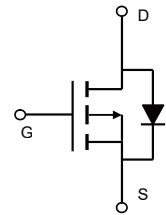
- $V_{DS} = -200V, I_D = -20A$
 $R_{DS(on)} < 215m\Omega @ V_{GS} = -10V$
 $R_{DS(on)} < 230m\Omega @ V_{GS} = -4.5V$
- High density cell design for ultra low $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Portable equipment and battery powered systems



TO-263



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM20P20	VSM20P20-T3	TO-263	Ø330mm	24mm	800units

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-200	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-20	A
Drain Current-Continuous($100^\circ C$)	$I_D(100^\circ C)$	-15	A
Pulsed Drain Current ($T_C = 25^\circ C$)	I_{DM}	-80	A
Maximum Power Dissipation	P_D	192	W
Derating factor		1.282	W/ $^\circ C$
Single pulse avalanche energy ^(Note 1)	E_{AS}	282	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.78	$^\circ C/W$
Thermal Resistance, Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	40	$^\circ C/W$

Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

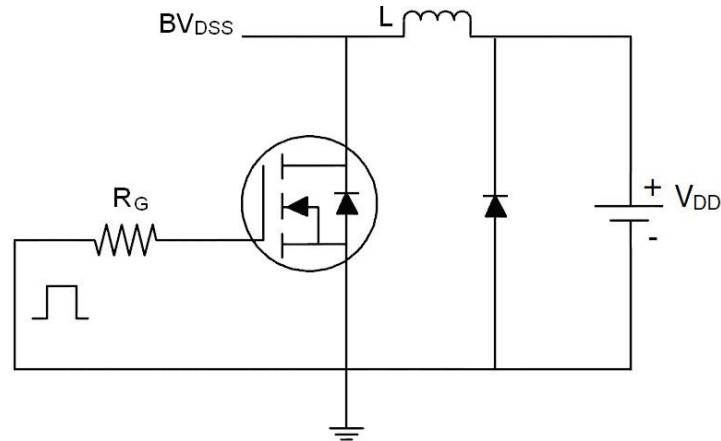
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-200	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-200V, V_{GS}=0V$	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.3	-1.8	-2.3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-15A$	-	190	215	m Ω
		$V_{GS}=-4.5V, I_D=-10A$	-	200	230	
Forward Transconductance	g_{FS}	$V_{DS}=-10V, I_D=-20A$	-	50	-	S
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{DS}=-100V, V_{GS}=0V,$ $F=1.0MHz$	-	6596	-	pF
Output Capacitance	C_{oss}		-	82	-	pF
Reverse Transfer Capacitance	C_{rss}		-	59	-	pF
Switching Characteristics (Note 3)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-100V, I_D=-20A,$ $V_{GS}=-10V, R_{GEN}=5\Omega$	-	17	-	nS
Turn-on Rise Time	t_r		-	80	-	nS
Turn-off Delay Time	$t_{d(off)}$		-	45	-	nS
Turn-off Fall Time	t_f		-	65	-	nS
Total Gate Charge	Q_g	$V_{DS}=-100V, I_D=-20A,$ $V_{GS}=-10V$	-	122	-	nC
Gate-Source Charge	Q_{gs}		-	19	-	nC
Gate-Drain Charge	Q_{gd}		-	22	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=-20A$	-	-	-1.2	V
Diode Forward Current	I_S		-	-	-20	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}C, I_F = 20A$ $di/dt = -100A/\mu s$	-	90	-	nS
Reverse Recovery Charge	Q_{rr}		-	145	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

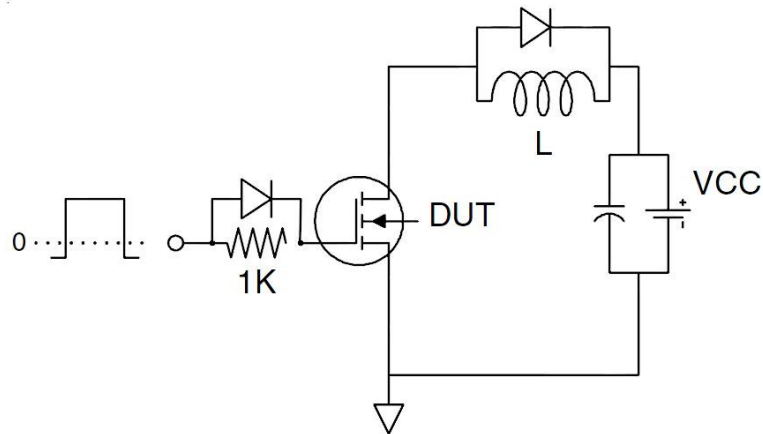
1. EAS condition : $T_J=25^{\circ}\text{C}, V_{DD}=-100V, V_G=-10V, L=0.5mH, R_g=25\Omega$.
2. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The maximum allowed junction temperature of 175°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.
3. Guaranteed by design, not subject to production.
4. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=175^{\circ}\text{C}$. The SOA curve provides a single pulse rating.

Test Circuit

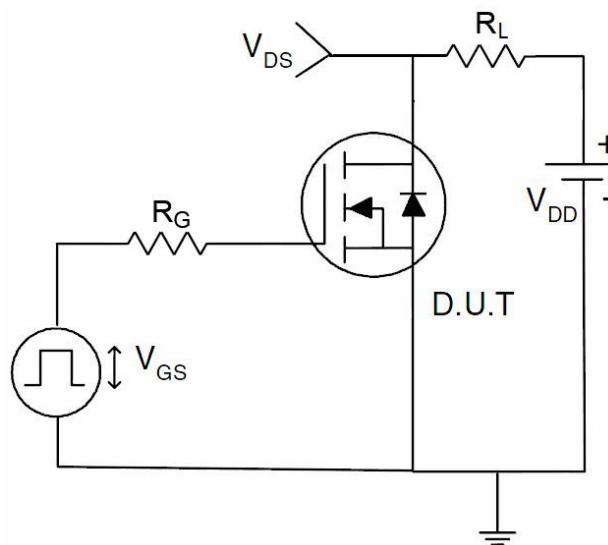
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

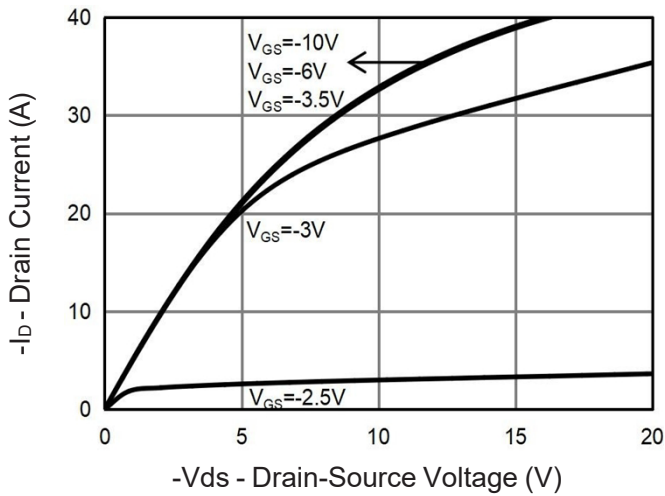


Figure 1 Output Characteristics

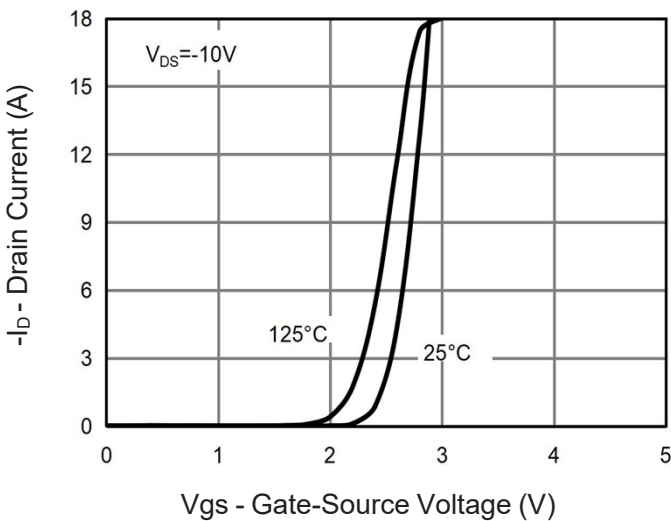


Figure 2 Transfer Characteristics

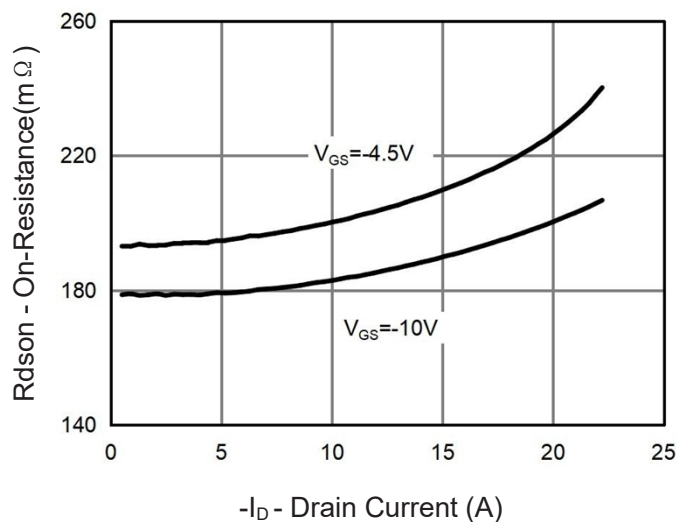


Figure 3 $R_{DS(on)}$ vs Drain Current

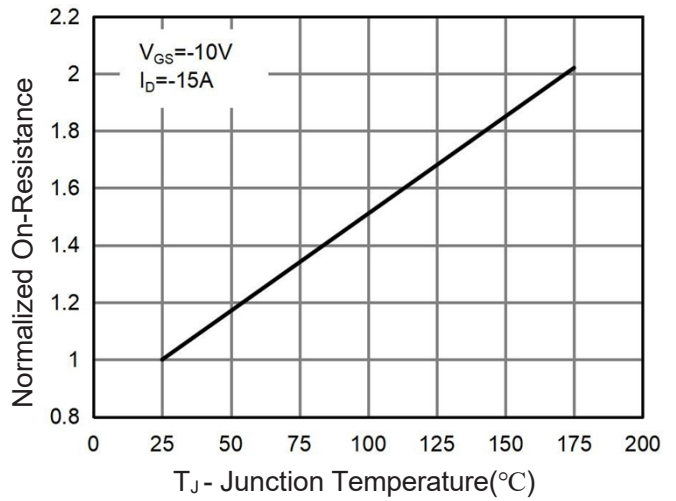


Figure 4 $R_{DS(on)}$ vs Junction Temperature

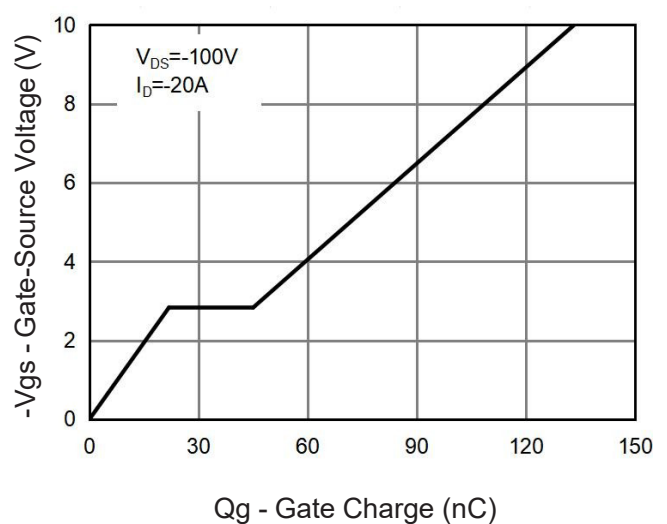


Figure 5 Gate Charge

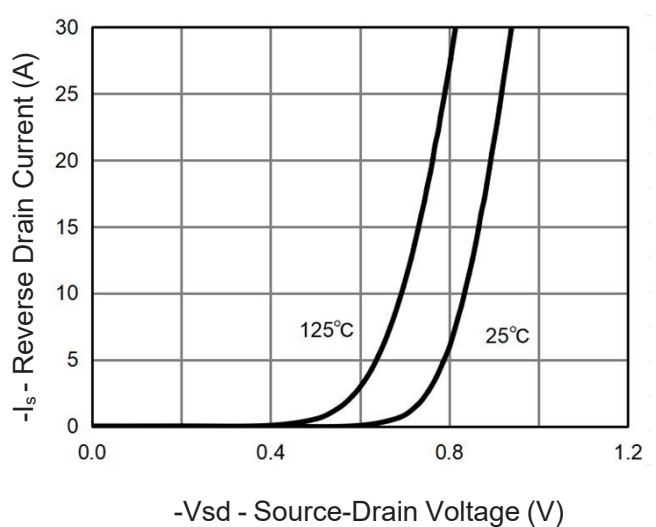
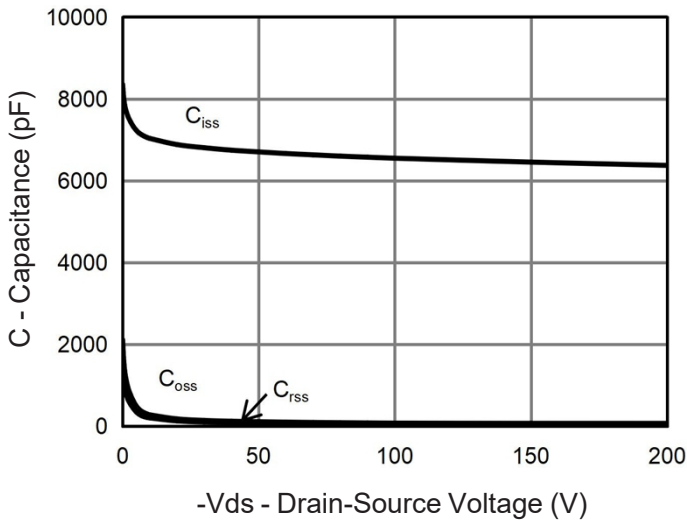
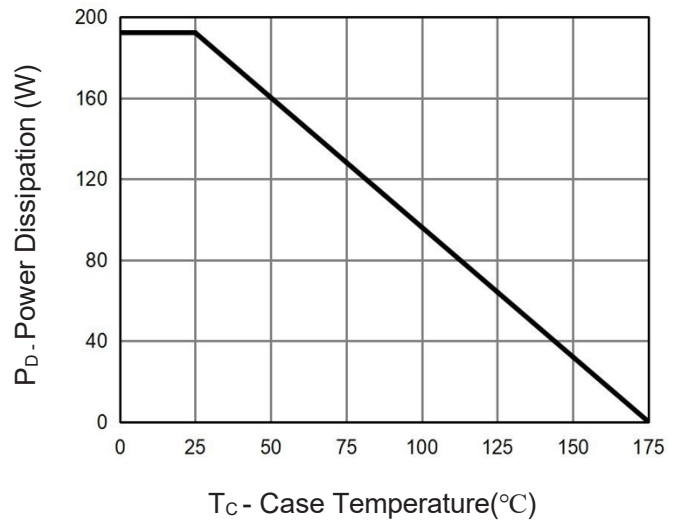
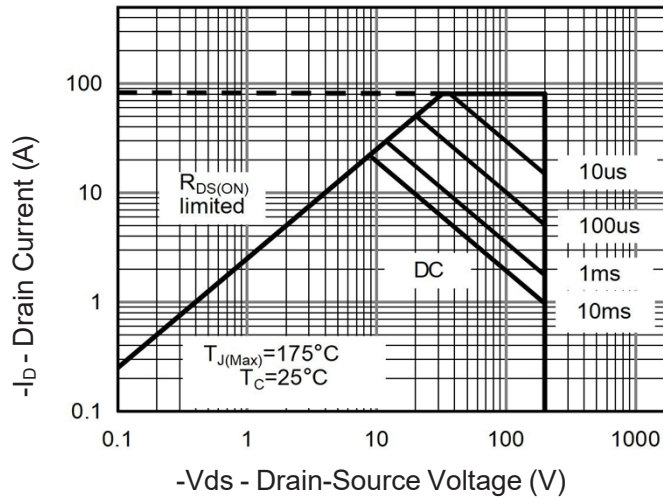
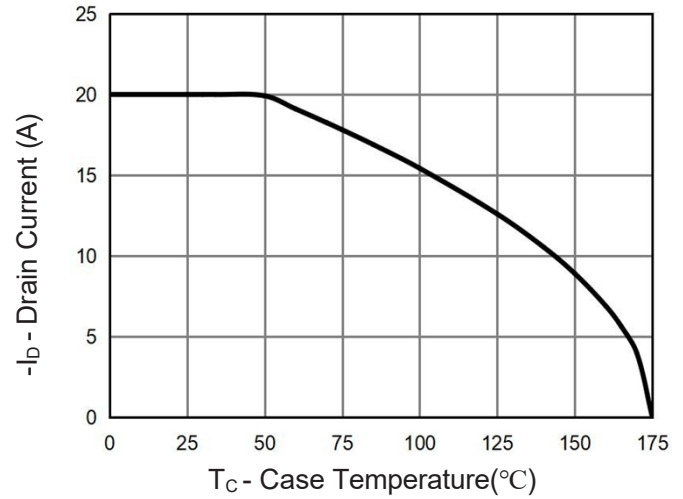
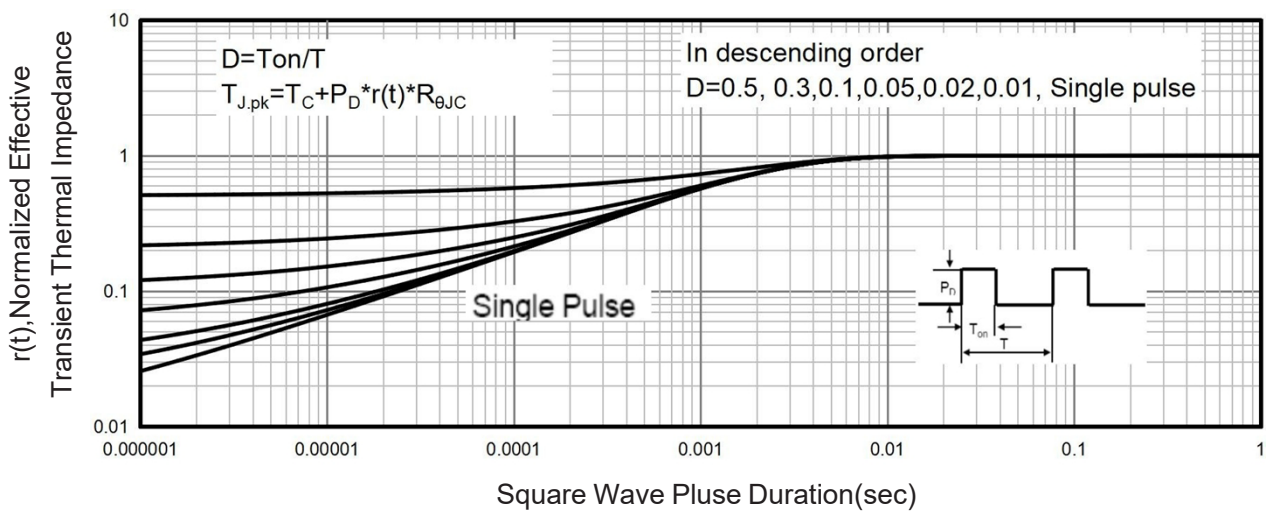


Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 Power De-rating

Figure 8 Safe Operation Area (Note 4)

Figure 10 Drain Current De-rating

Figure 11 Normalized Maximum Transient Thermal Impedance