Description

The VSM35P10 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

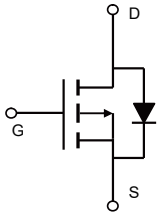
General Features

- V_{DS} =-100V,I_D =-35A
  $R_{DS(ON)}$ <40mΩ @ V_{GS}=-10V (Typ:30mΩ)
  $R_{DS(ON)}$ <45mΩ @ V_{GS}=-4.5V (Typ:32mΩ)
- Super high dense cell design
- Advanced trench process technology
- Reliable and rugged
- High density cell design for ultra low On-Resistance

Application

- Portable equipment and battery powered systems

TO-263



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM35P10	VSM35P10-T3	TO-263	Ø330mm	23mm	800units

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-100	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	-35	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	-24.7	A
Pulsed Drain Current	I_{DM}	-140	A
Maximum Power Dissipation	P_D	110	W
Single pulse avalanche energy (Note 1)	E_{AS}	368	mJ
Derating factor		0.735	W/℃
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case	$R_{\theta JC}$	1.36	℃/W

Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	40	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

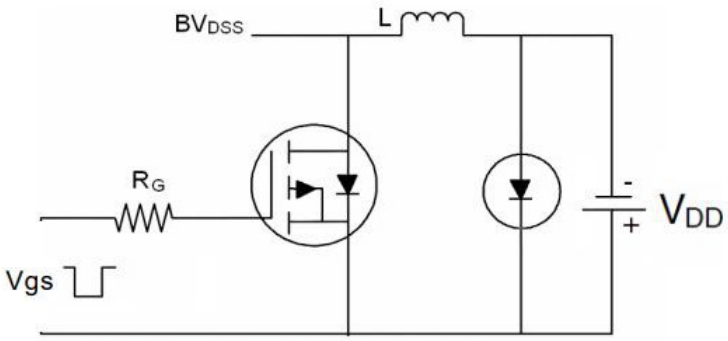
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-100V,V_{GS}=0V	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-1.5	-1.8	-2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-20A	-	30	40	mΩ
		V_{GS}=-4.5V, I_D=-20A	-	32	45	mΩ
Forward Transconductance	g_{FS}	V_{DS}=-10V,I_D=-20A	-	50	-	S
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=-50V,V_{GS}=0V, F=1.0MHz	-	5720	-	pF
Output Capacitance	C_{oss}		-	190	-	pF
Reverse Transfer Capacitance	C_{rss}		-	128	-	pF
Switching Characteristics (Note 3)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-50V,I_D=-20A V_{GS}=-10V,R_{GEN}=9.1Ω	-	17	-	nS
Turn-on Rise Time	t_r		-	80	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	45	-	nS
Turn-Off Fall Time	t_f		-	65	-	nS
Total Gate Charge	Q_g	V_{DS}=-50V,I_D=-20A, V_{GS}=-10V	-	118	-	nC
Gate-Source Charge	Q_{gs}		-	19.8	-	nC
Gate-Drain Charge	Q_{gd}		-	22.2	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=-20A	-	-	-1.2	V
Diode Forward Current	I_S	-	-	-	-35	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF =-20A di/dt = 100A/μs	-	90	-	nS
Reverse Recovery Charge	Qrr		-	145	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

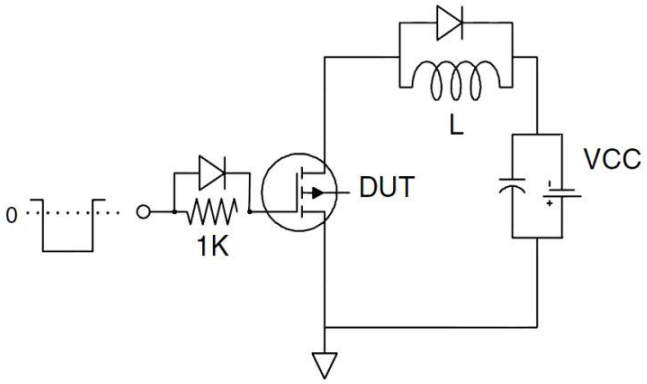
1. EAS condition : Tj=25℃,V_{DD}=-50V,V_G=15V,L=0.5mH,Rg=25Ω.
2. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The maximum allowed junction temperature of 175°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.
3. Guaranteed by design, not subject to production.
4. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C. The SOA curve provides a single pulse rating.

Test Circuit

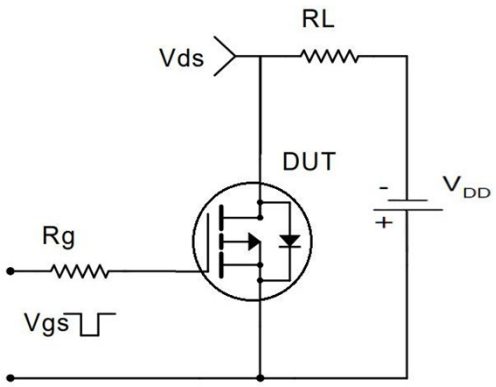
1） E_{AS} test Circuit



2） Gate charge test Circuit



3） Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

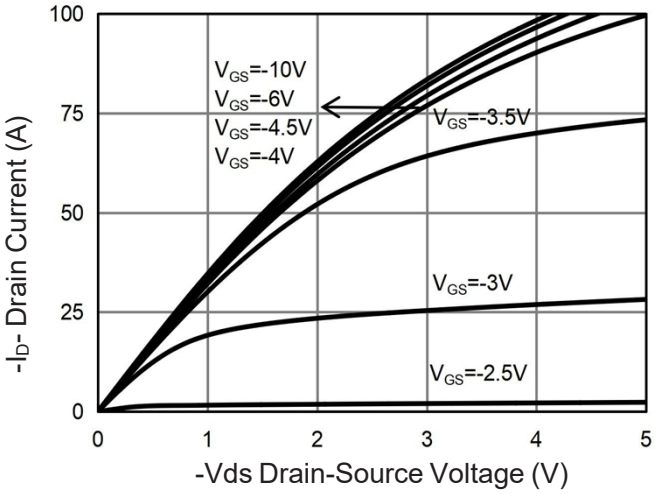


Figure 1 Output Characteristics

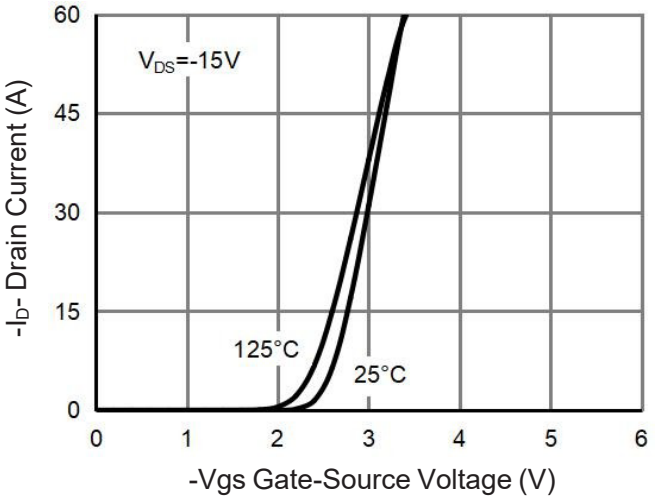


Figure 2 Transfer Characteristics

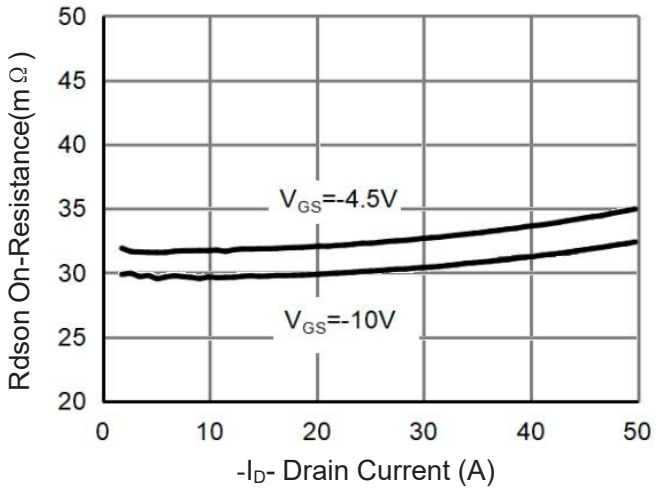


Figure 3 Rdson- Drain Current

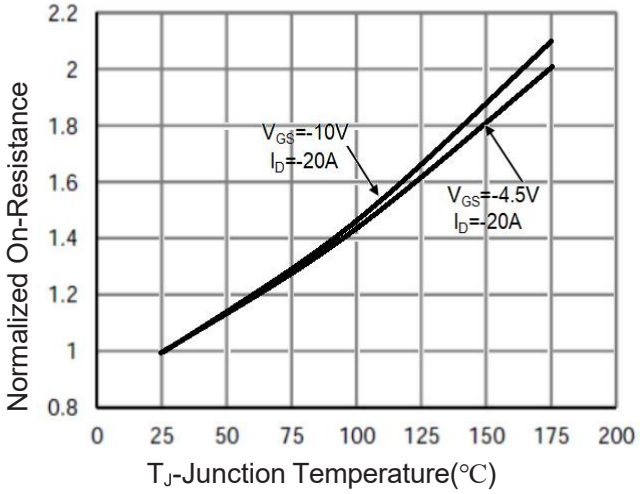


Figure 4 Rdson-JunctionTemperature

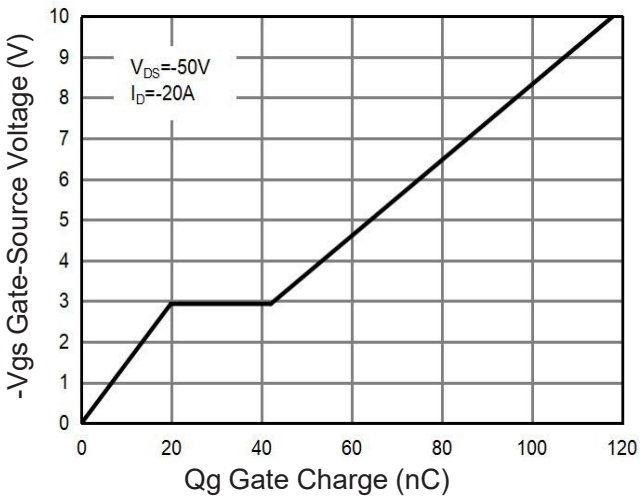


Figure 5 Gate Charge

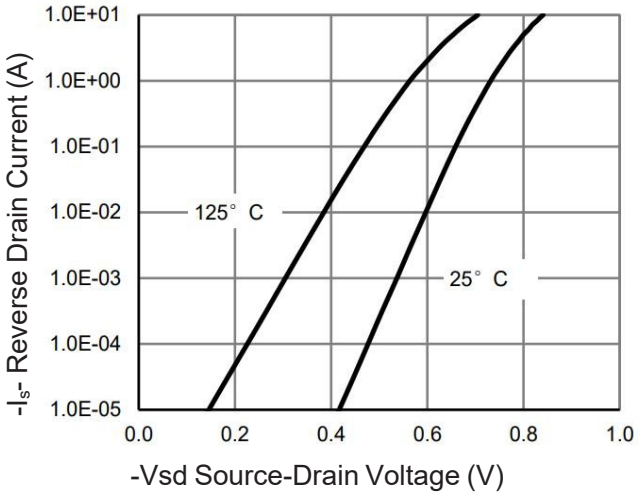


Figure 6 Source- Drain Diode Forward

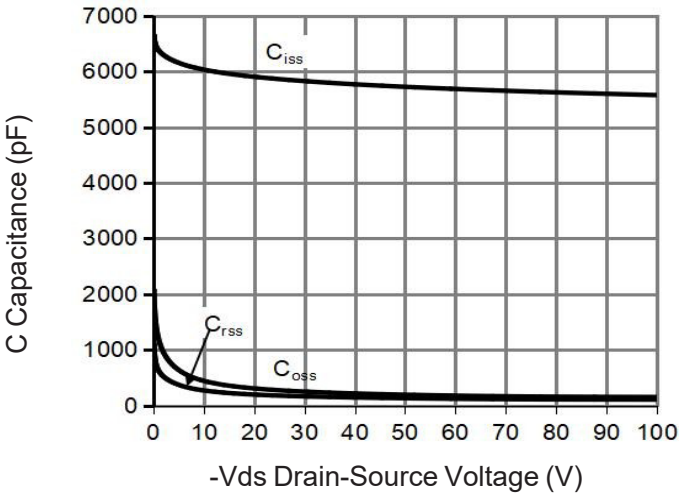


Figure 7 Capacitance vs Vds

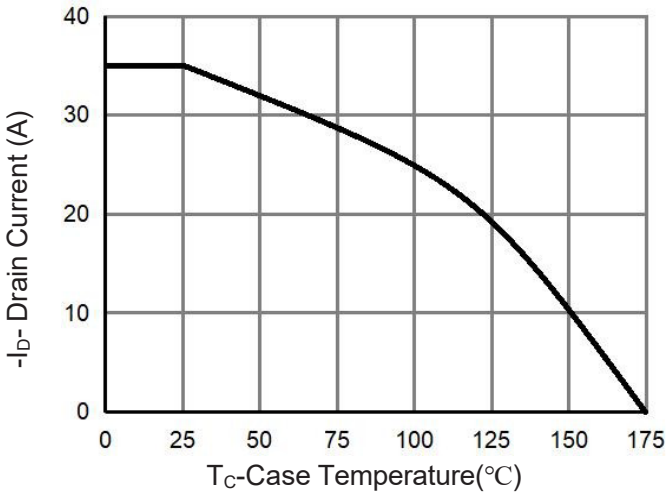


Figure 9 Drain Current De-rating

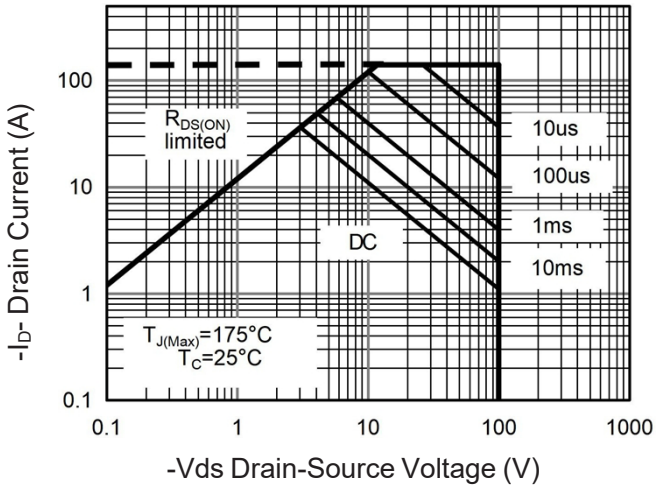


Figure 8 Safe Operation Area (Note 4)

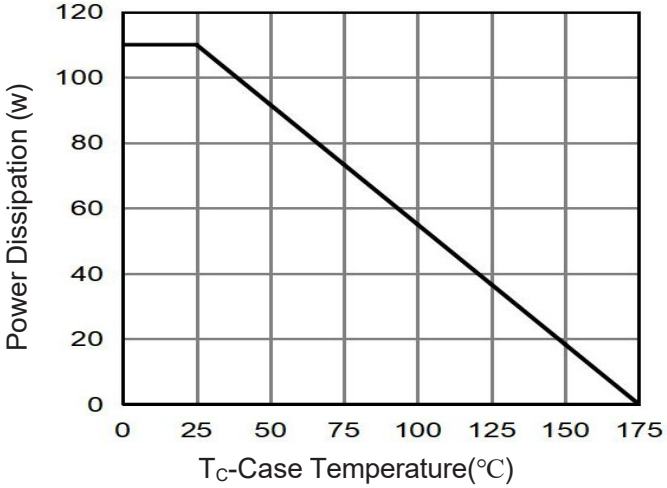


Figure 10 Power De-rating

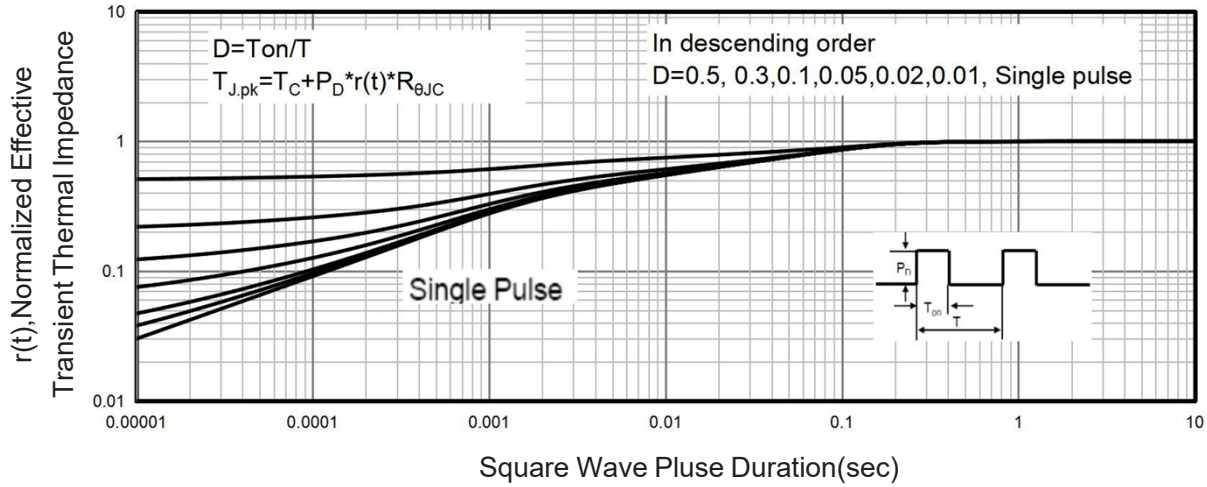


Figure 11 Normalized Maximum Transient Thermal Impedance