

Description

The VSM20N03 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

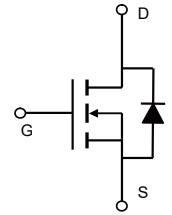
- $V_{DS}=30V, I_D=20A$
 $R_{DS(ON)} < 8m\Omega @ V_{GS}=10V$
 $R_{DS(ON)} < 12m\Omega @ V_{GS}=4.5V$
- High density cell design for ultra low $R_{DS(ON)}$
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply



DFN3x3



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM20N03	VSM20N03-D33	DFN3x3	-	-	-

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	20	A
Drain Current-Continuous($T_C=100^{\circ}C$)	$I_D(100^{\circ}C)$	14.1	A
Pulsed Drain Current	I_{DM}	80	A
Maximum Power Dissipation	P_D	20	W
Derating factor		0.27	W/ $^{\circ}C$
Single pulse avalanche energy (Note 5)	E_{AS}	72	mJ
V_{DS} Spike (Note 6)	10 μs	36	V
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^{\circ}C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	6.25	$^{\circ}C/W$
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Electrical Characteristics (T_c=25°C unless otherwise noted)

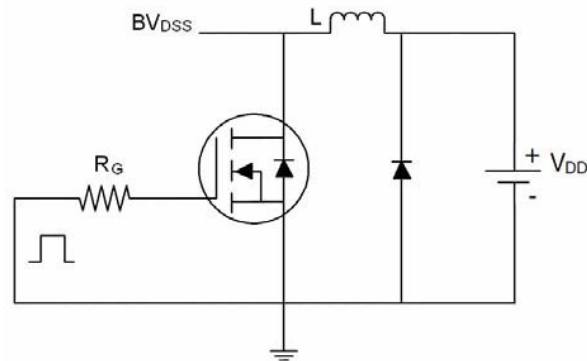
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0	1.5	2.2	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =10A	-	6.8	8	mΩ
		V _{GS} =4.5V, I _D =10A	-	8.8	12	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =10A	26	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, F=1.0MHz	-	1000	-	PF
Output Capacitance	C _{oss}		-	180.8	-	PF
Reverse Transfer Capacitance	C _{rss}		-	164.4	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =15V, R _L =0.75Ω V _{GS} =10V, R _G =3Ω	-	5	-	nS
Turn-on Rise Time	t _r		-	12	-	nS
Turn-Off Delay Time	t _{d(off)}		-	19	-	nS
Turn-Off Fall Time	t _f		-	6	-	nS
Total Gate Charge	Q _g	V _{DS} =15V, I _D =10A, V _{GS} =10V	-	17		nC
Gate-Source Charge	Q _{gs}		-	2.8		nC
Gate-Drain Charge	Q _{gd}		-	3.9		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =10A	-		1.2	V
Diode Forward Current (Note 2)	I _S		-	-	20	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F =10A di/dt = 100A/μs(Note3)	-	19	-	nS
Reverse Recovery Charge	Q _{rr}		-	10	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

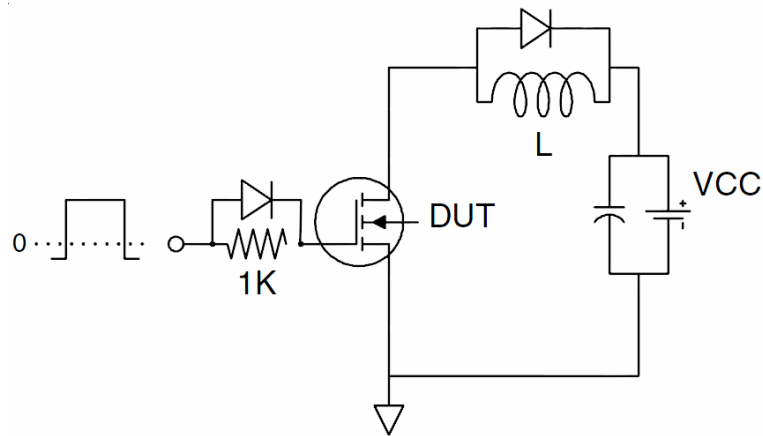
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition: T_J=25°C, V_{DD}=15V, V_G=10V, L=0.5mH, R_G=25Ω
6. The spike duty cycle 5% max, limited by junction temperature T_J(MAX)=125° C

Test circuit

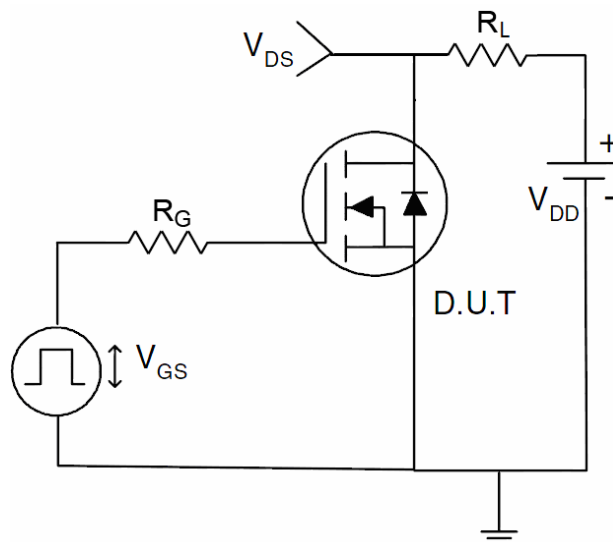
1) E_{AS} test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:



Typical Electrical and Thermal Characteristics (Curves)

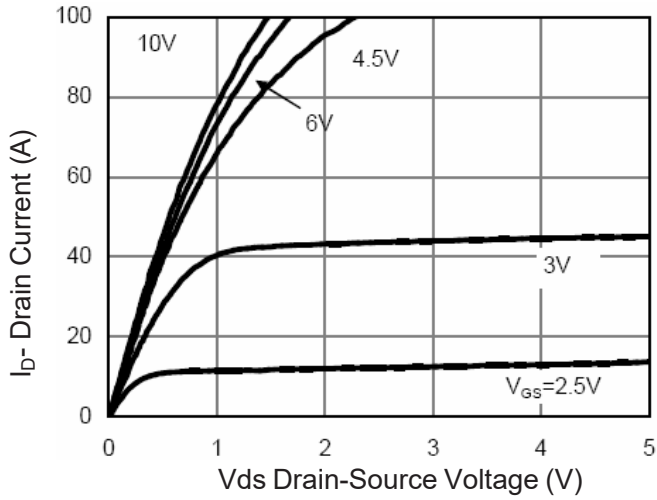


Figure 1 Output Characteristics

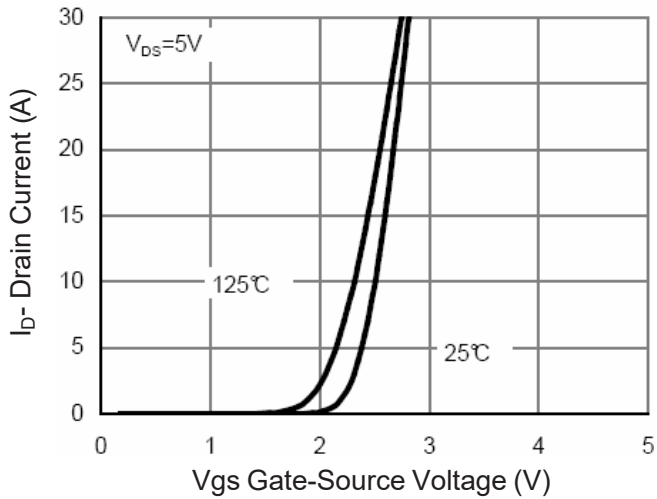


Figure 2 Transfer Characteristics

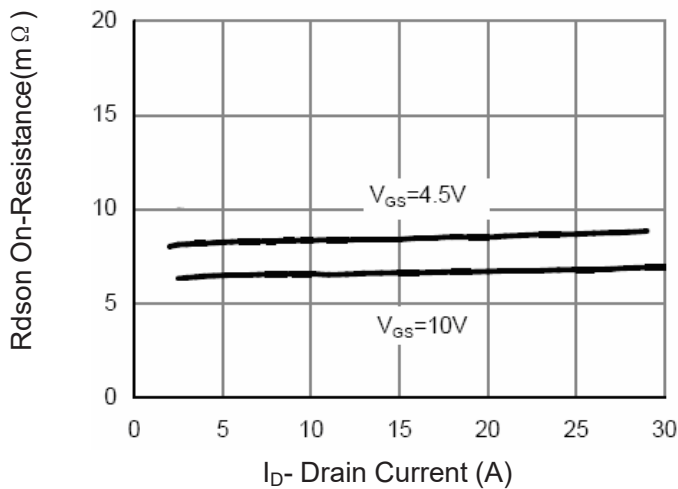


Figure 3 Rdson- Drain Current

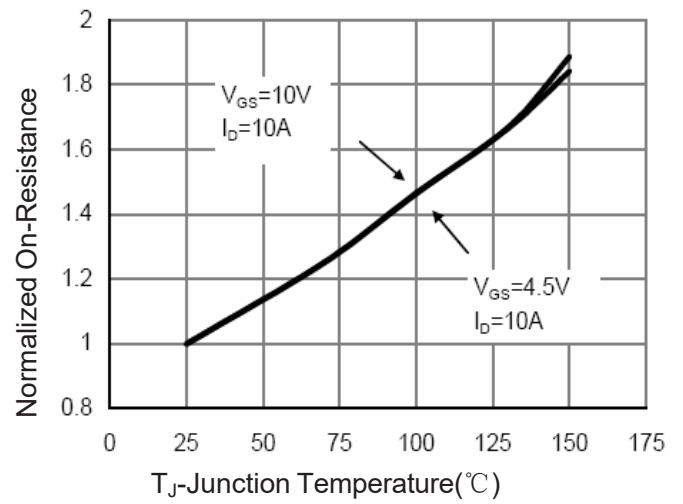


Figure 4 Rdson-Junction Temperature

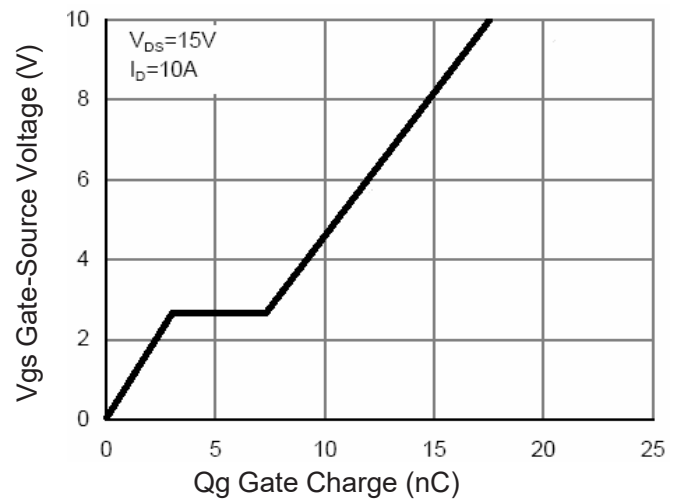


Figure 5 Gate Charge

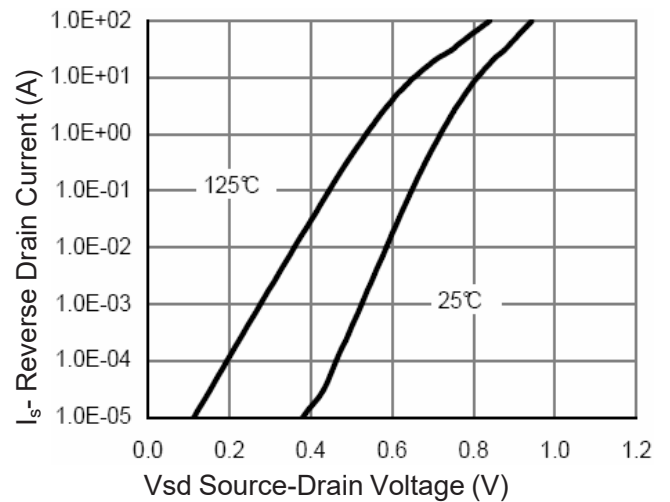
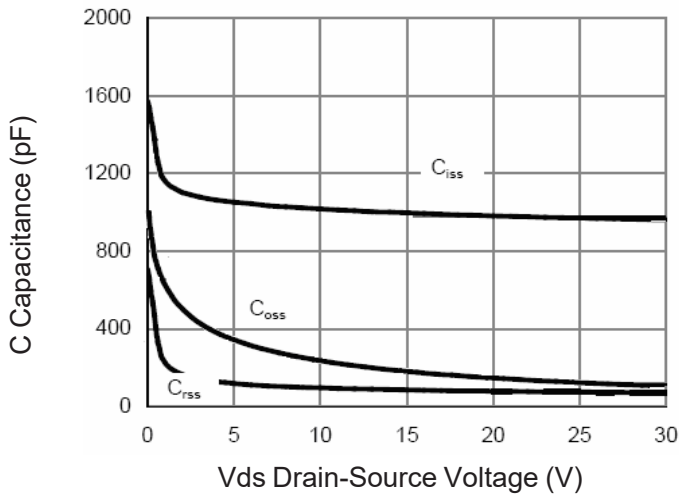
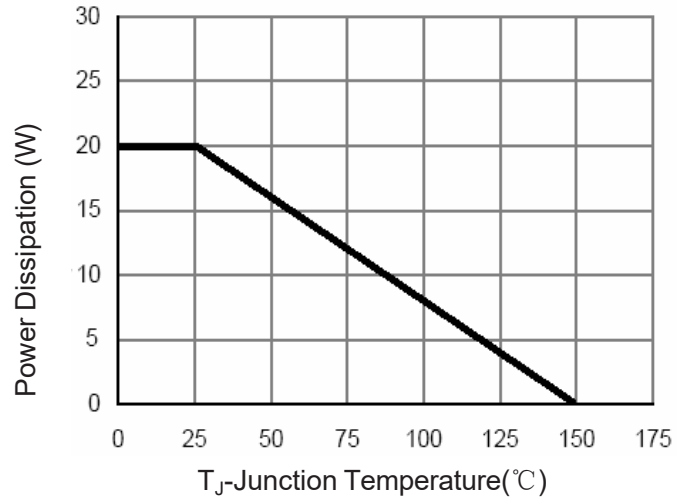
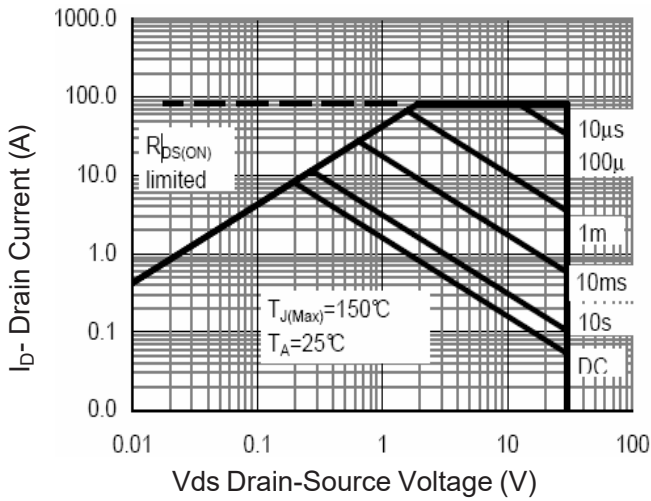
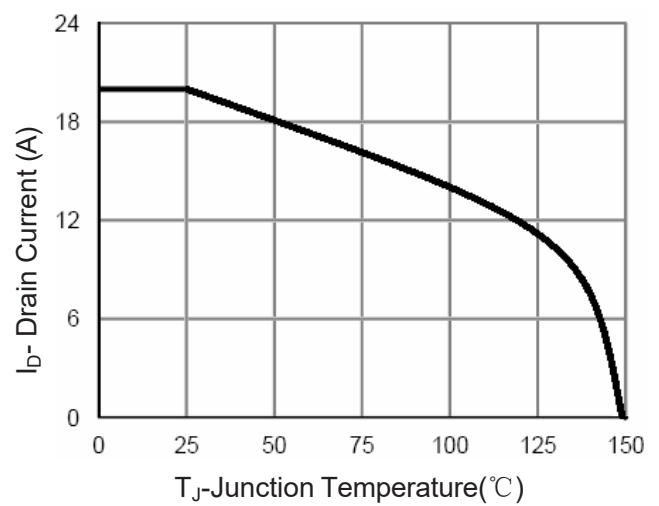
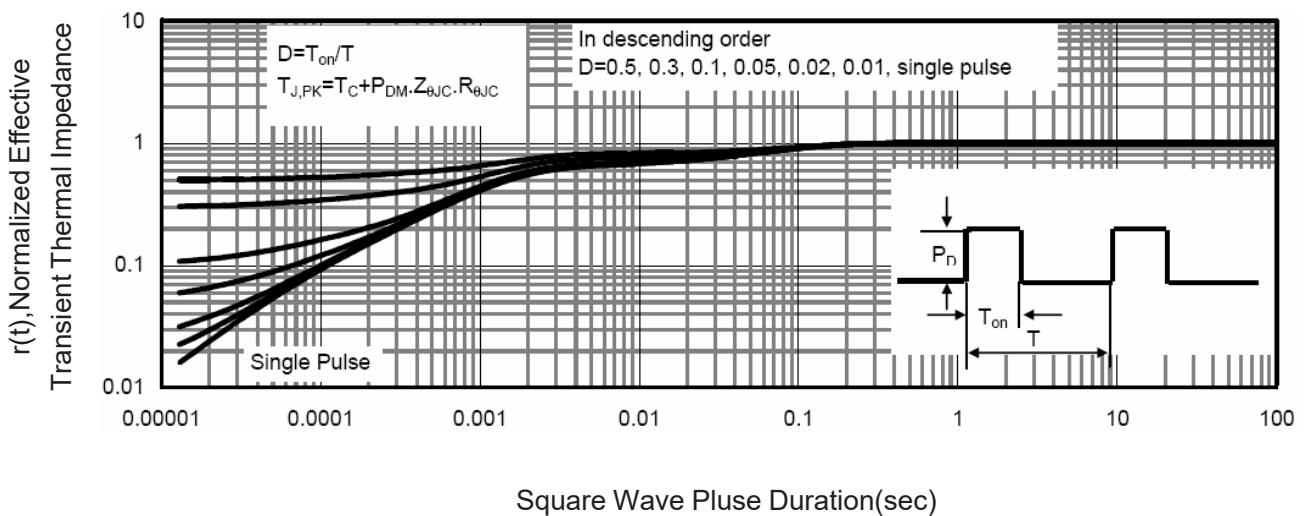


Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 Power De-rating

Figure 8 Safe Operation Area

Figure 10 I_D Current De-rating

Figure 11 Normalized Maximum Transient Thermal Impedance