

Description

The VSM115N03 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

Application

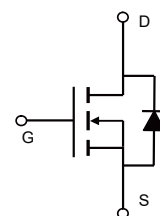
- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

General Features

- $V_{DS} = 30V, I_D = 115A$
 $R_{DS(ON)} = 2.2m\Omega$ (typical) @ $V_{GS} = 10V$
 $R_{DS(ON)} = 3.6m\Omega$ (typical) @ $V_{GS} = 4.5V$
- High density cell design for ultra low $R_{DS(on)}$
- Very low on-resistance $R_{DS(on)}$
- Good stability and uniformity with high E_{AS}
- 150 °C operating temperature
- Pb-free lead plating



DFN5x6



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM115N03	VSM115N03-D56	DFN5x6	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	115	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	81	A
Pulsed Drain Current ^(Note 1)	I_{DM}	460	A
Maximum Power Dissipation	P_D	70	W
Derating factor		0.56	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	384	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	1.79	$^\circ C/W$
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Electrical Characteristics (TC=25°C unless otherwise noted)

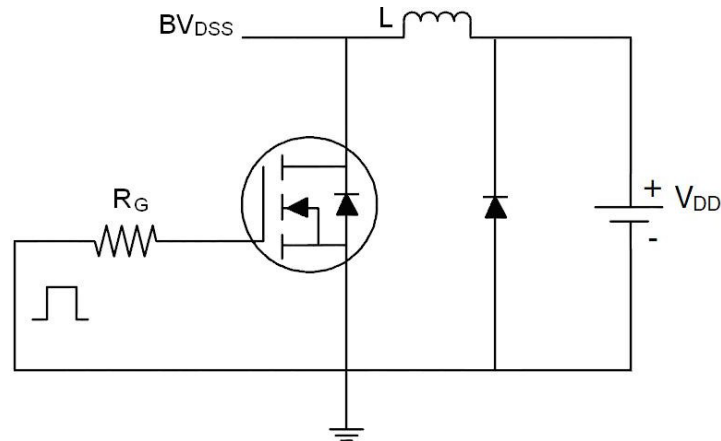
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1	1.5	2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	2.2	2.9	mΩ
		V _{GS} =4.5V, I _D =20A	-	3.6	5.2	
Forward Transconductance	g _{FS}	V _{DS} =10V, I _D =20A	-	50	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, F=1.0MHz	-	3120	-	PF
Output Capacitance	C _{oss}		-	445	-	PF
Reverse Transfer Capacitance	C _{rss}		-	421	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =15V, I _D =20A V _{GS} =10V, R _{GEN} =6Ω	-	11	-	nS
Turn-on Rise Time	t _r		-	16	-	nS
Turn-Off Delay Time	t _{d(off)}		-	38	-	nS
Turn-Off Fall Time	t _f		-	7	-	nS
Total Gate Charge	Q _g	V _{DS} =15V, I _D =20A, V _{GS} =10V	-	71	-	nC
Gate-Source Charge	Q _{gs}		-	10.4	-	nC
Gate-Drain Charge	Q _{gd}		-	16.2	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =20A	-	-	1.2	V
Diode Forward Current (Note 2)	I _S		-	-	115	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 20A di/dt = 100A/μs ^(Note3)	-	30	-	nS
Reverse Recovery Charge	Q _{rr}		-	60	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

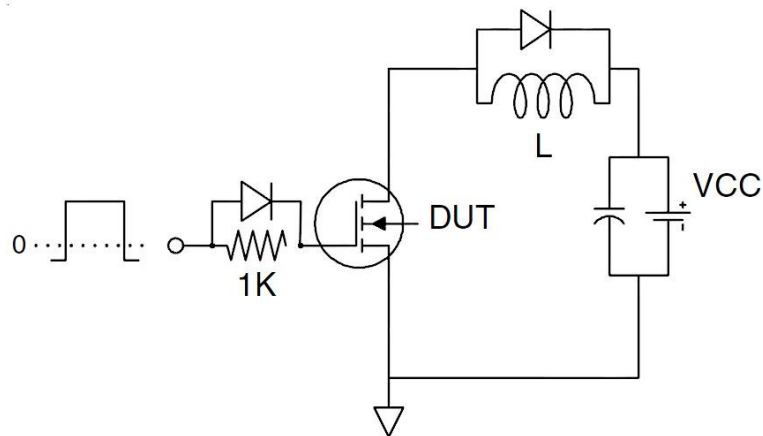
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^\circ C, V_{DD}=15V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test Circuit

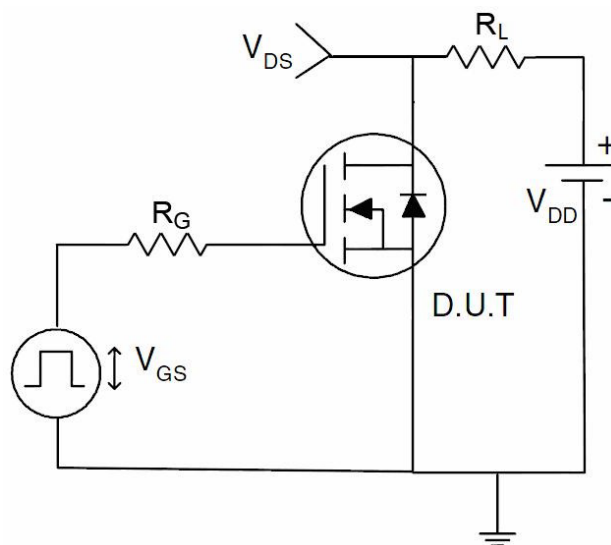
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

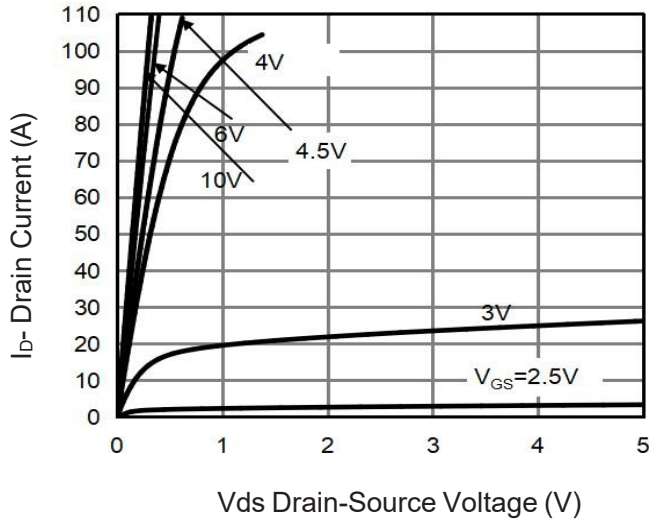


Figure 1 Output Characteristics

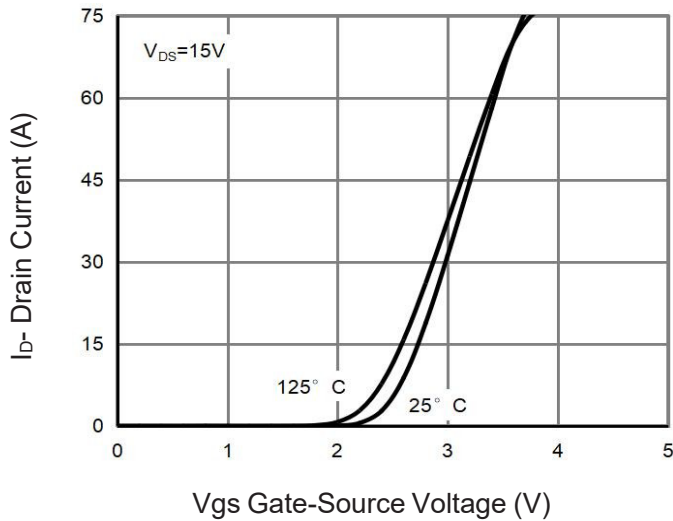


Figure 2 Transfer Characteristics

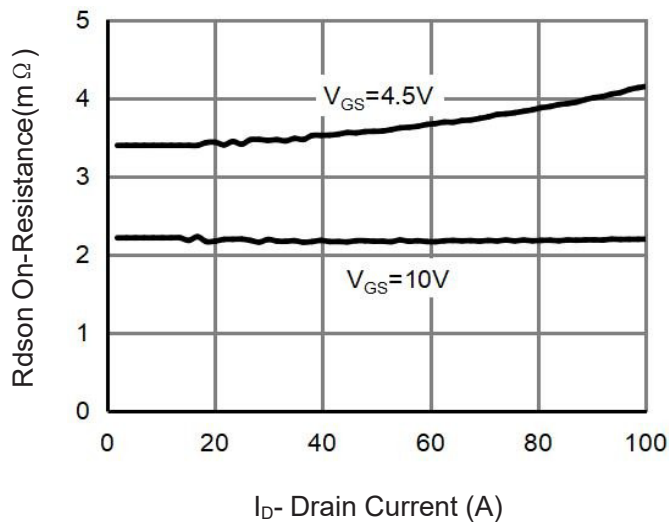


Figure 3 Rdson- Drain Current

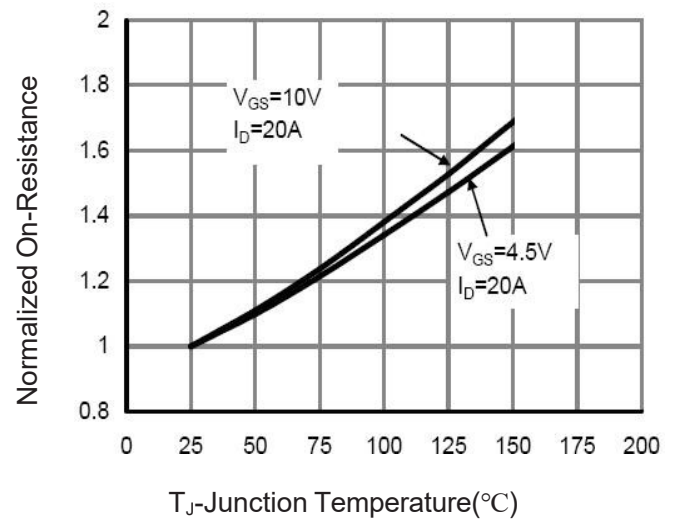


Figure 4 Rdson-Junction Temperature

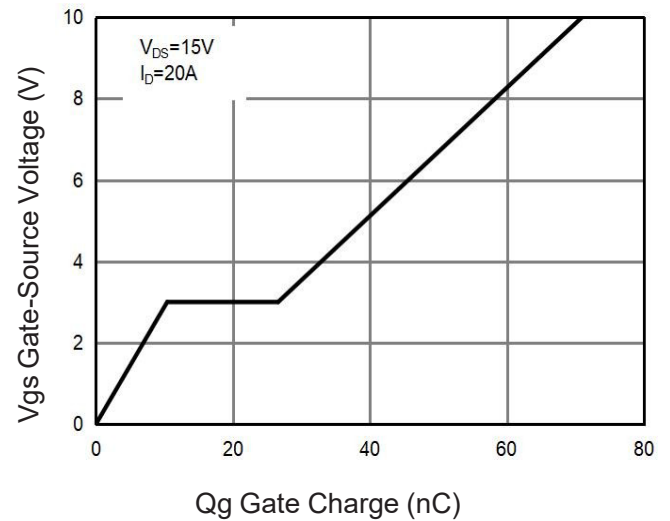


Figure 5 Gate Charge

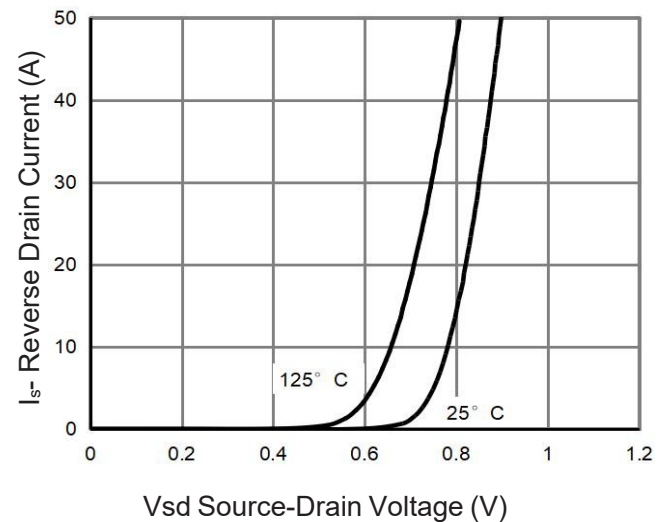
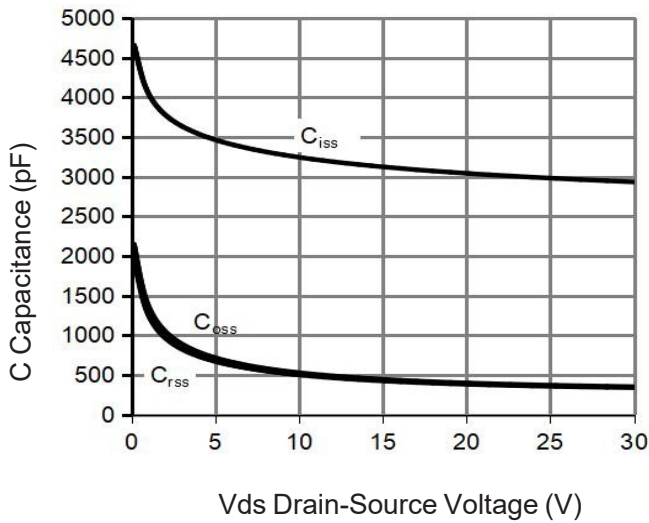
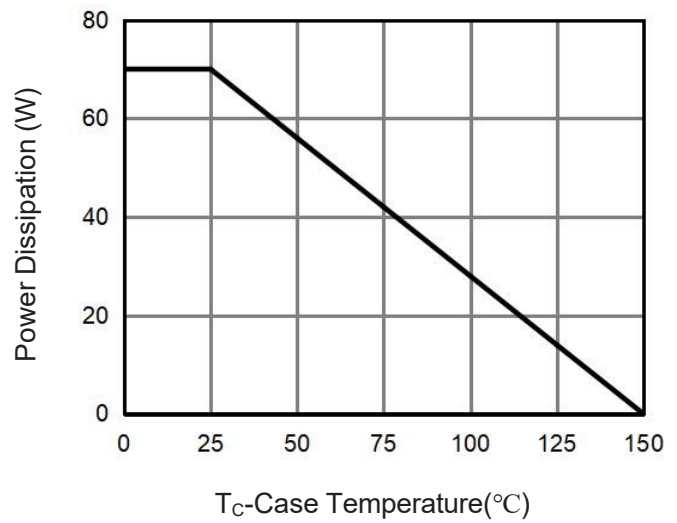


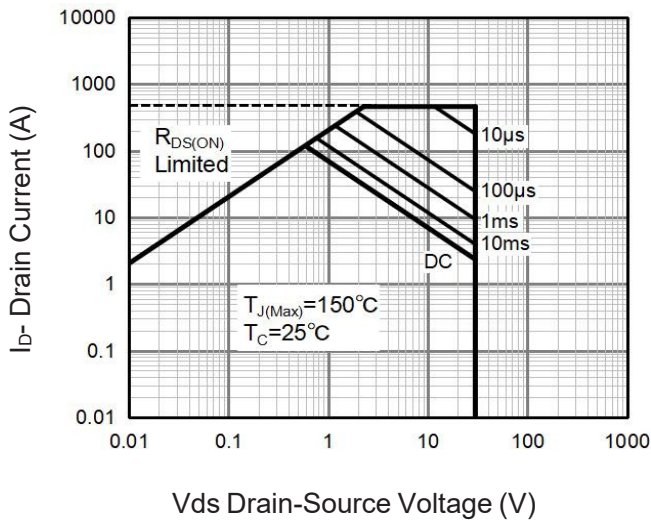
Figure 6 Source- Drain Diode Forward



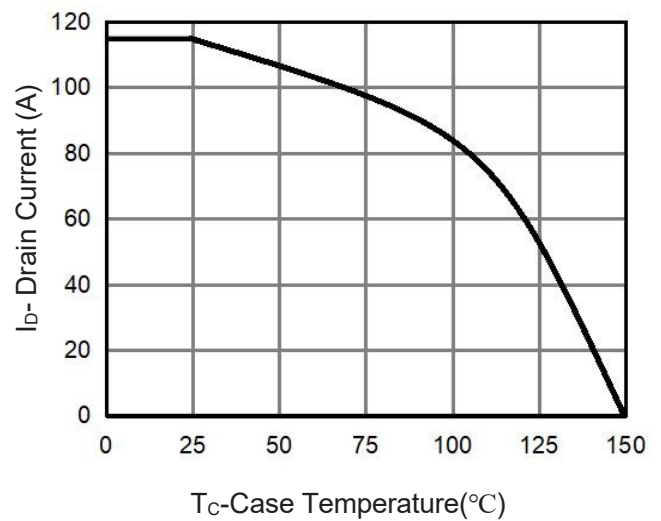
Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



T_C -Case Temperature($^{\circ}C$)
Figure 9 Power De-rating



Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area



T_C -Case Temperature($^{\circ}C$)
Figure10 ID Current- Junction Temperature

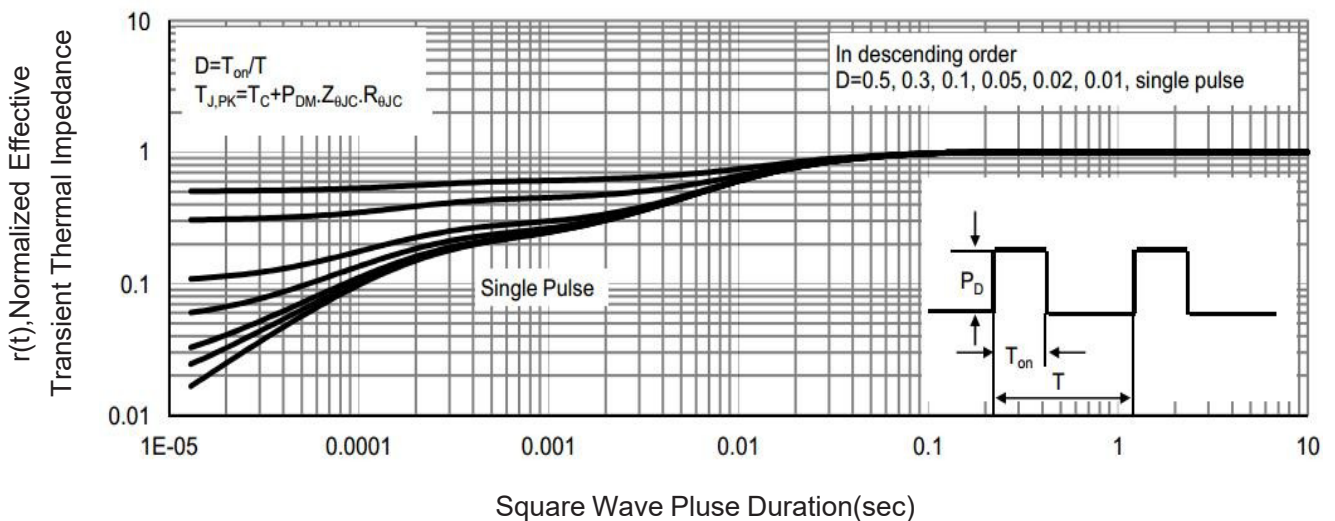


Figure 11 Normalized Maximum Transient Thermal Impedance