

Description

The VSM28N04 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

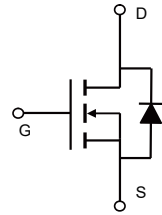
- $V_{DS} = 40\text{ V}, I_D = 28\text{ A}$
 $R_{DS(ON)} < 13\text{ m}\Omega @ V_{GS}=10\text{V}$ (Typ: 9.8 m Ω)
 $R_{DS(ON)} < 18.2\text{ m}\Omega @ V_{GS}=4.5\text{V}$ (Typ: 14 m Ω)
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- LED backlighting
- Uninterruptible power supply



DFN5x6



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM28N04	VSM28N04-D56	DFN5x6	Ø330mm	12mm	5000units

Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	28	A
Drain Current-Continuous($T_c=100^\circ\text{C}$)	$I_D(100^\circ\text{C})$	24.8	A
Pulsed Drain Current	I_{DM}	112	A
Maximum Power Dissipation	P_D	36	W
Debating factor		0.288	W/ $^\circ\text{C}$
Single pulse avalanche energy ^(Note 1)	E_{AS}	92	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance,Junction-to-Case	$R_{\theta JC}$	3.47	$^\circ\text{C/W}$
Thermal Resistance,Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	50	$^\circ\text{C/W}$

Electrical Characteristics (T_c=25°C unless otherwise noted)

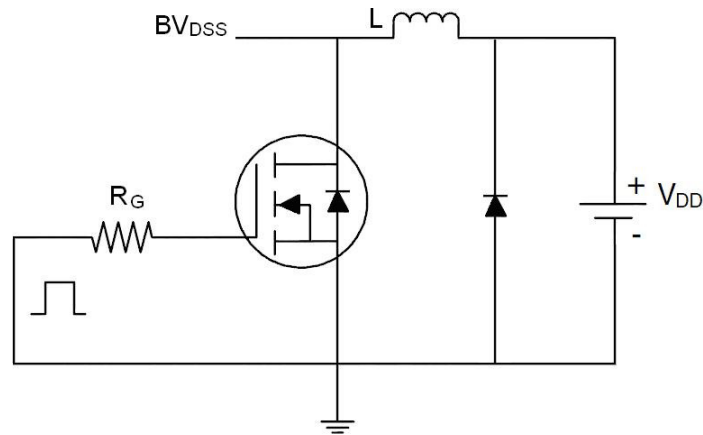
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	40	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0	1.5	2.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	9.8	13	mΩ
		V _{GS} =4.5V, I _D =20A	-	14	18.2	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =15A	-	15	-	S
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} =20V, V _{GS} =0V, F=1.0MHz	-	964	-	pF
Output Capacitance	C _{oss}		-	109	-	pF
Reverse Transfer Capacitance	C _{rss}		-	96	-	pF
Switching Characteristics (Note 3)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =20V, R _L =1.3Ω V _{GS} =10V, R _{GEN} =3Ω	-	5.5	-	nS
Turn-on Rise Time	t _r		-	14	-	nS
Turn-Off Delay Time	t _{d(off)}		-	24	-	nS
Turn-Off Fall Time	t _f		-	12	-	nS
Total Gate Charge	Q _g	V _{DS} =20V, I _D =15A, V _{GS} =10V	-	22.9	-	nC
Gate-Source Charge	Q _{gs}		-	3.5	-	nC
Gate-Drain Charge	Q _{gd}		-	5.3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _S =20A	-	-	1.2	V
Diode Forward Current	I _S		-	-	28	A

Notes:

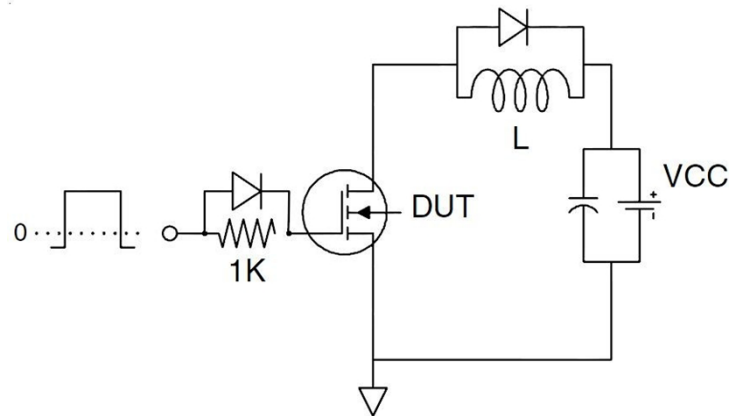
1. EAS condition : T_j=25°C, V_{DD}=32V, V_G=10V, L=0.5mH, R_g=25Ω.
2. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it.
3. Guaranteed by design, not subject to production.
4. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150°C. The SOA curve provides a single pulse rating.

Test circuit

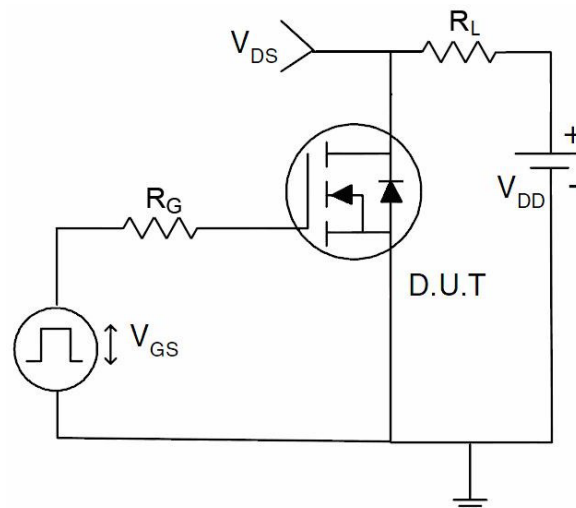
1) E_{AS} test Circuits



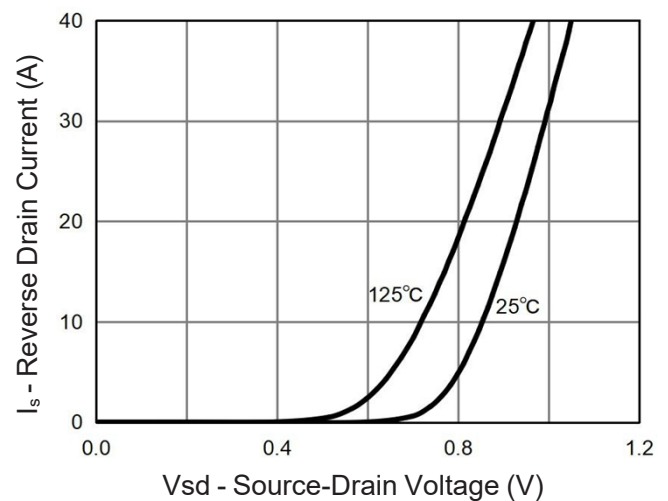
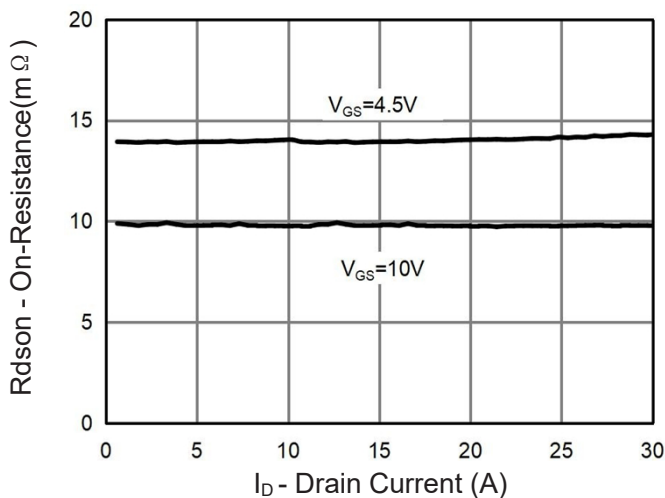
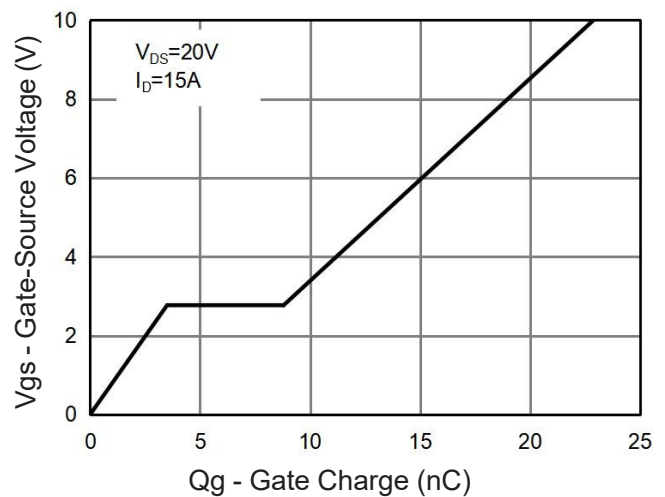
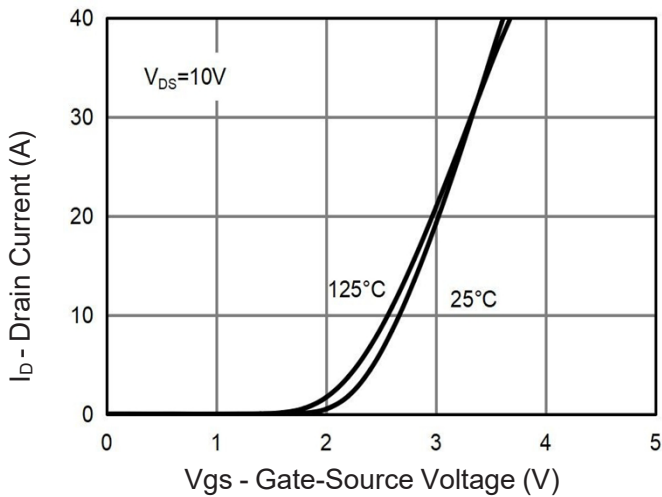
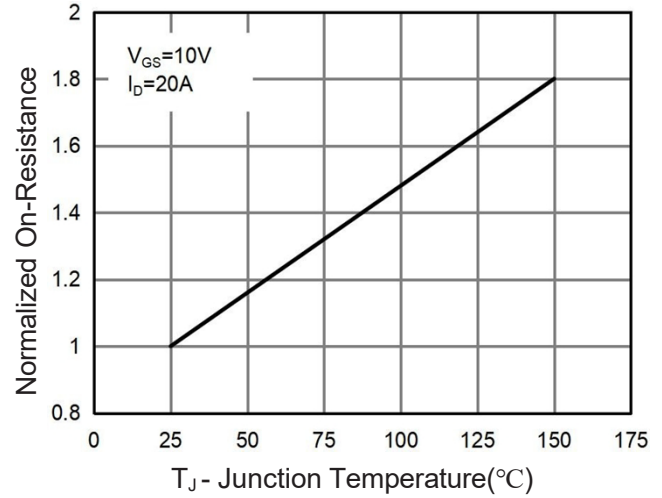
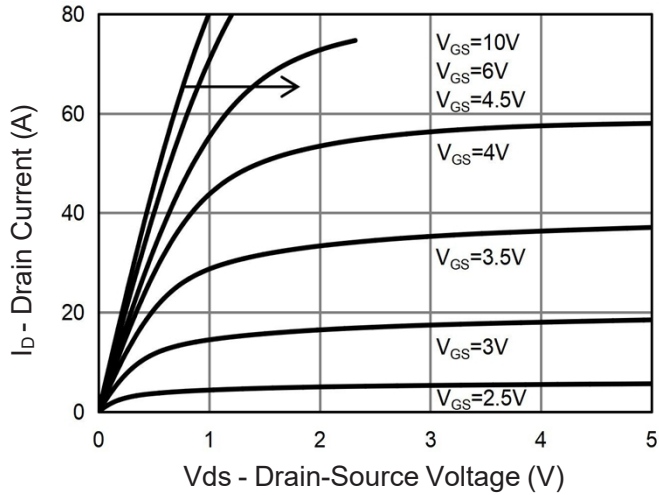
2) Gate charge test Circuit

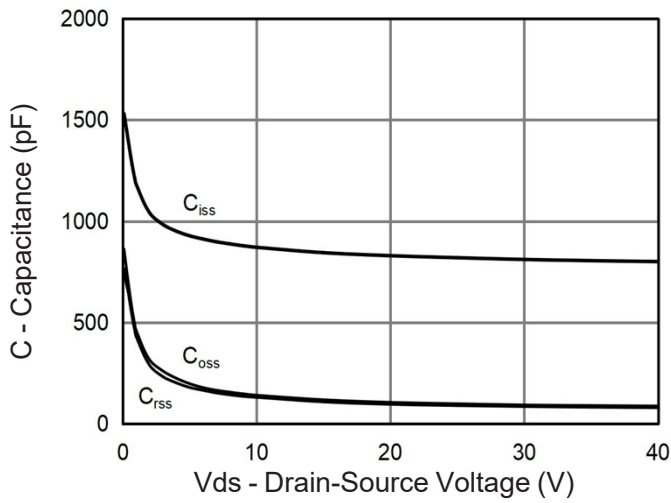
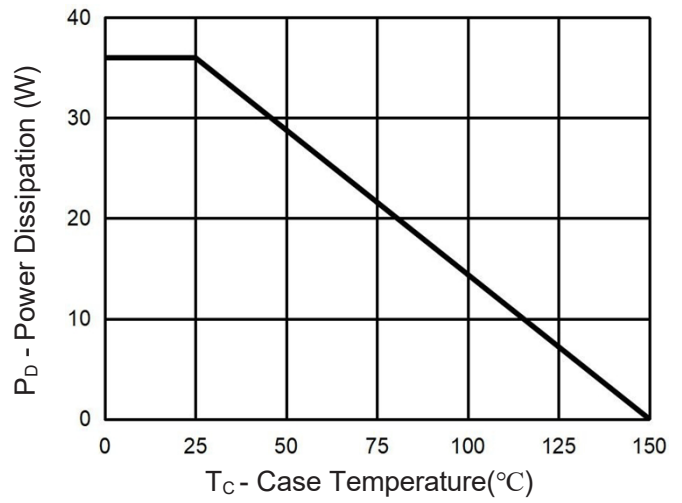
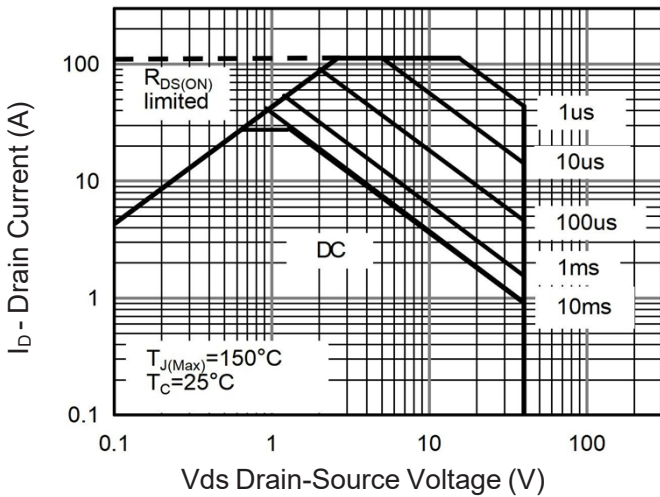
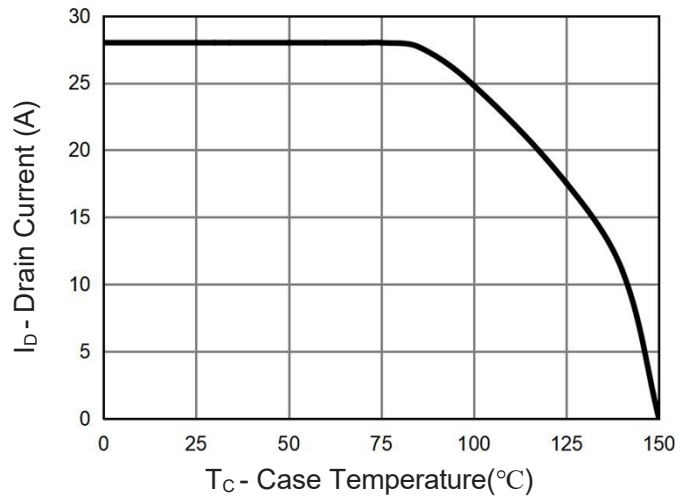
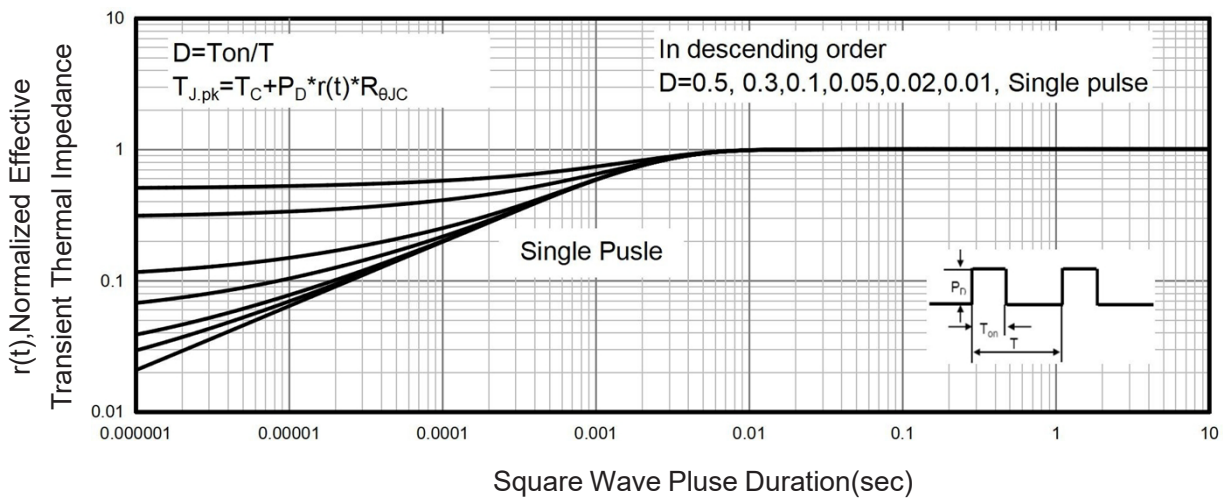


3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)




Figure 7 Capacitance vs Vds

Figure 9 Power De-rating

Figure 8 Safe Operation Area (Note 4)

Figure 10 Drain Current De-rating

Figure 11 Normalized Maximum Transient Thermal Impedance