Description

The VSM60N10 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.

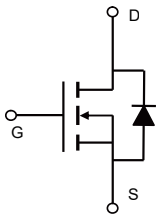
General Features

- V_{DS} = 100V,I_D =60A
  $R_{DS(ON)}$ <16mΩ @ V_{GS}=12.6V
- Special designed for convertors and power controls
- High density cell design for ultra low Rdson
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

DFN5x6



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM60N10	VSM60N10-D56	DFN5x6	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	60	A
Drain Current-Continuous(T_C=70℃)	I_D (70℃)	50	A
Pulsed Drain Current	I_{DM}	80	A
Maximum Power Dissipation	P_D	105	W
Derating factor		0.70	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	550	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to- Case (Note 2)	$R_{\theta Jc}$	1.43	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

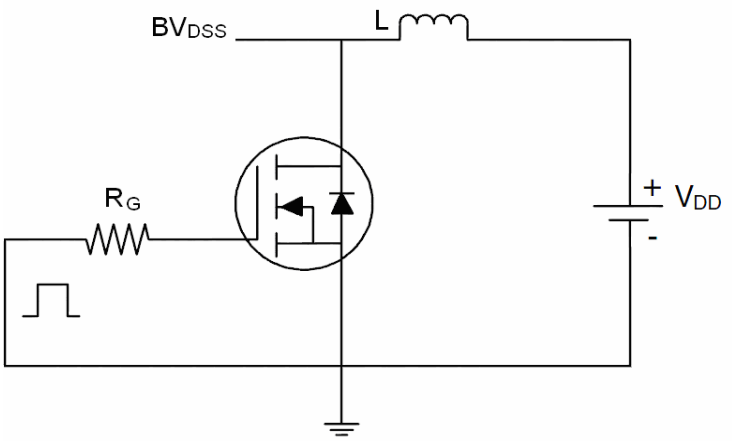
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	100	110	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2.5	3.7	4.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=30A	-	12.6	16	mΩ
Forward Transconductance	g_{FS}	V_{DS}=15V,I_D=10A	-	30	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=50V,V_{GS}=0V, F=1.0MHz	-	2850	-	PF
Output Capacitance	C_{oss}		-	220	-	PF
Reverse Transfer Capacitance	C_{rss}		-	90	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=30V,I_D=5A,R_L=10Ω V_{GS}=10V,R_G=1Ω	-	17	-	nS
Turn-on Rise Time	t_r		-	10	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	26	-	nS
Turn-Off Fall Time	t_f		-	10	-	nS
Total Gate Charge	Q_g	V_{DS}=50V,I_D=10A, V_{GS}=10V	-	47	-	nC
Gate-Source Charge	Q_{gs}		-	13	--	nC
Gate-Drain Charge	Q_{gd}		-	12.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=4A	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	60	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF = 10A di/dt = 100A/μs (Note3)	-	-	60	nS
Reverse Recovery Charge	Qrr		-	-	200	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

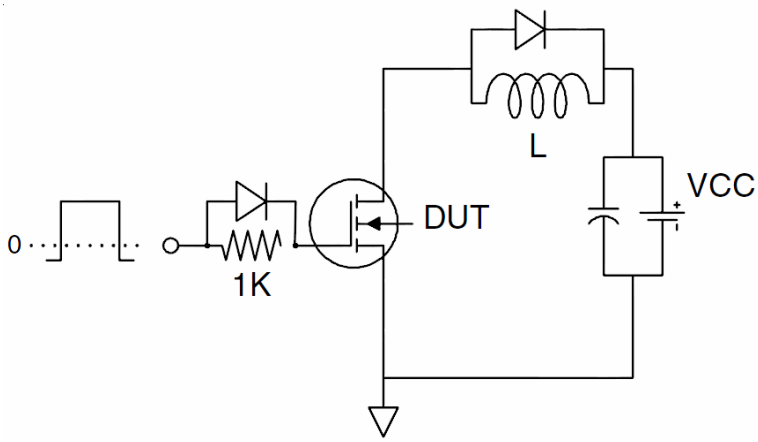
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition：Tj=25℃,V_{DD}=50V,V_G=10V,L=0.5mH,Rg=25Ω

Test Circuit

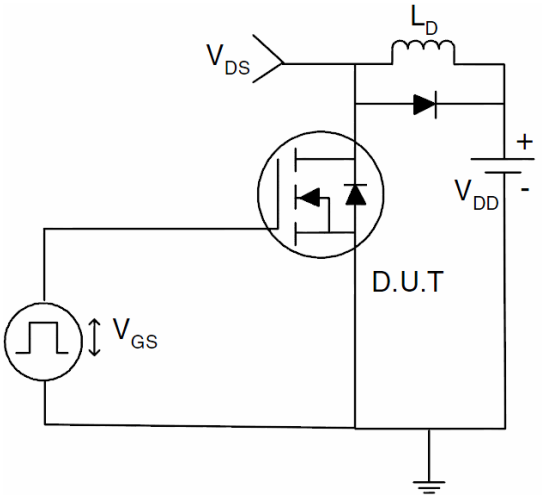
1） E_{AS} test Circuit



2） Gate charge test Circuit



3） Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

Figure1. Safe operating area

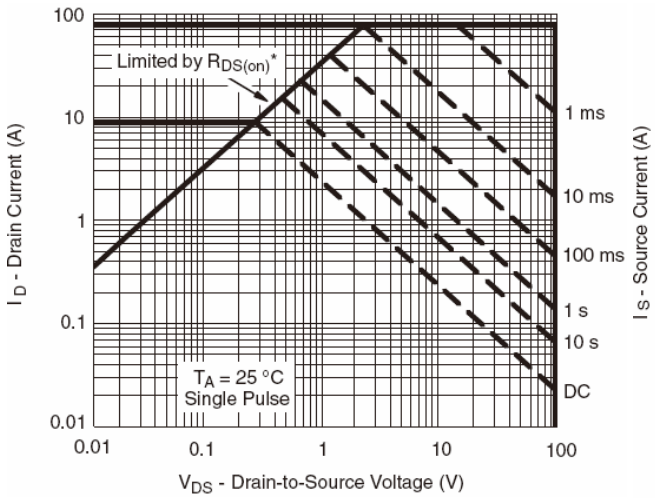


Figure2. Source-Drain Diode Forward Voltage

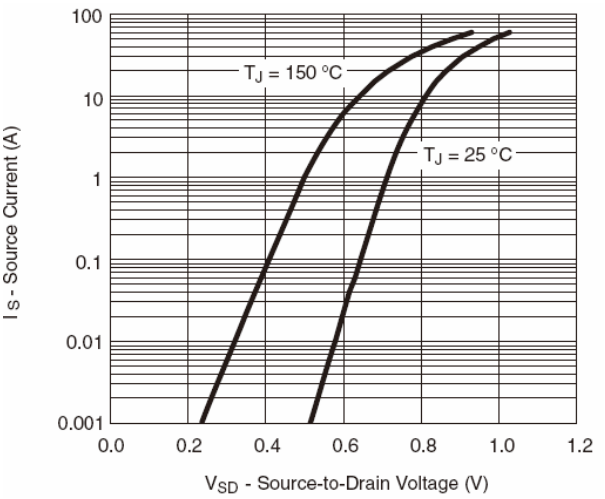


Figure3. Output characteristics

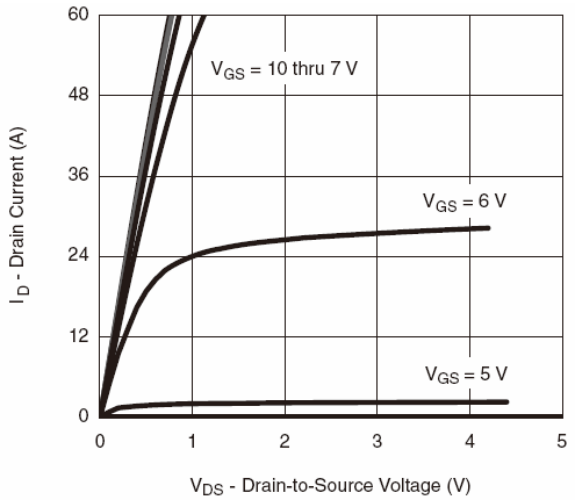


Figure4. Transfer characteristics

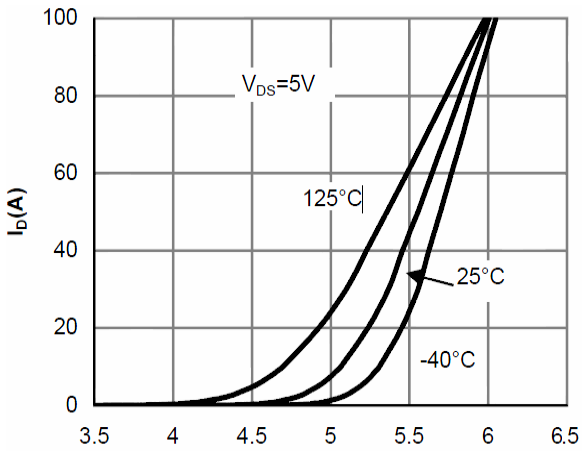


Figure5. Static drain-source on resistance

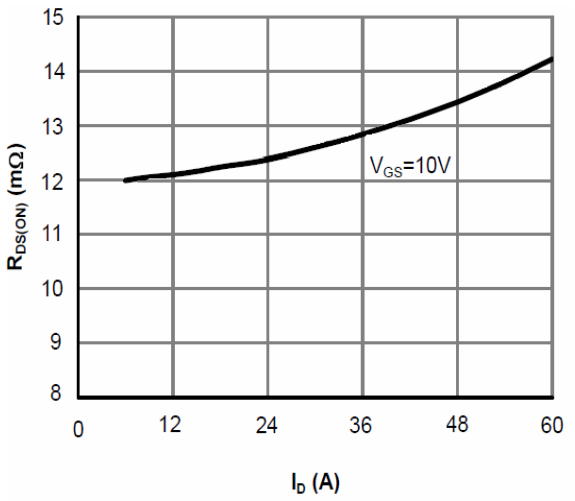


Figure6. $R_{DS(ON)}$ vs Junction Temperature

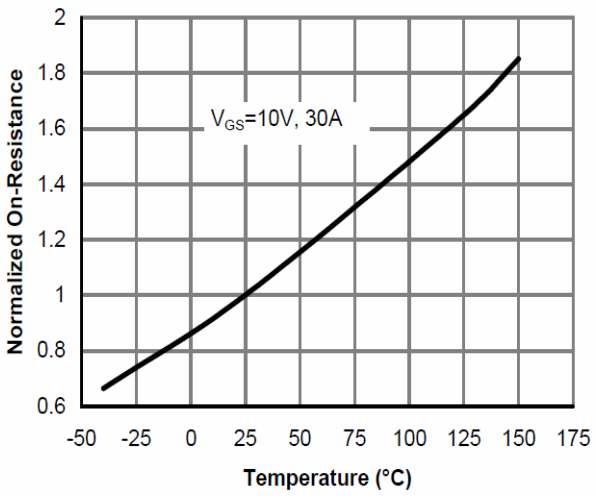


Figure7. BV_{DSS} vs Junction Temperature

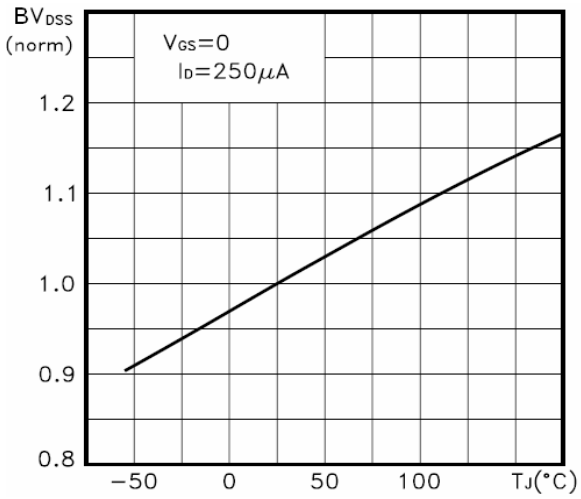


Figure8. $V_{GS(th)}$ vs Junction Temperature

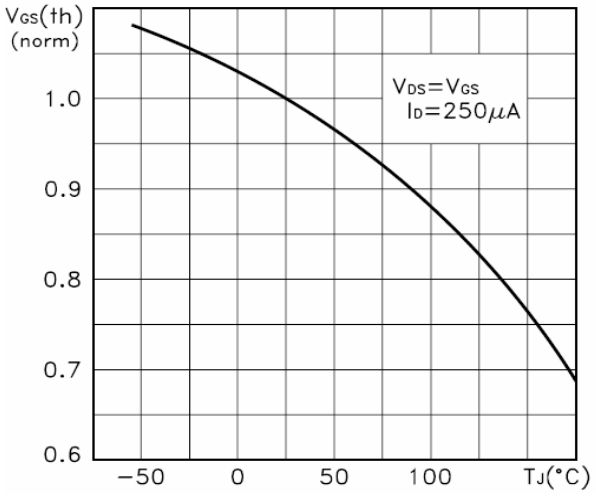


Figure9. Gate charge waveforms

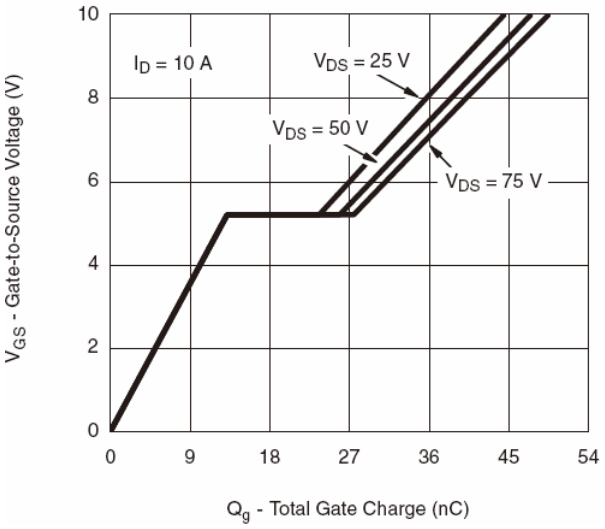


Figure10. Capacitance

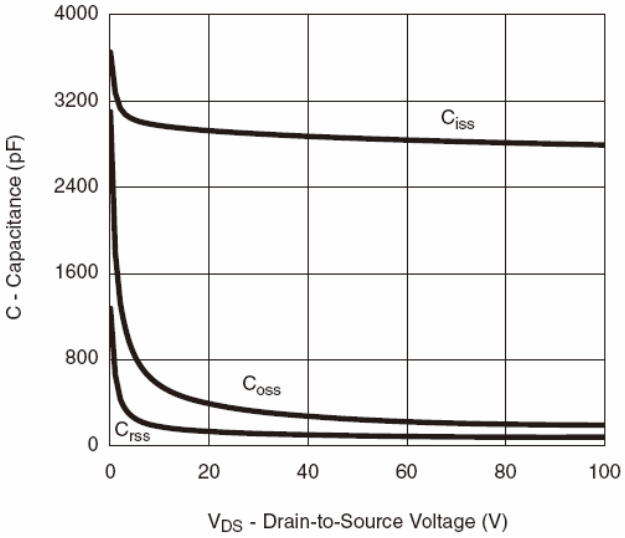


Figure11. Normalized Maximum Transient Thermal Impedance