

Description

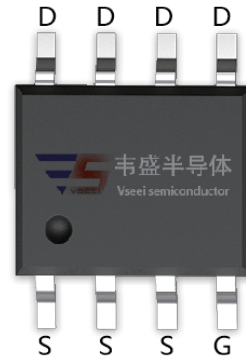
The VSM12N06 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

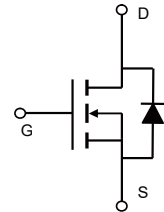
- $V_{DS} = 60V, I_D = 12A$
 $R_{DS(ON)} < 11m\Omega @ V_{GS}=10V$ (Typ:9mΩ)
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Low gate to drain charge to reduce switching losses

Application

- Power switching application
- Load switch



SOP-8



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM12N06	VSM12N06-S8	SOP-8	Ø330mm	12mm	4000 units

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	12	A
Drain Current-Continuous($T_C=100^{\circ}C$)	$I_D(100^{\circ}C)$	8.5	A
Pulsed Drain Current	I_{DM}	50	A
Maximum Power Dissipation	P_D	3	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^{\circ}C$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient(Note 2)	$R_{\theta JA}$	42	$^{\circ}C/W$
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Electrical Characteristics (TC=25°C unless otherwise noted)

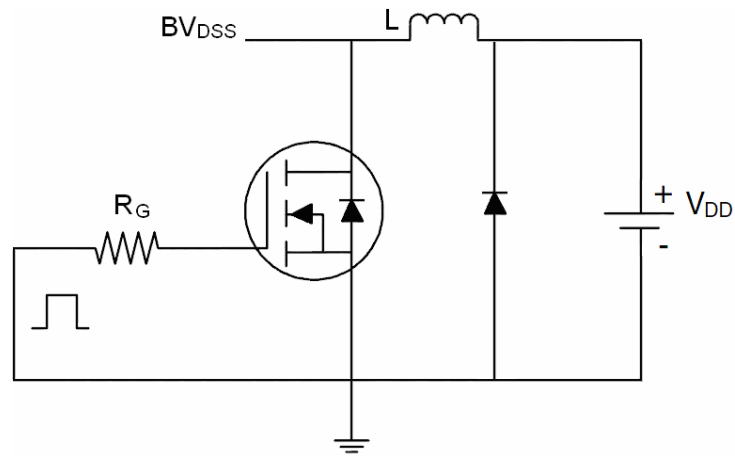
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	60		-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2	3	4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =12A	-	9	11	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =12A	40	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =30V, V _{GS} =0V, F=1.0MHz	-	3080	-	PF
Output Capacitance	C _{oss}		-	272	-	PF
Reverse Transfer Capacitance	C _{rss}		-	195	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =30V, R _L =1Ω V _{GS} =10V, R _{GEN} =3Ω	-	8	-	nS
Turn-on Rise Time	t _r		-	6.5	-	nS
Turn-Off Delay Time	t _{d(off)}		-	36	-	nS
Turn-Off Fall Time	t _f		-	13	-	nS
Total Gate Charge	Q _g	V _{DS} =30V, I _D =12A, V _{GS} =10V	-	55.5	-	nC
Gate-Source Charge	Q _{gs}		-	14.5	-	nC
Gate-Drain Charge	Q _{gd}		-	16.4	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =12A	-	-	1.2	V
Diode Forward Current (Note 2)	I _S		-	-	12	A
Reverse Recovery Time	t _{rr}	TJ = 25°C, IF=12A	-	30	-	nS
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs (Note3)	-	42	-	nC

Notes:

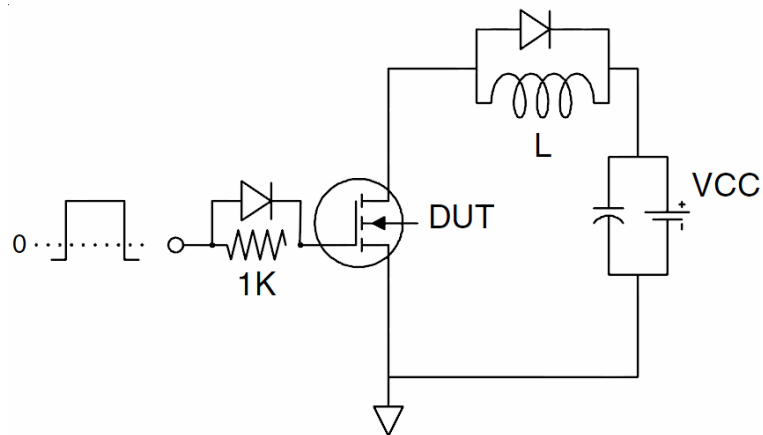
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

Test Circuit

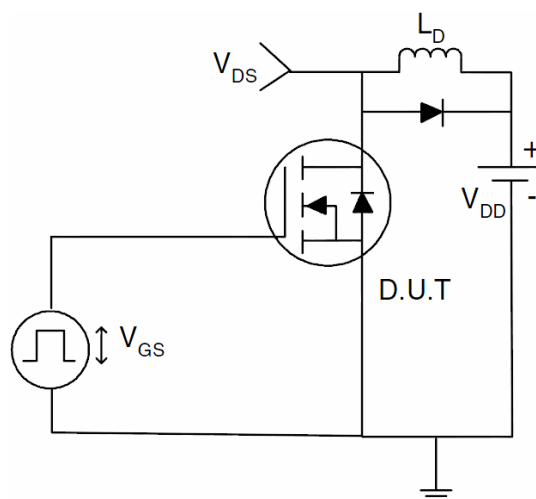
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

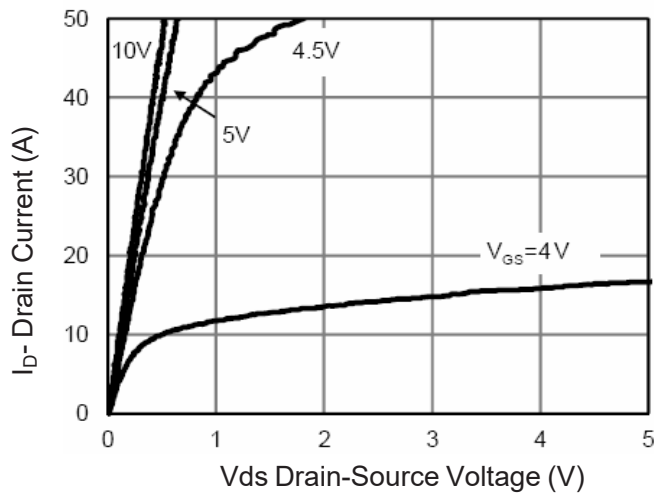


Figure 1 Output Characteristics

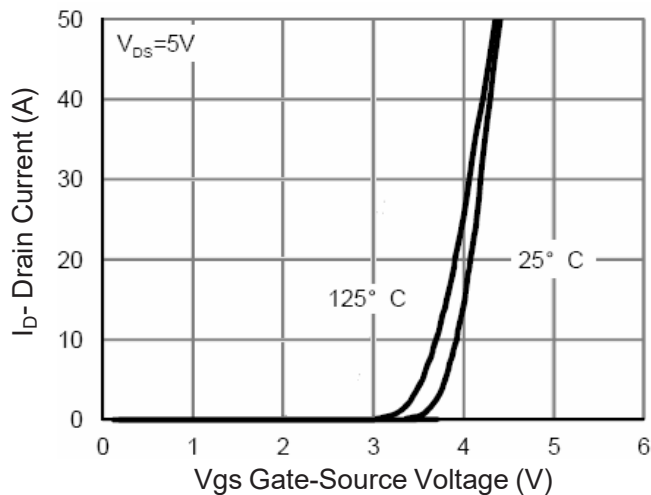


Figure 2 Transfer Characteristics

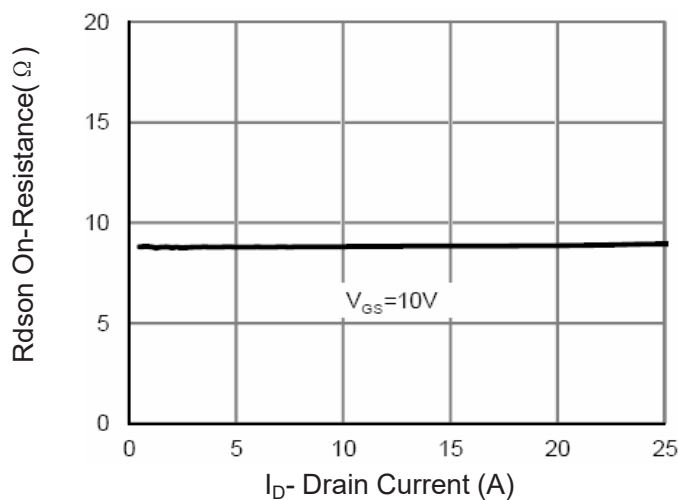


Figure 3 $R_{DS(on)}$ - Drain Current

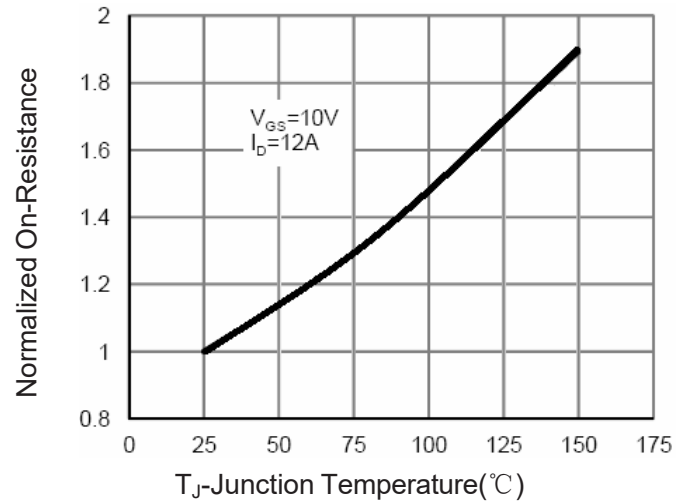


Figure 4 $R_{DS(on)}$ -Junction Temperature

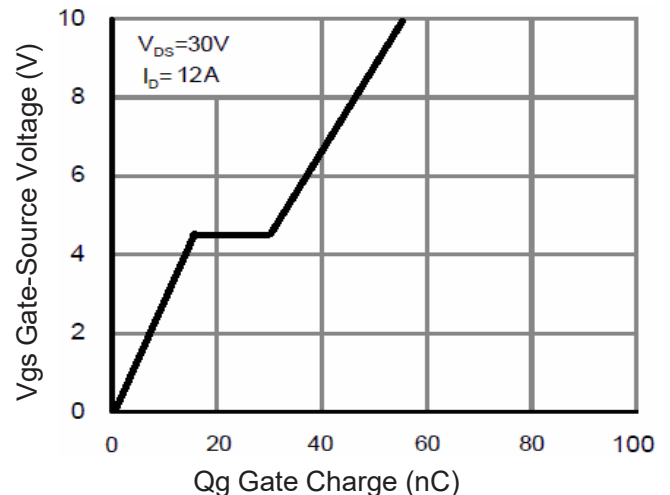


Figure 5 Gate Charge

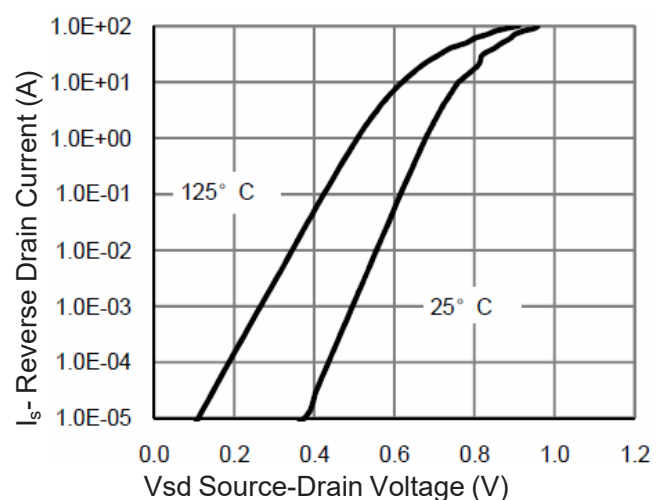
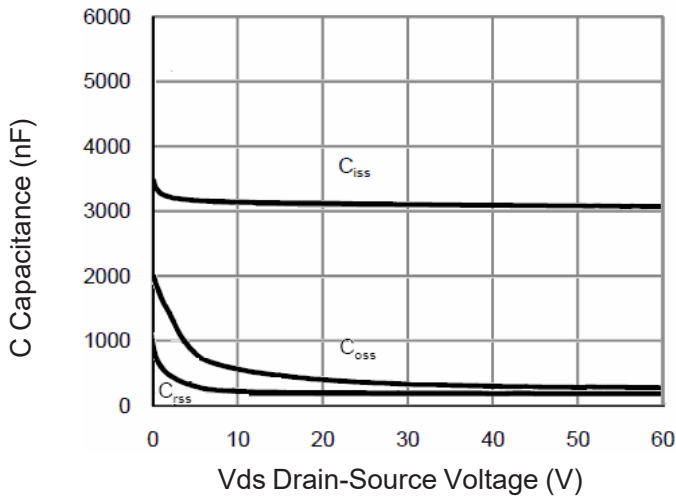
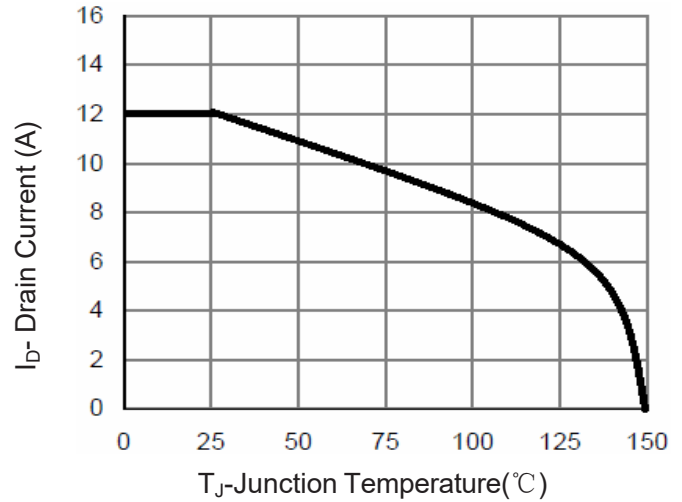
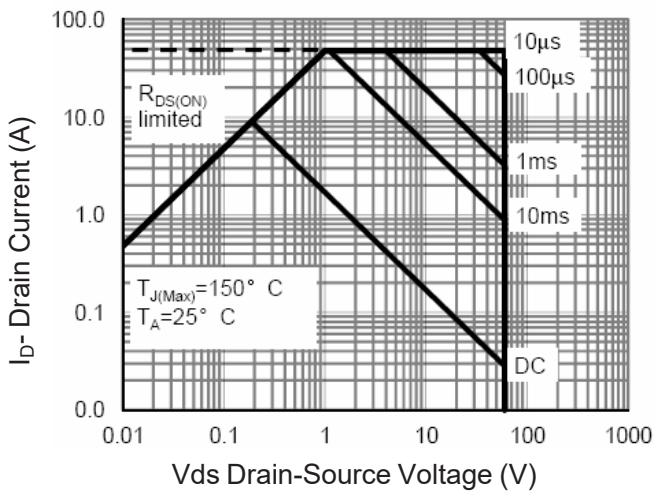
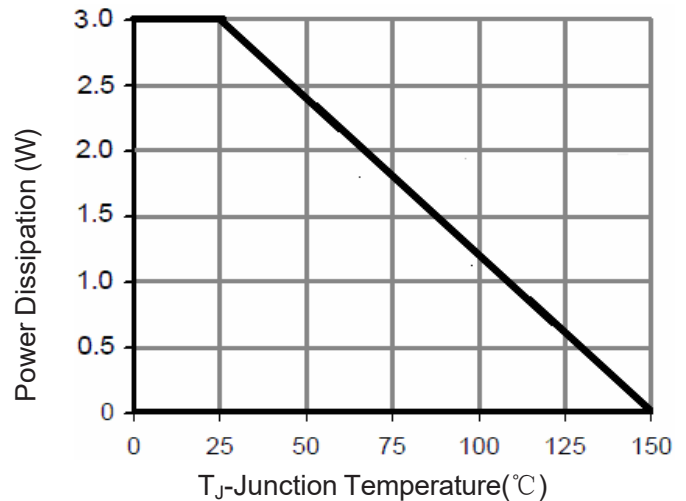
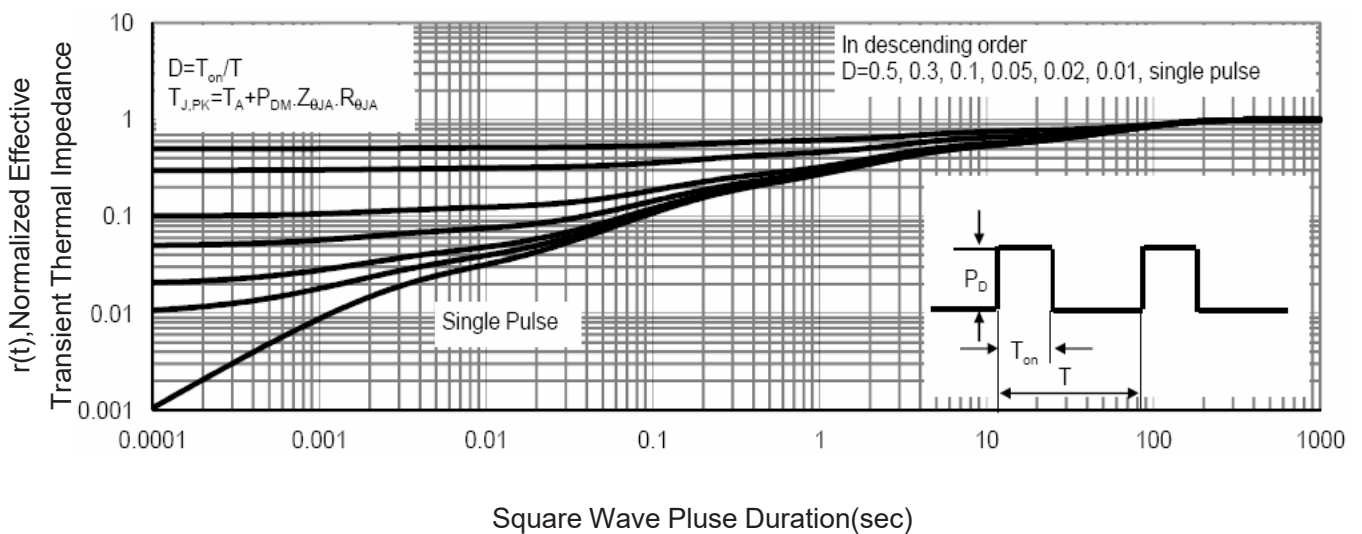


Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 Current De-rating

Figure 8 Safe Operation Area

Figure 10 Power De-rating

Figure 11 Normalized Maximum Transient Thermal Impedance