

Description

The VSM8N06 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

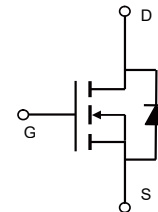
- $V_{DS} = 60V, I_D = 8A$
 $R_{DS(ON)} < 20m\Omega @ V_{GS}=10V$ (Typ:15.6m Ω)
 $R_{DS(ON)} < 28m\Omega @ V_{GS}=4.5V$ (Typ:20m Ω)
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Low gate to drain charge to reduce switching losses

Application

- Power switching application
- Load switch



SOP-8



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM8N06	VSM8N06-S8	SOP-8	-	-	-

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	8	A
Drain Current-Continuous($T_C=100^{\circ}C$)	$I_D(100^{\circ}C)$	5.6	A
Pulsed Drain Current	I_{DM}	32	A
Maximum Power Dissipation	P_D	2.1	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^{\circ}C$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	60	$^{\circ}C/W$
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Electrical Characteristics (TC=25°C unless otherwise noted)

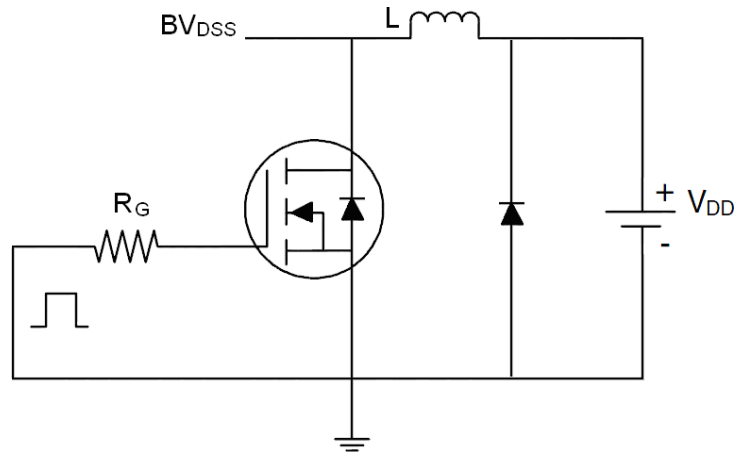
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	60		-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.6	2.2	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=8A$	-	15.6	20	m Ω
		$V_{GS}=4.5V, I_D=8A$	-	20	28	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=8A$	18	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{iss}	$V_{DS}=30V, V_{GS}=0V,$ $F=1.0MHz$	-	1600	-	PF
Output Capacitance	C_{oss}		-	112	-	PF
Reverse Transfer Capacitance	C_{rss}		-	98	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, R_L=1\Omega$ $V_{GS}=10V, R_{GEN}=3\Omega$	-	7	-	nS
Turn-on Rise Time	t_r		-	5.5	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	29	-	nS
Turn-Off Fall Time	t_f		-	4.5	-	nS
Total Gate Charge	Q_g	$V_{DS}=30V, I_D=8A,$ $V_{GS}=10V$	-	38.5	-	nC
Gate-Source Charge	Q_{gs}		-	4.7	-	nC
Gate-Drain Charge	Q_{gd}		-	10.3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=8A$	-	-	1.2	V
Diode Forward Current (Note 2)	I_S	-	-	-	8	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}C, I_F = 8A$	-	28	-	nS
Reverse Recovery Charge	Q_{rr}	$di/dt = 100A/\mu s$ (Note3)	-	40	-	nC

Notes:

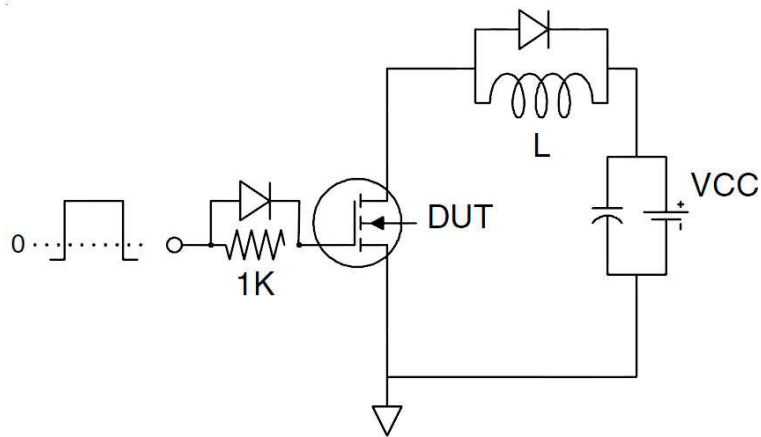
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

Test Circuit

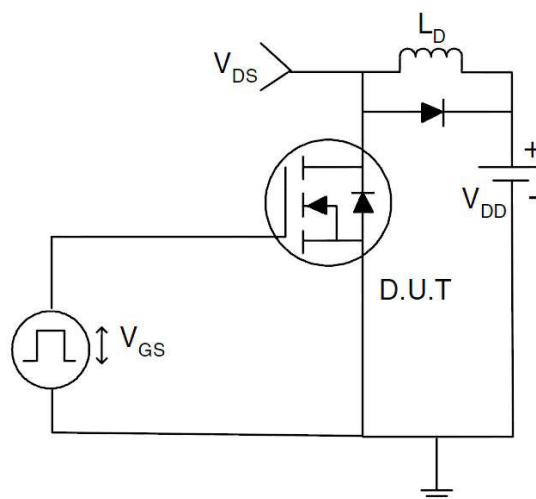
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

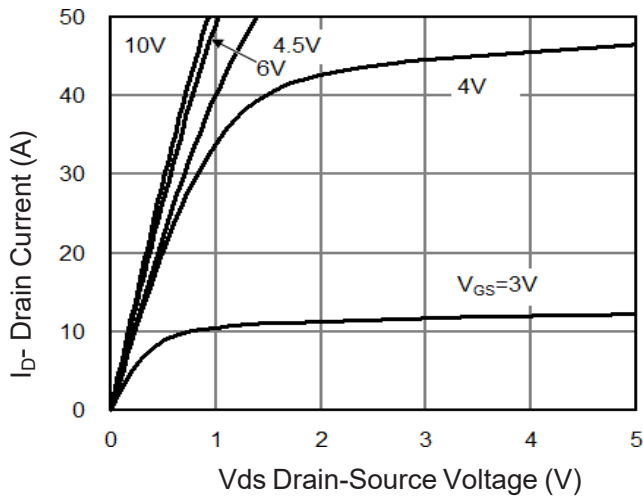


Figure 1 Output Characteristics

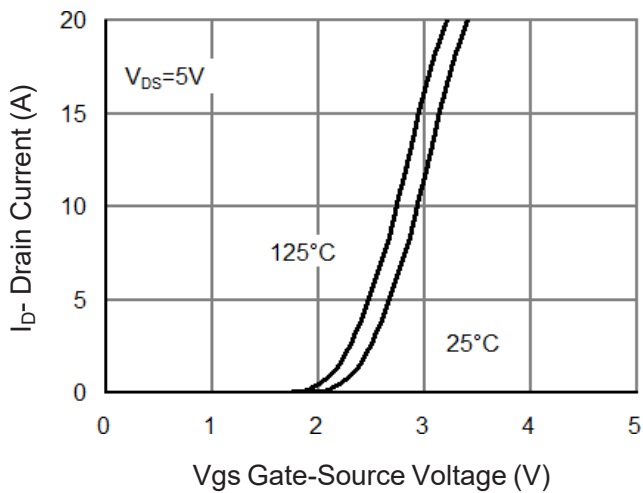


Figure 2 Transfer Characteristics

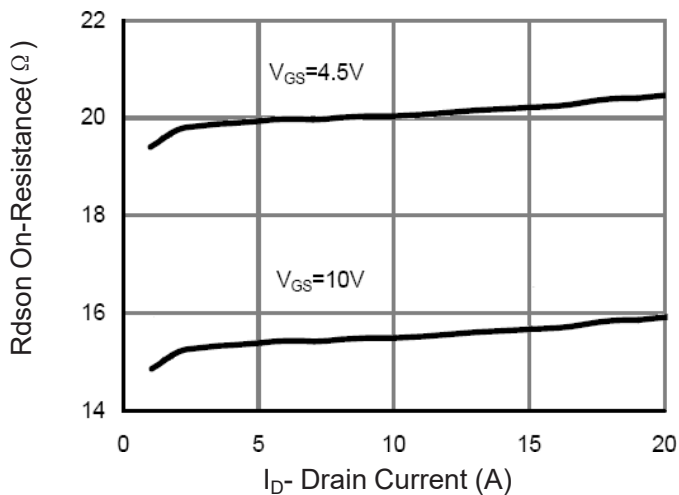


Figure 3 Rdson- Drain Current

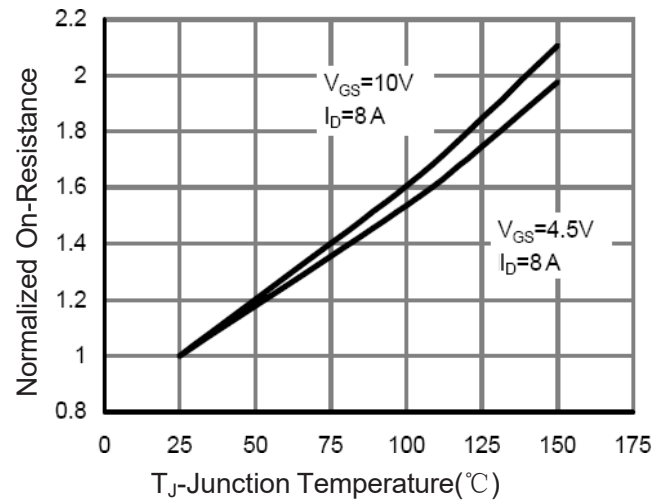


Figure 4 Rdson-Junction Temperature

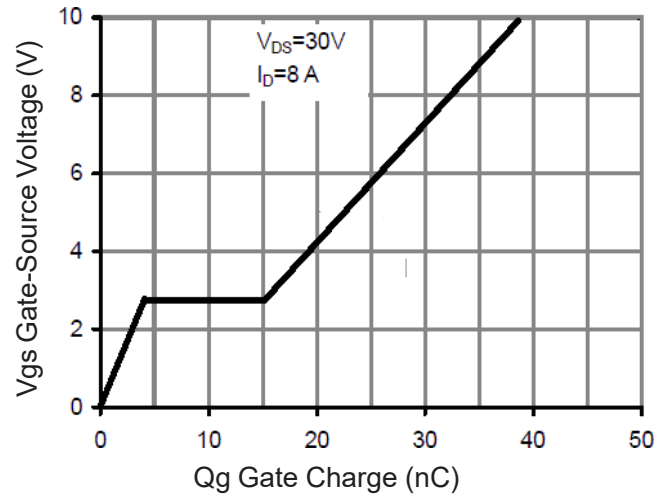


Figure 5 Gate Charge

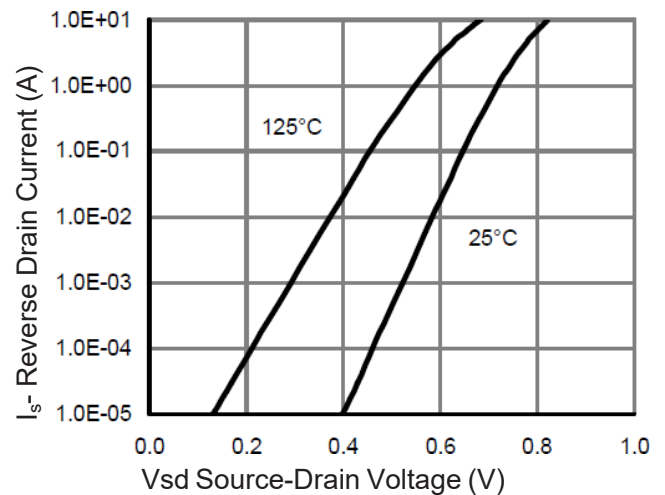
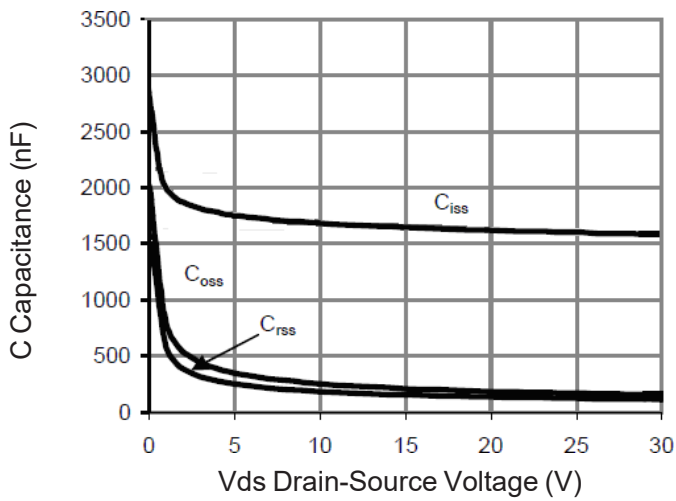
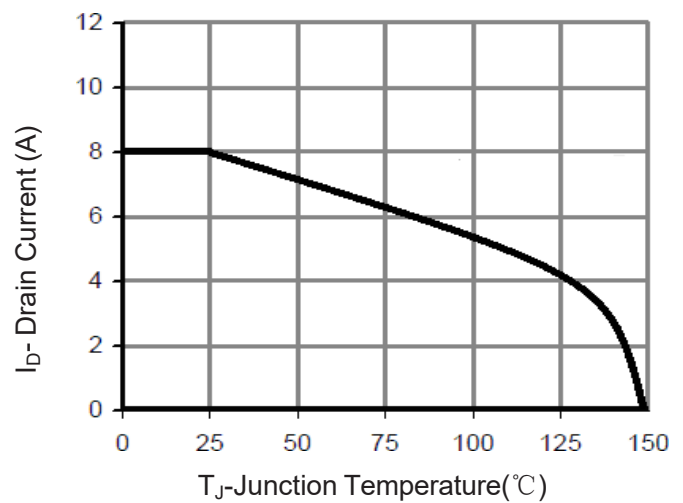
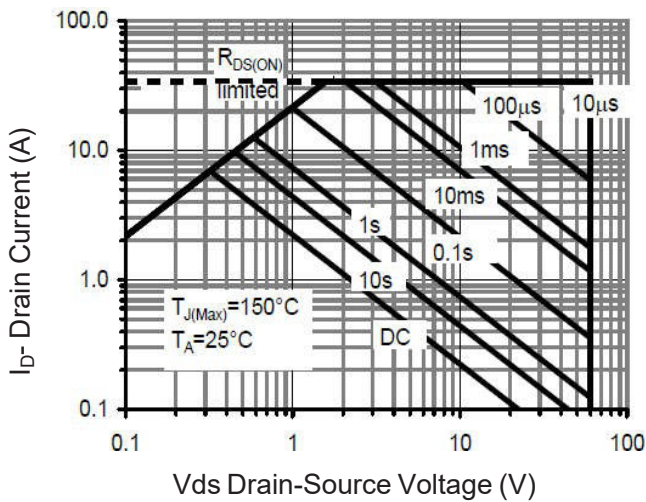
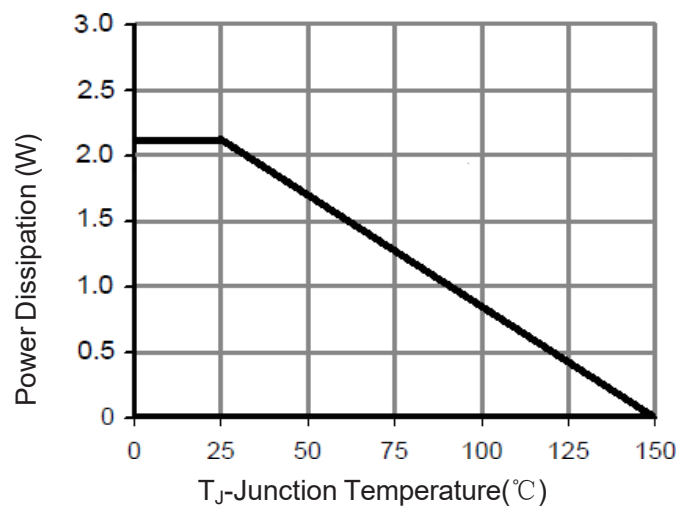
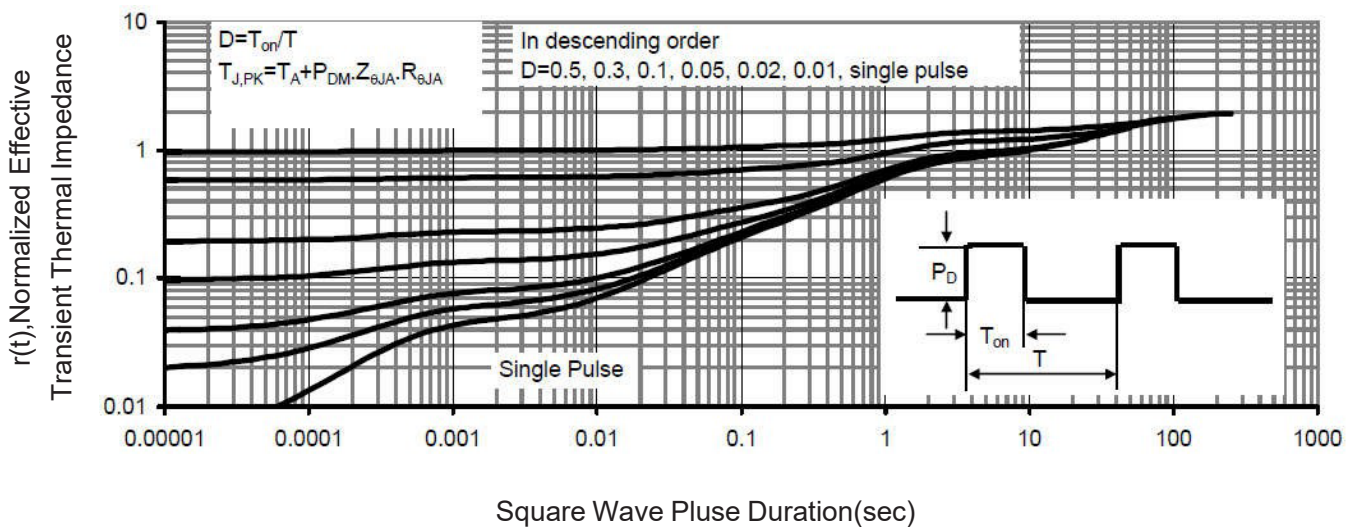


Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 Current De-rating

Figure 8 Safe Operation Area

Figure 10 Power De-rating

Figure 11 Normalized Maximum Transient Thermal Impedance