

Description

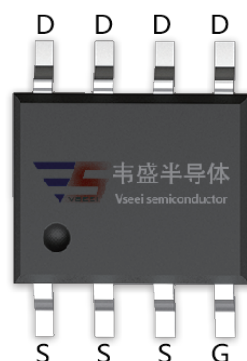
The VSM8N10 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

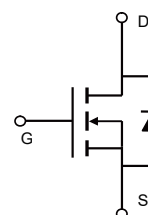
- $V_{DS} = 100V, I_D = 8A$
 $R_{DS(ON)} < 32m\Omega @ V_{GS}=10V$ (Typ:26m Ω)
 $R_{DS(ON)} < 35m\Omega @ V_{GS}=10V$ (Typ:29m Ω)
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current

Application

- DC/DC Primary Side Switch
- Telecom/Server
- Synchronous Rectification



SOP-8



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM8N10	VSM8N10-S8	SOP-8	Ø330mm	12mm	4000 units

Absolute Maximum Ratings ($T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	8	A
Drain Current-Continuous($T_A=100^{\circ}C$)	$I_D(100^{\circ}C)$	5.6	A
Pulsed Drain Current ^(Note 1)	I_{DM}	57	A
Maximum Power Dissipation	P_D	2.6	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^{\circ}C$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	48	$^{\circ}C/W$
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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

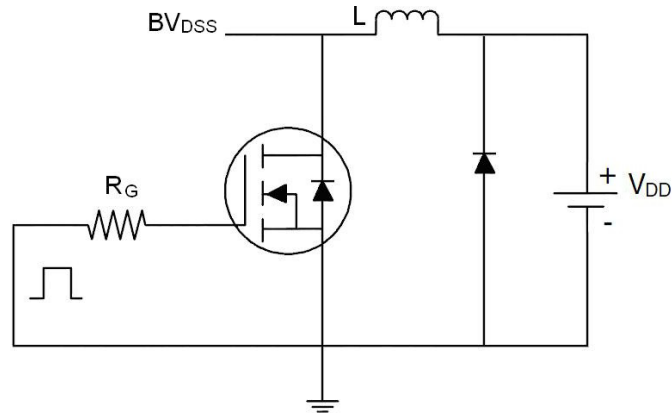
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.3	1.8	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=8A$	-	26	32	m Ω
		$V_{GS}=4.5V, I_D=8A$	-	29	35	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=8A$	-	20	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{iss}	$V_{DS}=50V, V_{GS}=0V,$ $F=1.0MHz$	-	2479	-	PF
Output Capacitance	C_{oss}		-	96	-	PF
Reverse Transfer Capacitance	C_{rss}		-	79	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=50V, I_D=10A, R_L=5\Omega,$ $R_G=1\Omega, V_{GS}=10V$	-	9	-	nS
Turn-on Rise Time	t_r		-	9	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	32	-	nS
Turn-Off Fall Time	t_f		-	8	-	nS
Total Gate Charge	Q_g	$I_D=10A, V_{DD}=50V, V_{GS}=10V$	-	67.2	-	nC
Gate-Source Charge	Q_{gs}		-	9.4	-	nC
Gate-Drain Charge	Q_{gd}		-	15.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=8A$	-	0.85	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	8	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}C, I_F = 8A$ $di/dt = 100A/\mu s$ (Note3)	-	30	-	nS
Reverse Recovery Charge	Q_{rr}		-	44	-	nC

Notes:

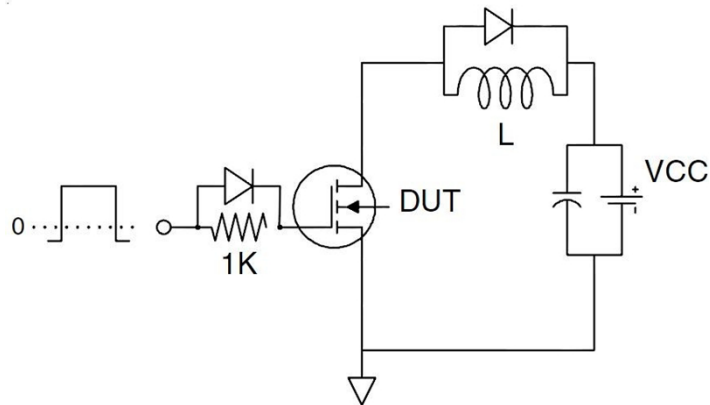
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

Test Circuit

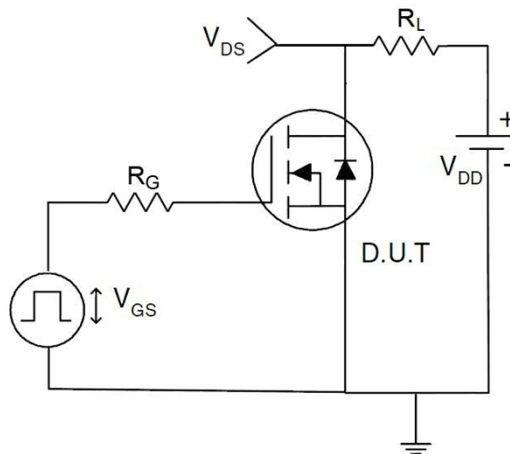
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

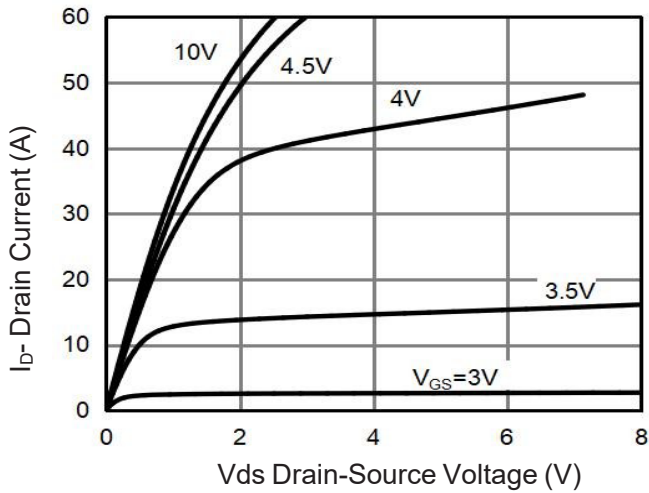


Figure 1 Output Characteristics

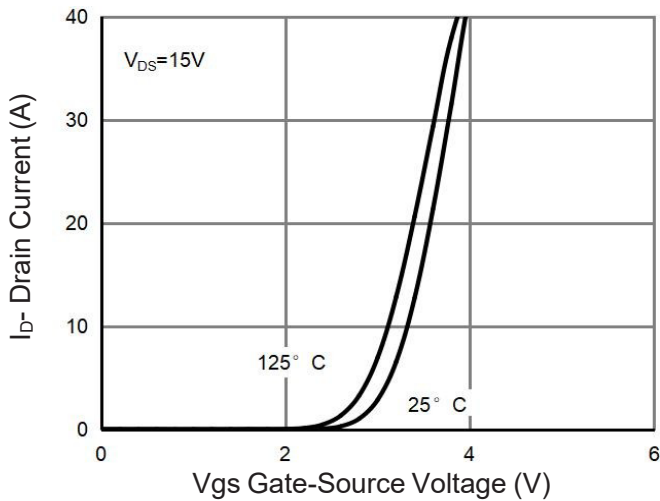


Figure 2 Transfer Characteristics

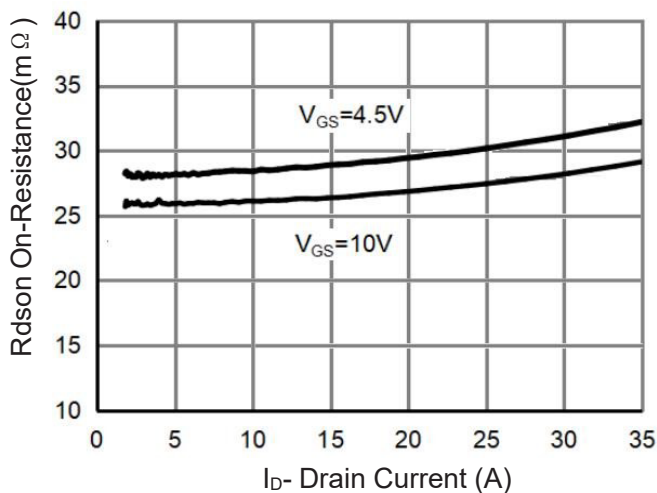


Figure 3 $R_{DS(on)}$ - Drain Current

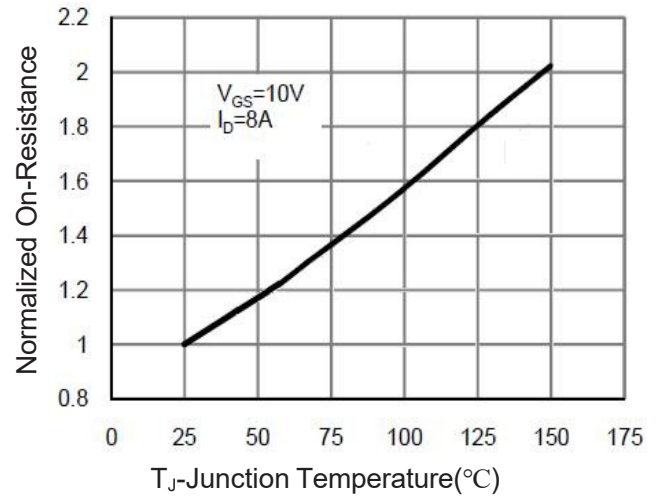


Figure 4 $R_{DS(on)}$ -Junction Temperature

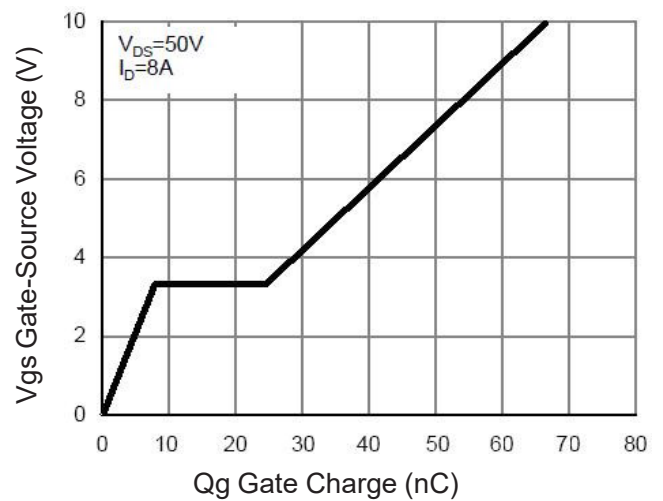


Figure 5 Gate Charge

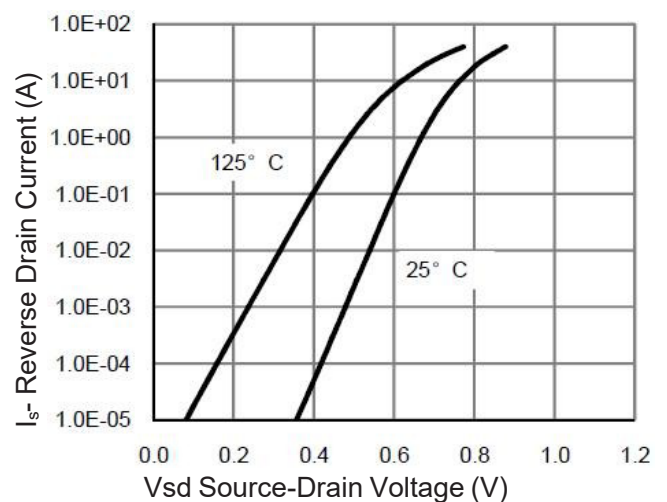
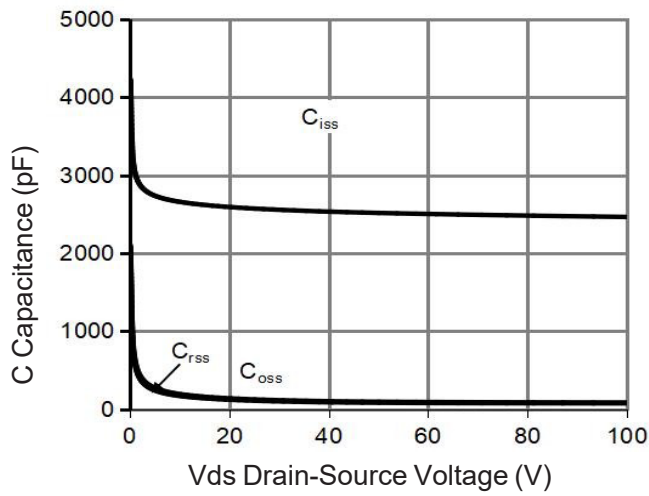
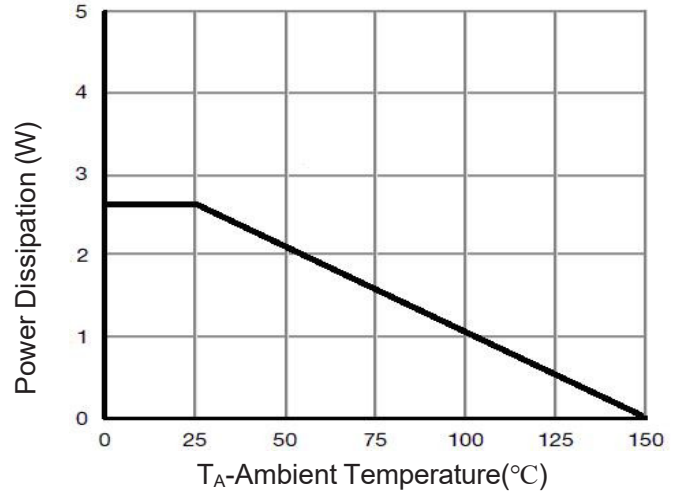
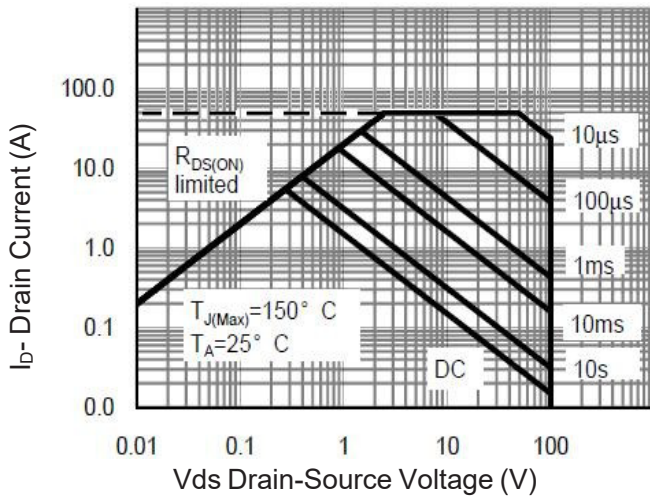
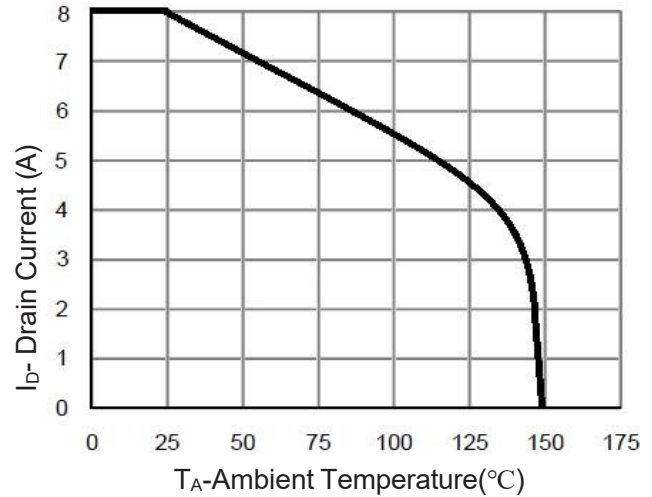
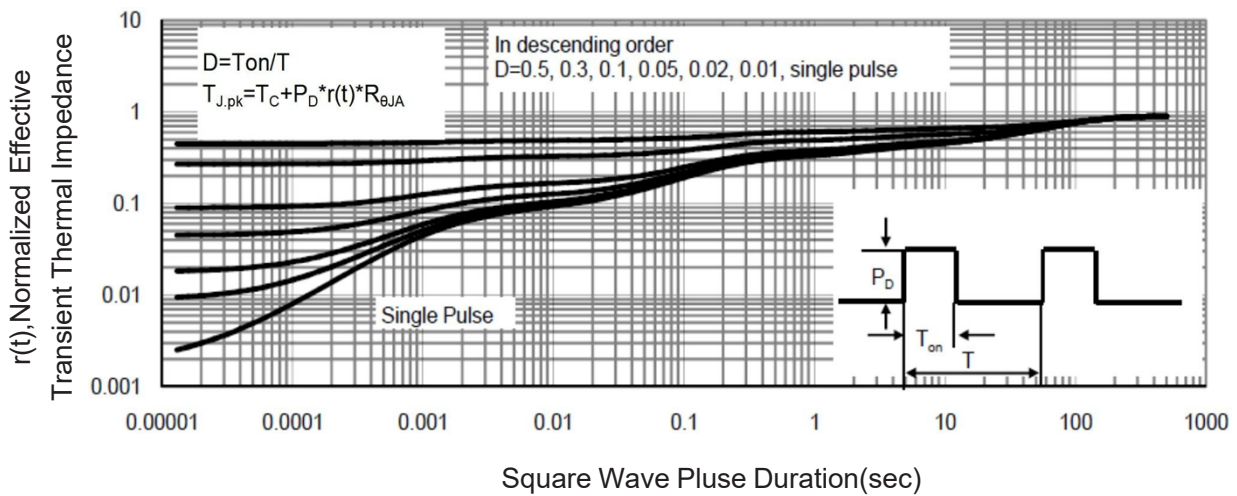


Figure 6 Source-Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 Power De-rating

Figure 8 Safe Operation Area

Figure 10 Current De-rating

Figure 11 Normalized Maximum Transient Thermal Impedance