## Description

The VSM3008BY uses advanced trench technology and design to provide excellent $R_{DS(on)}$ with low gate charge. It can be used in a wide variety of applications.

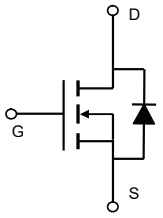
## General Features

- $V_{DS}$ = 30 V,$I_D$ = 8 A
  $R_{DS(on)}$ < 13.5 mΩ @ $V_{GS}$=10V
- High density cell design for ultra low $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high $E_{AS}$
- Excellent package for good heat dissipation
- 100% Rg tested
- 100% ΔVds tested
- 100% UIS tested

## Application

- Power switching applications
- Hard switched and high frequency circuits
- Uninterruptible power supply


SOT-23-3




Schematic

## Package Marking and Ordering Information

| Device Marking | Device | Device Package | Reel Size | Tape width | Quantity |
|---|---|---|---|---|---|
| VSM3008BY | VSM3008BY-S2-3 | SOT-23-3 | Ø178mm | 8mm | 3000units |

## Absolute Maximum Ratings ($T_A$=25℃unless otherwise noted)

| Parameter | Symbol | Limit | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 30 | V |
| Gate-Source Voltage | $V_{GS}$ | ±20 | V |
| Drain Current-Continuous | $I_D$ | 8 | A |
| Drain Current-Continuous($T_A$=75℃) | $I_D$ (75℃) | 6.2 | A |
| Pulsed Drain Current | $I_{DM}$ | 32 | A |
| Maximum Power Dissipation | $P_D$ | 1.47 | W |
| Single pulse avalanche energy (Note 1) | $E_{AS}$ | 44 | mJ |
| Operating Junction and Storage Temperature Range | $T_J$,$T_{STG}$ | -55 To 150 | ℃ |

## Thermal Characteristic

| | | | |
|---|---|---|---|
| Thermal Resistance,Junction-to-Cace (Note 2) | $R_{\theta JC}$ | 63 | ℃/W |
| Thermal Resistance,Junction-to-Ambient (Note 3) | $R_{\theta JA}$ | 85 | ℃/W |

## Electrical Characteristics ($T_A$=25℃unless otherwise noted)

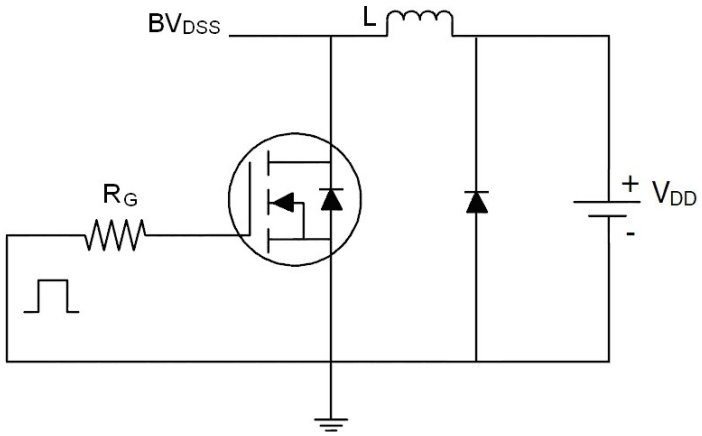
| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$=0V $I_D$=250μA | 30 | - | - | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$=30V,$V_{GS}$=0V | - | - | 1 | uA |
| Gate-Body Leakage Current | $I_{GSS}$ | $V_{GS}$=±20V,$V_{DS}$=0V | - | - | ±100 | nA |
| **On Characteristics** | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$,$I_D$=250μA | 1.2 | 1.9 | 2.5 | V |
| Drain-Source On-State Resistance | $R_{DS(ON)}$ | $V_{GS}$=10V, $I_D$=6A | - | 11.7 | 13.5 | mΩ |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$=10V,$I_D$=8A | - | 18 | - | S |
| **Dynamic Characteristics** | | | | | | |
| Input Capacitance | $C_{lss}$ | $V_{DS}$=15V,$V_{GS}$=0V, F=1.0MHz | - | 520.1 | - | pF |
| Output Capacitance | $C_{oss}$ | | - | 97.3 | - | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 81.7 | - | pF |
| **Switching Characteristics**(Note 4) | | | | | | |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}$=15V,$R_L$=0.5Ω, $V_{GS}$=10V,$R_{GEN}$=3Ω | - | 5 | - | nS |
| Turn-on Rise Time | $t_r$ | | - | 8 | - | nS |
| Turn-off Delay Time | $t_{d(off)}$ | | - | 20 | - | nS |
| Turn-off Fall Time | $t_f$ | | - | 7 | - | nS |
| Total Gate Charge | $Q_g$ | $V_{DS}$=15V,$I_D$=5A, $V_{GS}$=10V | - | 27.9 | - | nC |
| Gate-Source Charge | $Q_{gs}$ | | - | 8.4 | - | nC |
| Gate-Drain Charge | $Q_{gd}$ | | - | 4.2 | - | nC |
| **Drain-Source Diode Characteristics** | | | | | | |
| Diode Forward Voltage | $V_{SD}$ | $V_{GS}$=0V,$I_S$=4A | - | - | 1.2 | V |
| Diode Forward Current | $I_S$ | | - | - | 8 | A |

## Notes:

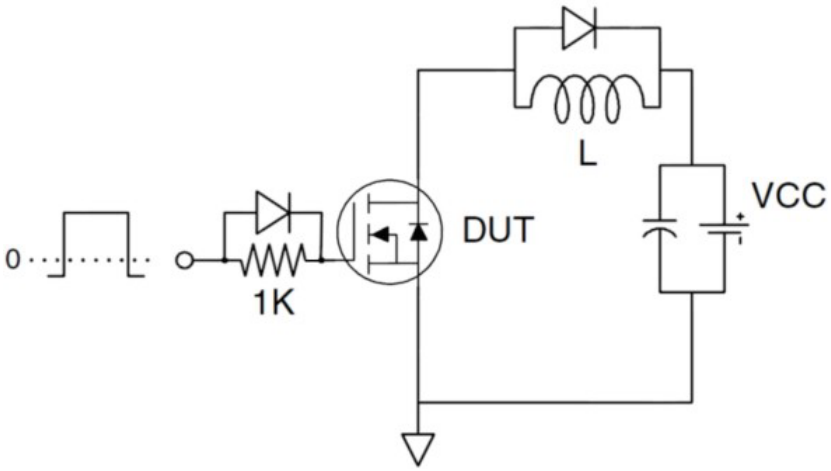
1. EAS condition : Tj=25℃,$V_{DD}$=25V,$V_G$=10V,L=0.5mH,Rg=25Ω.
2. The $R_{\theta JC}$ is the thermal impedance from junction to lead.
3. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A$ =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it.
4. Guaranteed by design, not subject to production.
5. These curves are based on the junction-to-ambient thermal impedance, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

## Test Circuit

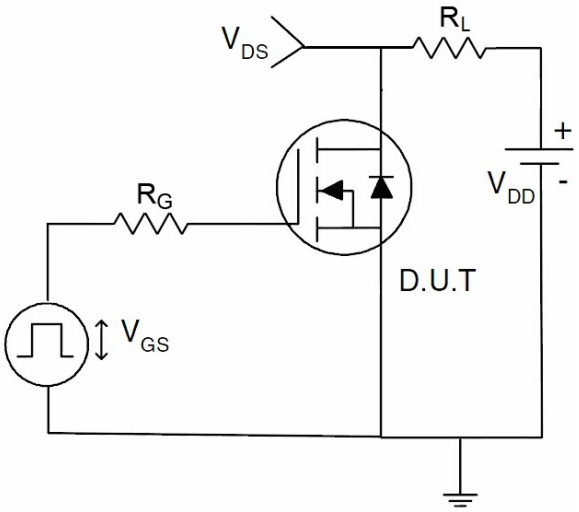
### 1) $E_{AS}$ Test Circuit




### 2) Gate Charge Test Circuit




### 3) Switch Time Test Circuit



## Typical Electrical and Thermal Characteristics (Curves)

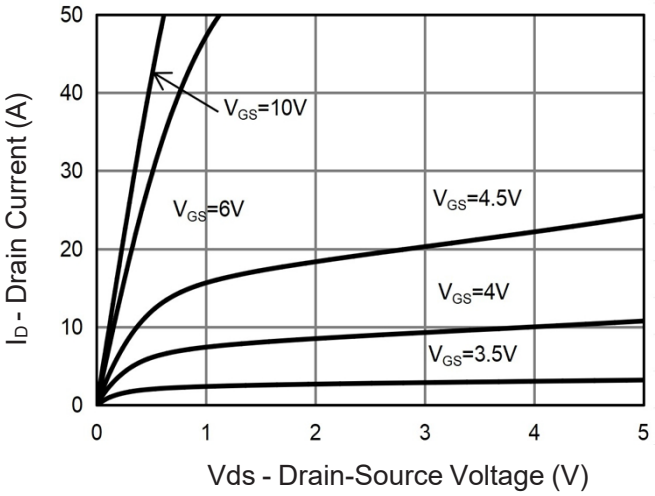



**Figure 1 Output Characteristics**

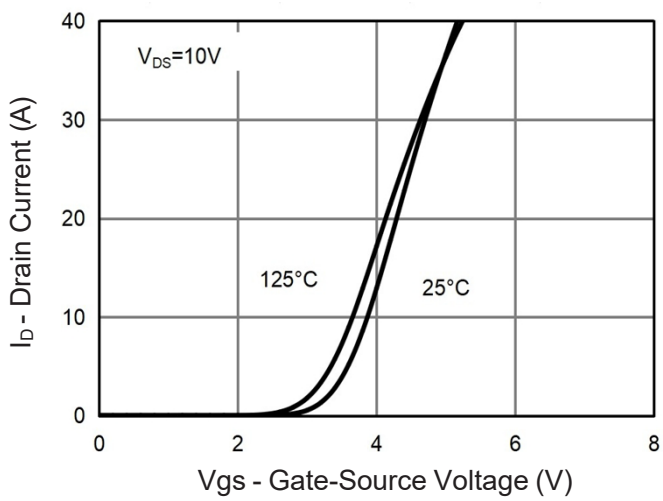



**Figure 2 Transfer Characteristics**

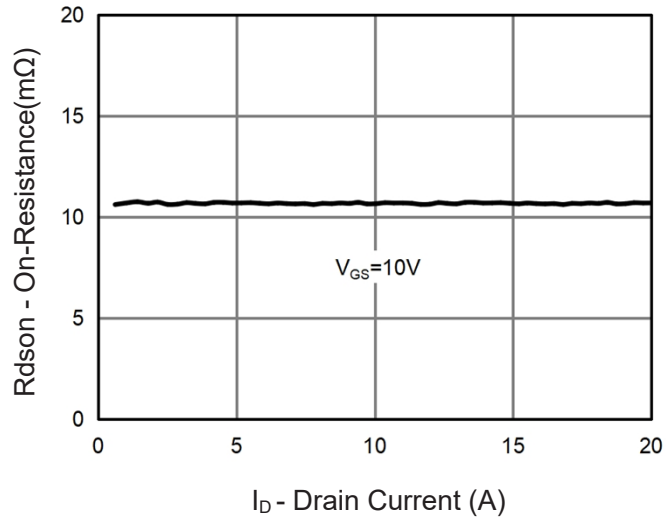



**Figure 3 Rdson vs Drain Current**

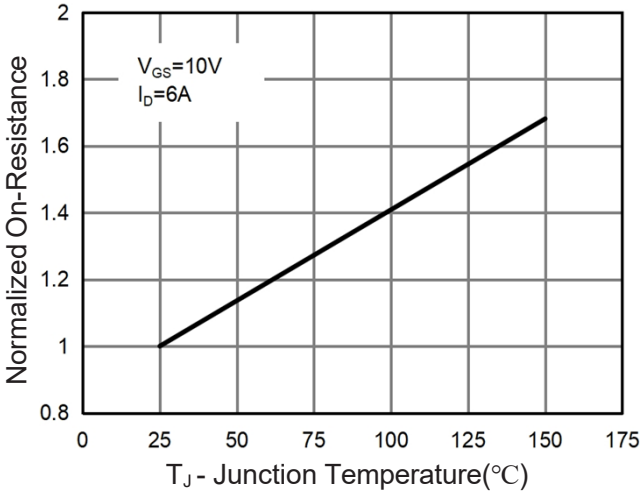



**Figure 4 Rdson vs Junction Temperature**

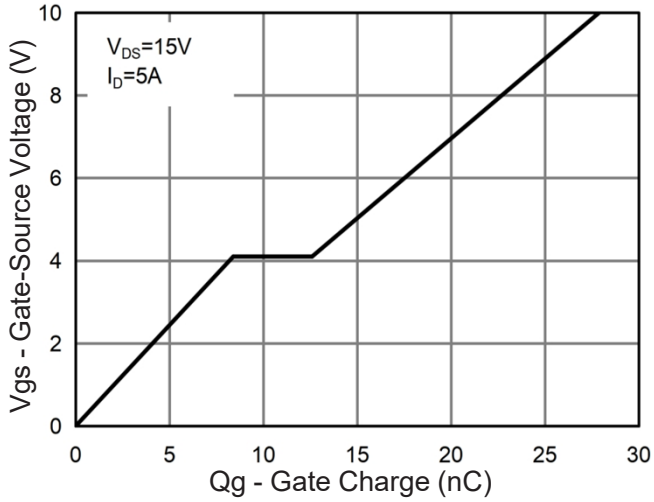



**Figure 5 Gate Charge**

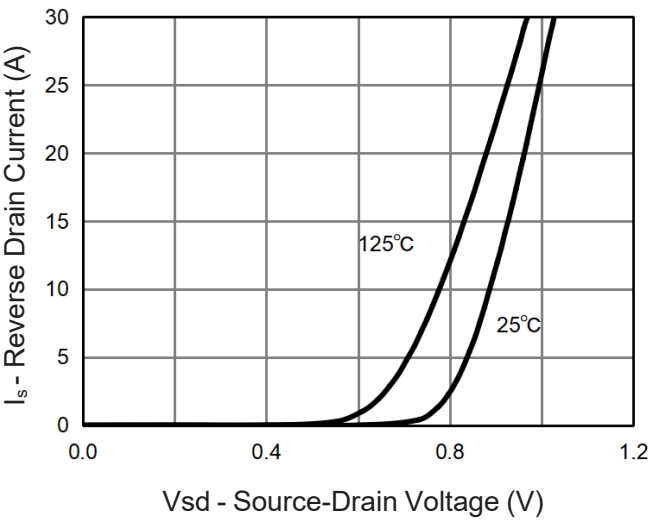



**Figure 6 Source-Drain Diode Forward**

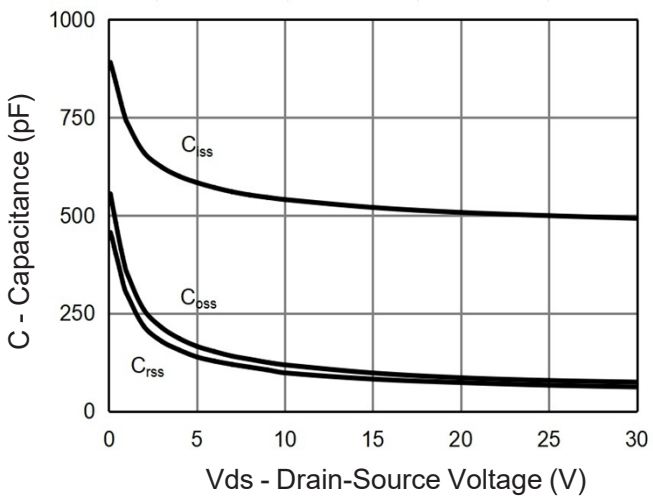



**Figure 7 Capacitance vs Vds**

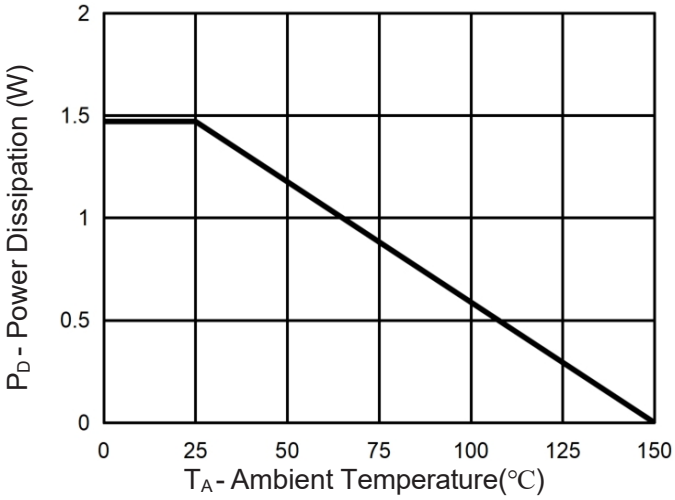



**Figure 9 Power De-rating**

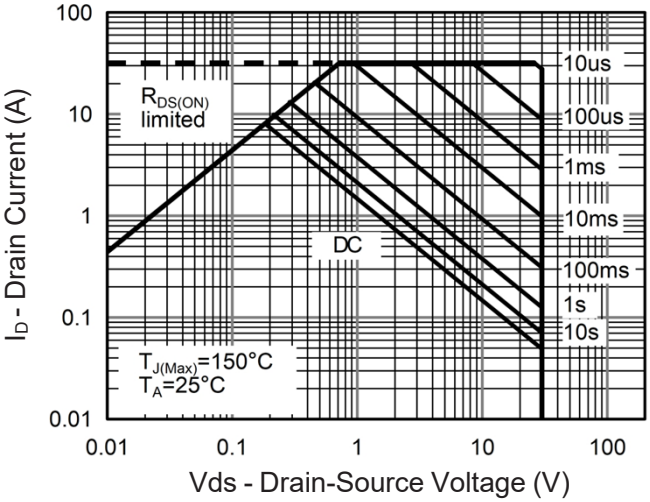



**Figure 8 Safe Operation Area**(Note 5)

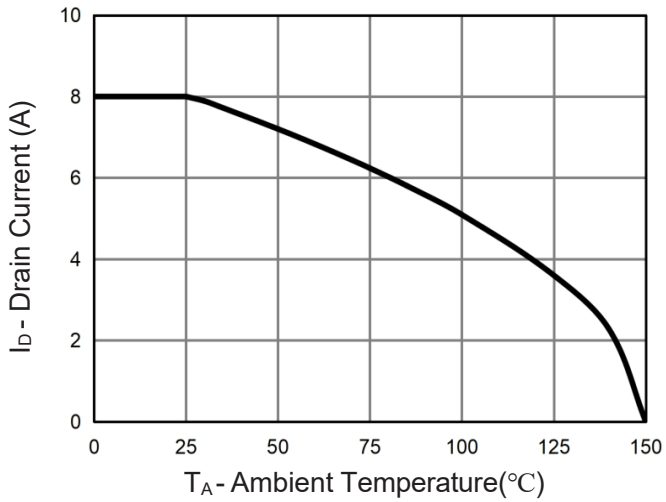



**Figure10 Drain Current De-rating**

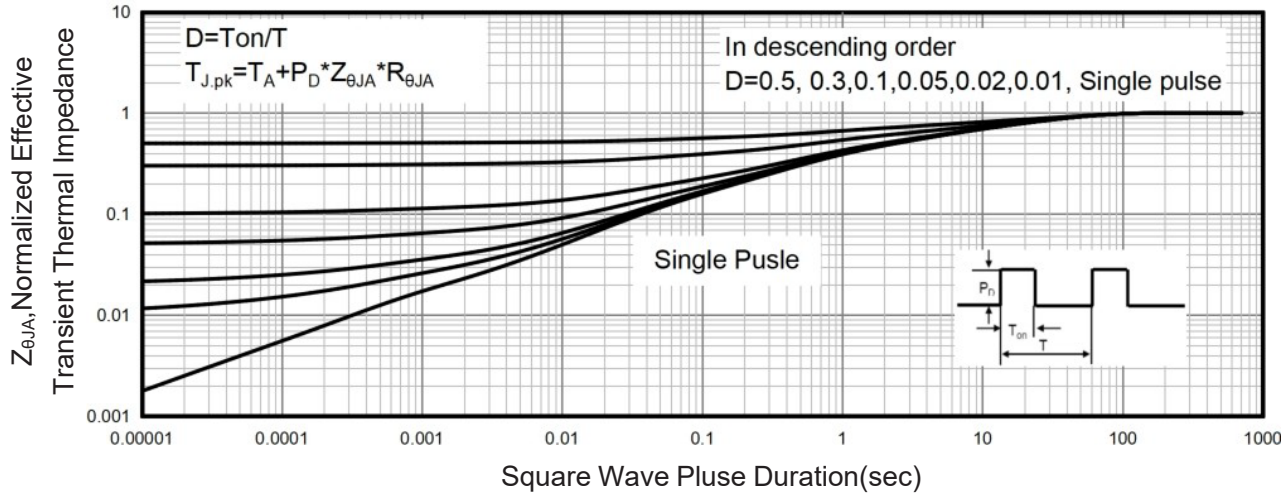



**Figure 11 Normalized Maximum Transient Thermal Impedance**