Description

The VSM50N60EY uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.It is ESD protected.

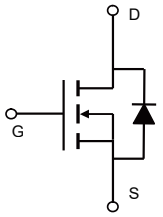
General Features

- V_{DS} =60V ,I_D =3.8A
  $R_{DS(ON)}$ < 55mΩ @ V_{GS}=10V
  $R_{DS(ON)}$ < 71mΩ @ V_{GS}=4.5V
  ESD Rating：2800V HBM
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

SOT-23



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM50N60EY	VSM50N60EY-S2	SOT-23	Ø180mm	8mm	3000units

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	3.8	A
Drain Current-Continuous(T_A=100℃)	I_D (100℃)	2.6	A
Pulsed Drain Current	I_{DM}	15.2	A
Maximum Power Dissipation	P_D	1.54	W
Derating factor		0.0124	W/℃
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Ambient (Note 1)	$R_{\theta JA}$	80.94	℃/W

Electrical Characteristics (T_A=25℃unless otherwise noted)

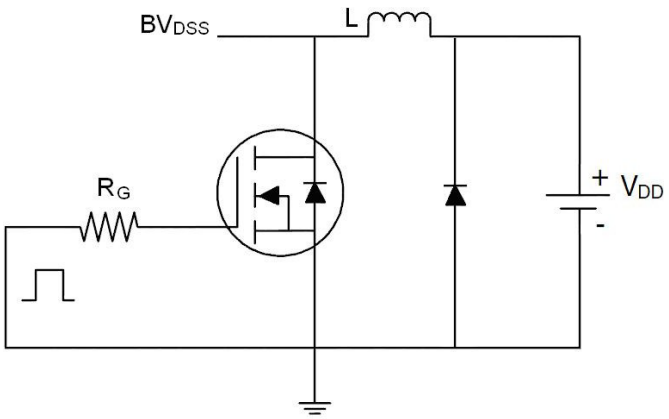
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±10	μA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.1	1.6	2.1	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=3A	-	48	55	mΩ
		V_{GS}=4.5V, I_D=3A	-	62	71	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=3A	-	12	-	S
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=30V,V_{GS}=0V, F=1.0MHz	-	617	-	pF
Output Capacitance	C_{oss}		-	43.4	-	pF
Reverse Transfer Capacitance	C_{rss}		-	35.7	-	pF
Switching Characteristics (Note 2)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=30V,R_L=0.5Ω, R_G=10Ω,V_{GS}=10V	-	7	-	nS
Turn-on Rise Time	t_r		-	11	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	26	-	nS
Turn-Off Fall Time	t_f		-	9	-	nS
Total Gate Charge	Q_g	I_D=3A,V_{DD}=30V,V_{GS}=10V	-	20	-	nC
Gate-Source Charge	Q_{gs}		-	2	-	nC
Gate-Drain Charge	Q_{gd}		-	4	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=3A	-	-	1.2	V
Diode Forward Current	I_S		-	-	3.5	A

Notes:

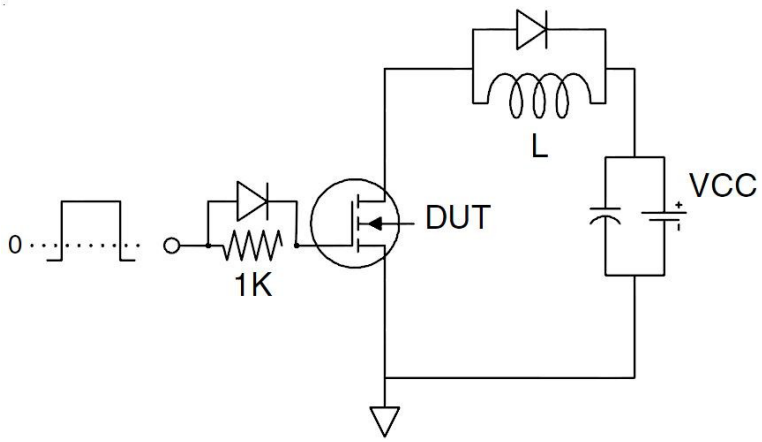
1. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it.
2. Guaranteed by design, not subject to production.
3. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

Test circuit

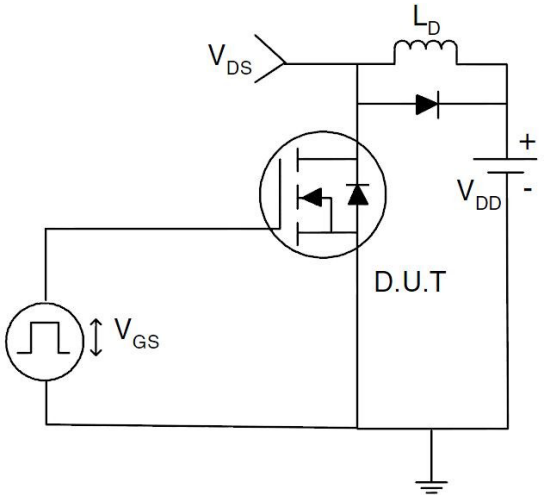
1） E_{AS} test Circuits



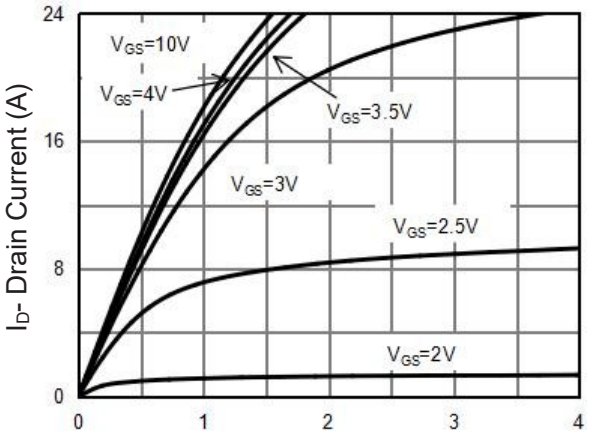
2） Gate charge test Circuit:



3） Switch Time Test Circuit：

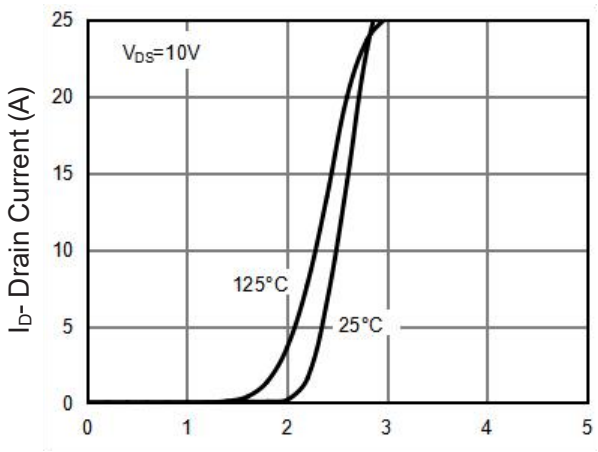


Typical Electrical and Thermal Characteristics (Curves)



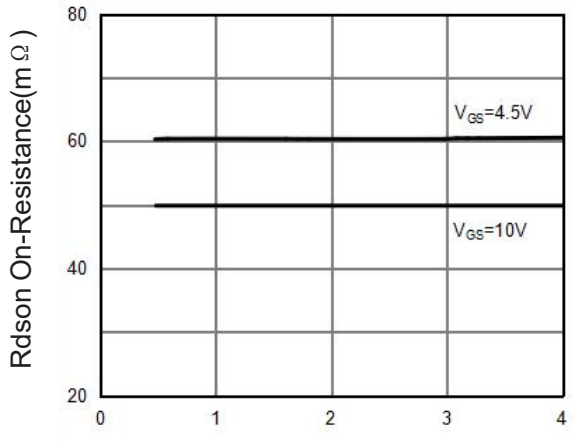
Vds Drain-Source Voltage (V)

Figure 1 Output Characteristics



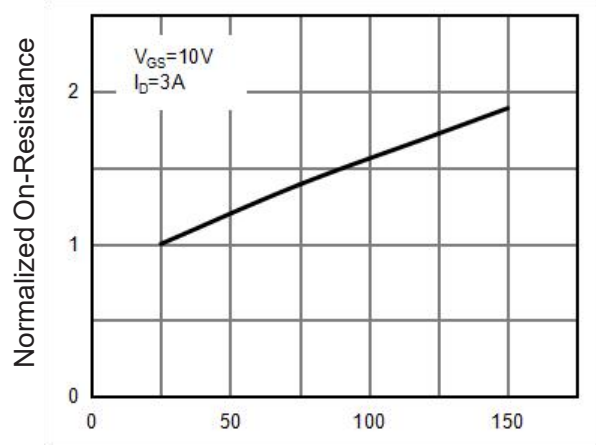
Vgs Gate-Source Voltage (V)

Figure 2 Transfer Characteristics



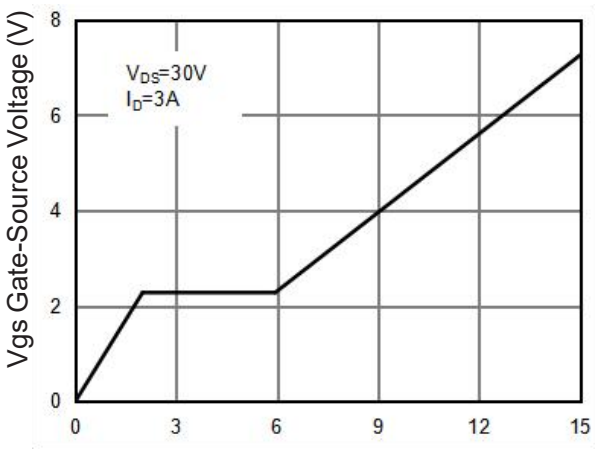
I_D- Drain Current (A)

Figure 3 Rdson- Drain Current



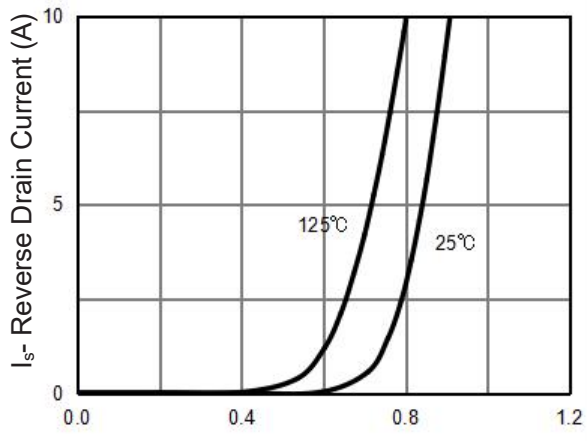
T_J-Junction Temperature(℃)

Figure 4 Rdson-JunctionTemperature



Qg Gate Charge (nC)

Figure 5 Gate Charge



Vsd Source-Drain Voltage (V)

Figure 6 Source- Drain Diode Forward

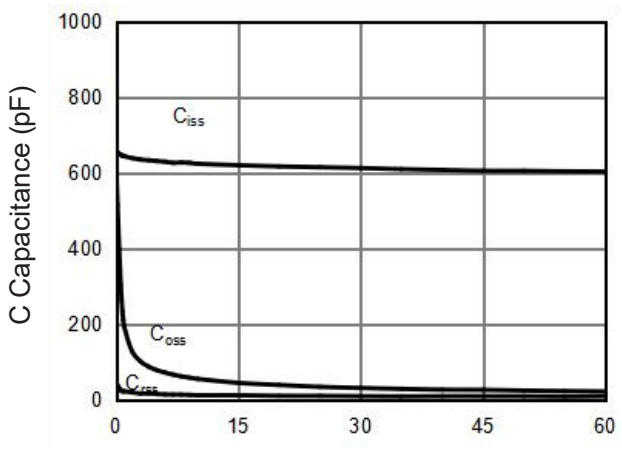


Figure 7 Capacitance vs Vds

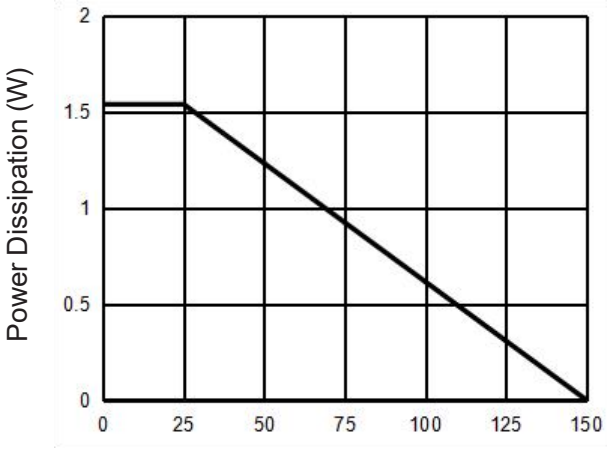


Figure 9 Power De-rating

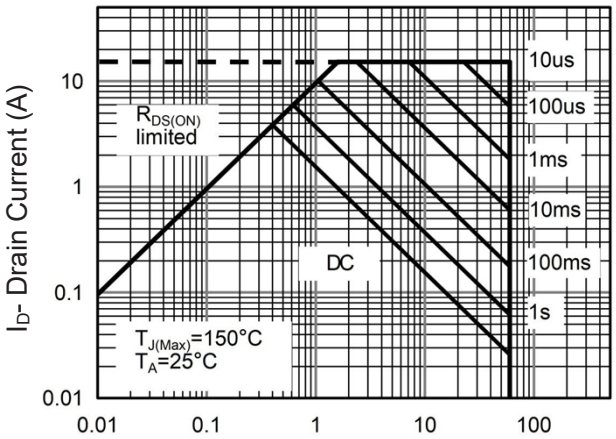


Figure 8 Safe Operation Area (Note 3)

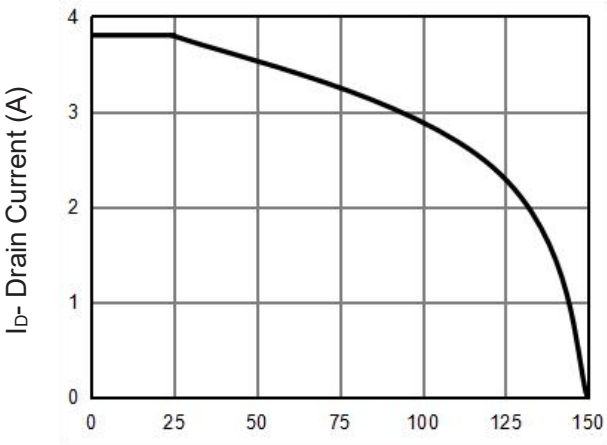


Figure 10 Current De-rating

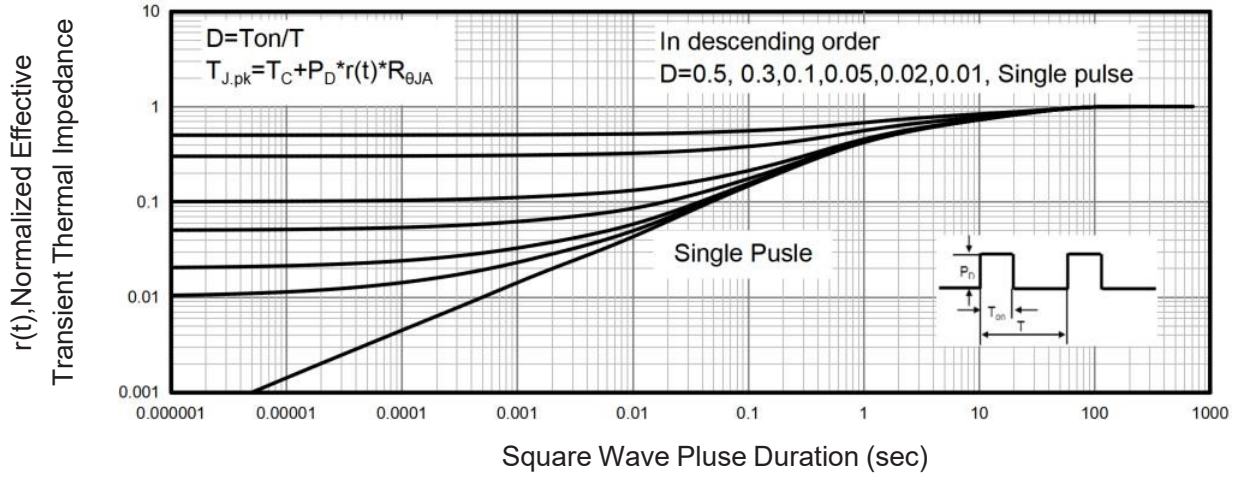


Figure 11 Normalized Maximum Transient Thermal Impedance