Description

The VSM130N07 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

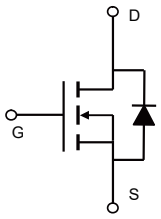
General Features

- V_{DS} = 75V,I_D =130A
  $R_{DS(ON)}$ <9 mΩ @ V_{GS}=10V (Typ:7.7mΩ)
- Special process technology for high ESD capability
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

TO-220



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM130N07	VSM130N07-TC	TO-220	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	75	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	130	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	92	A
Pulsed Drain Current	I_{DM}	520	A
Maximum Power Dissipation	P_D	300	W
Single pulse avalanche energy (Note 1)	E_{AS}	1936	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case	$R_{\theta JC}$	0.5	℃/W
Thermal Resistance,Junction-to-Ambient (Note 4)	$R_{\theta JA}$	40	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

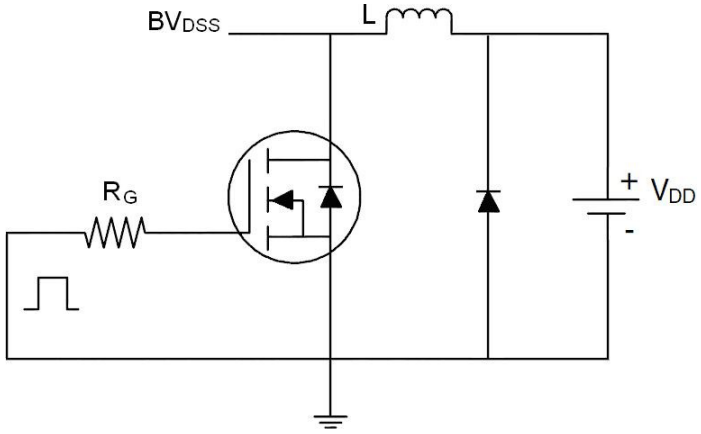
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	75	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=75V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	-	7.7	9	mΩ
Forward Transconductance	g_{FS}	V_{DS}=10V,I_D=20A	-	30	-	S
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=40V,V_{GS}=0V, F=1.0MHz	-	8404	-	PF
Output Capacitance	C_{oss}		-	846	-	PF
Reverse Transfer Capacitance	C_{rss}		-	288	-	PF
Switching Characteristics (Note 2)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=40V, R_L=1Ω V_{GS}=10V,R_{GEN}=3Ω	-	66	-	nS
Turn-on Rise Time	t_r		-	38	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	81	-	nS
Turn-Off Fall Time	t_f		-	16	-	nS
Total Gate Charge	Q_g	V_{DS}=40V,I_D=20A, V_{GS}=10V	-	123	-	nC
Gate-Source Charge	Q_{gs}		-	52	-	nC
Gate-Drain Charge	Q_{gd}		-	26	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=20A	-	-	1.2	V
Diode Forward Current	I_S	-	-	-	130	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF =40A di/dt = 100A/μs	-	72	-	nS
Reverse Recovery Charge	Qrr		-	210	-	nC

Notes:

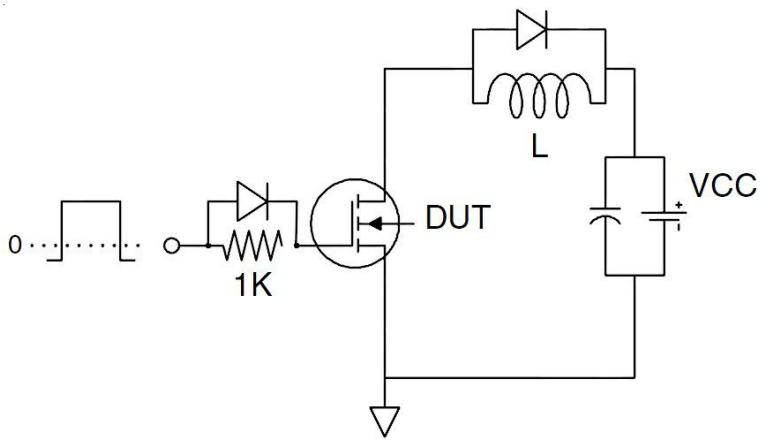
1. EAS condition : Tj=25℃,V_{DD}=15V,V_G=40V,L=0.5mH,Rg=25Ω
2. Guaranteed by design, not subject to production
3. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C. The SOA curve provides a single pulse rating.
4. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

Test circuit

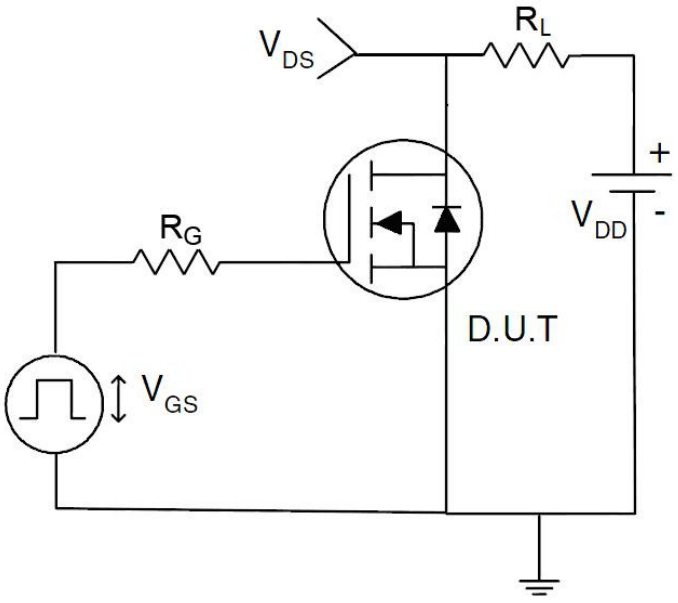
1) **E_{AS} test Circuit**



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

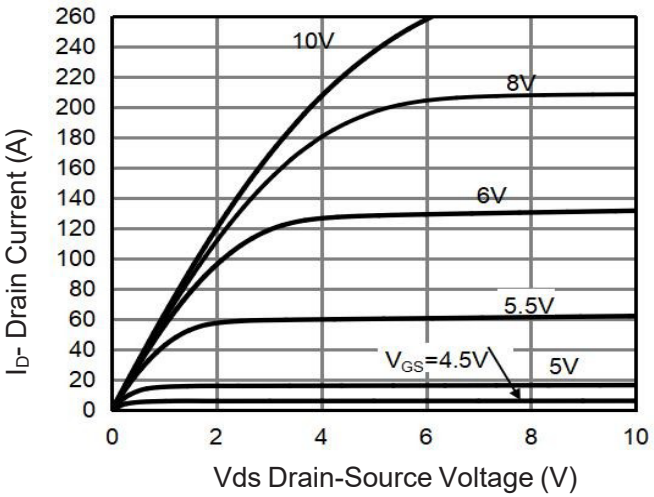


Figure 1 Output Characteristics

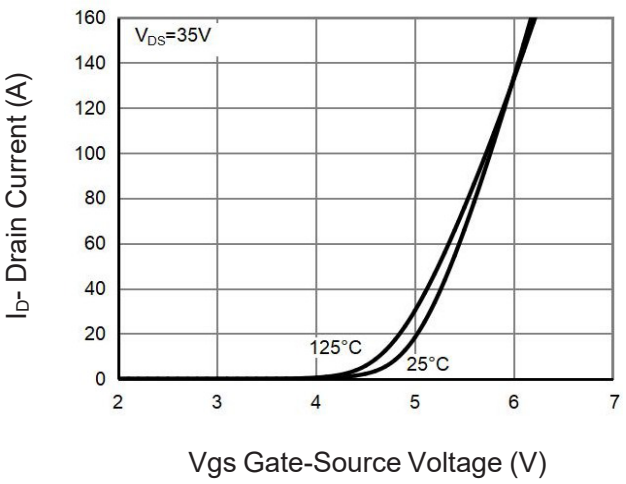


Figure 2 Transfer Characteristics

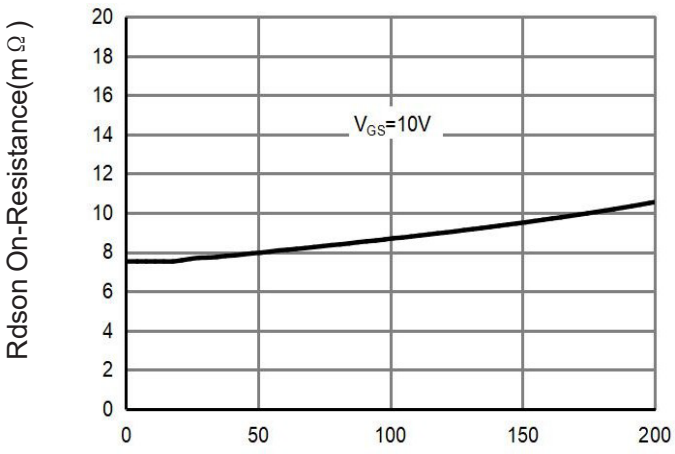


Figure 3 Rdson- Drain Current

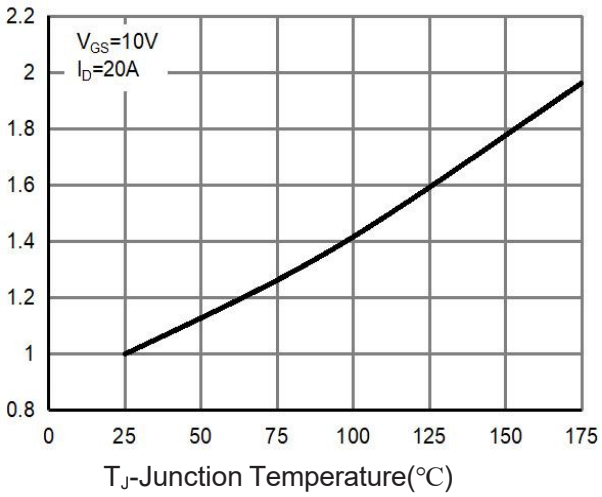


Figure 4 Rdson-JunctionTemperature

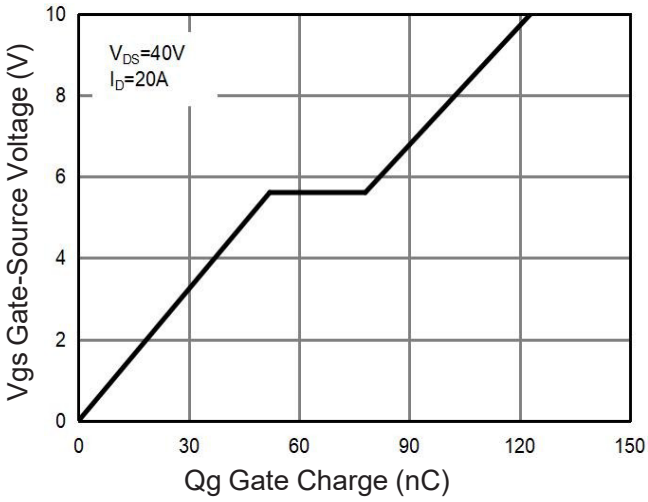


Figure 5 Gate Charge

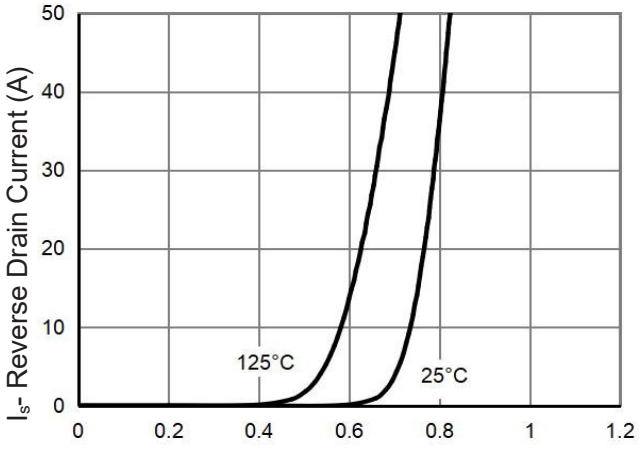


Figure 6 Source- Drain Diode Forward

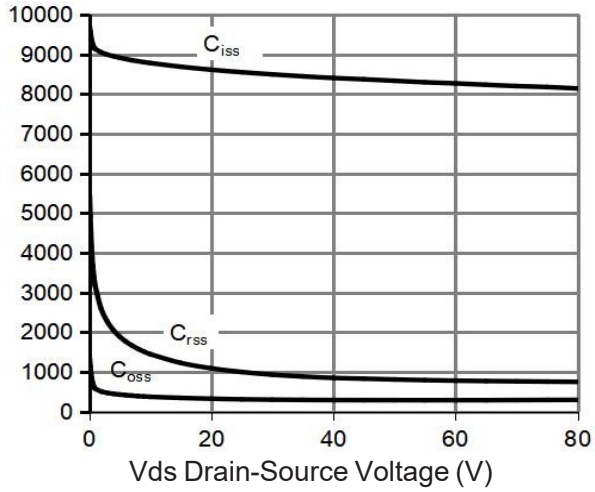


Figure 7 Capacitance vs Vds

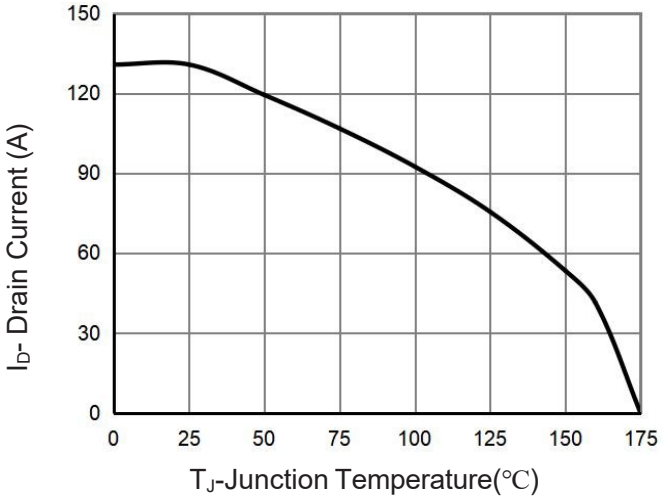


Figure 9 Current De-rating

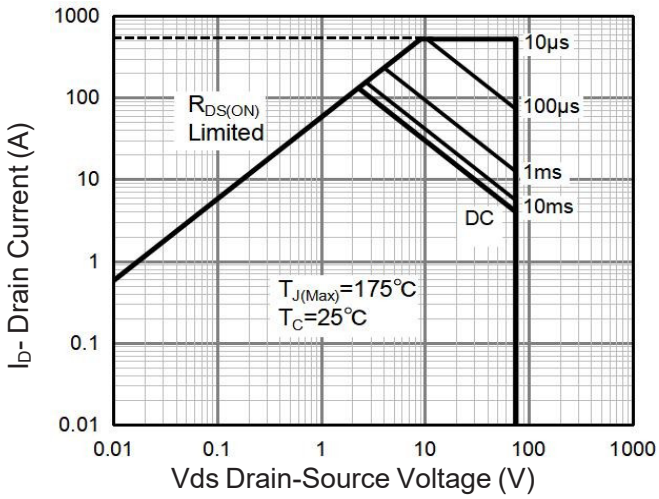


Figure 8 Safe Operation Area (Note3)

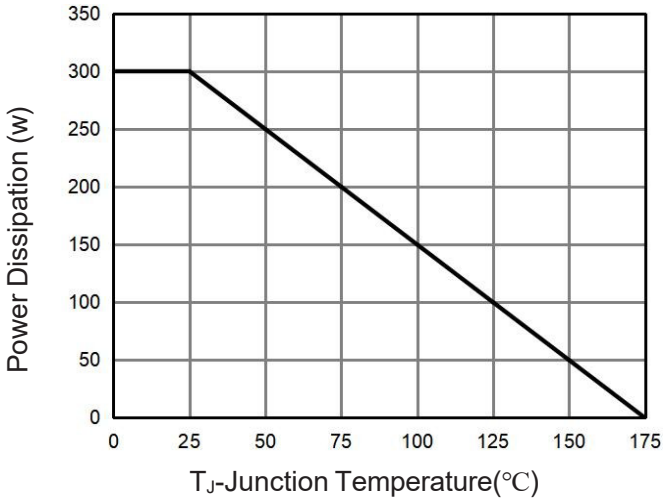


Figure 10 Power De-rating

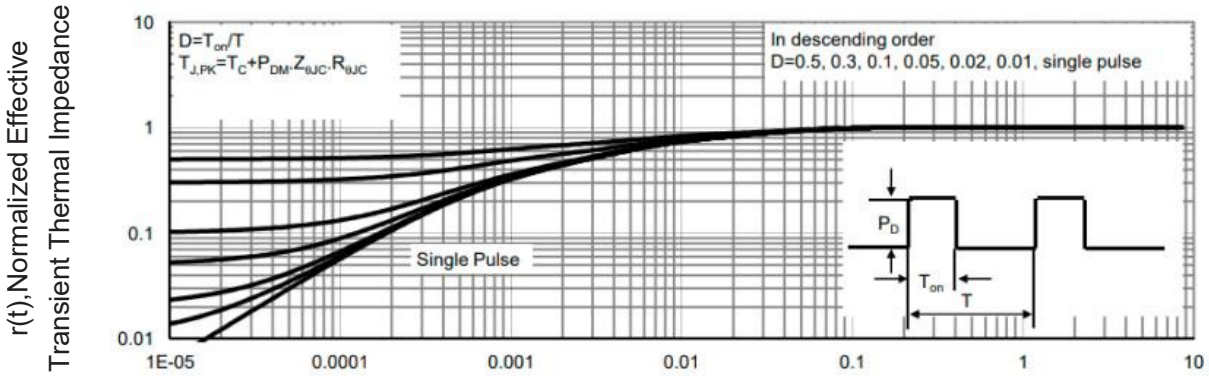


Figure 11 Normalized Maximum Transient Thermal Impedance