Description

The VSM165N04 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

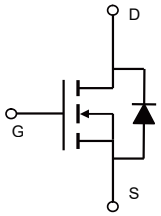
General Features

- V_{DS} =40V,I_D =165A
  $R_{DS(ON)}$ =2.1mΩ @ V_{GS}=10V (Typ)
  $R_{DS(ON)}$ =2.9mΩ @ V_{GS}=4.5V (Typ)
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

TO-220



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM165N04	VSM165N04-TC	TO-220	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	165	A
Pulsed Drain Current	I_{DM}	660	A
Maximum Power Dissipation	P_D	130	W
Single pulse avalanche energy (Note 5)	E_{AS}	1102	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case	$R_{\theta JC}$	1.154	℃/W
Thermal Resistance,Junction-to-Ambient(Note 2)	$R_{\theta JA}$	40	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.0	1.6	2.2	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	-	2.1	2.6	mΩ
		V_{GS}=4.5V, I_D=20A	-	2.9	3.8	
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=20A	-	40	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=20V,V_{GS}=0V, F=1.0MHz	-	6116	-	pF
Output Capacitance	C_{oss}		-	693	-	pF
Reverse Transfer Capacitance	C_{rss}		-	659	-	pF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=20V,I_D=20A V_{GS}=10V,R_G=6Ω	-	15	-	nS
Turn-on Rise Time	t_r		-	70	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	80	-	nS
Turn-Off Fall Time	t_f		-	30	-	nS
Total Gate Charge	Q_g	V_{DS}=20V,I_D=20A, V_{GS}=10V	-	155	-	nC
Gate-Source Charge	Q_{gs}		-	15	-	nC
Gate-Drain Charge	Q_{gd}		-	42	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=20A	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	165	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF = 40A di/dt = 100A/μs(Note3)	-	52	-	nS
Reverse Recovery Charge	Qrr		-	64	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.

2. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

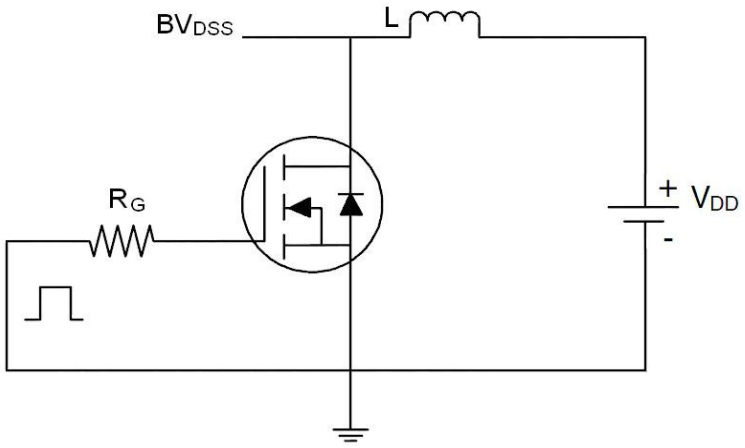
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

4. Guaranteed by design, not subject to production

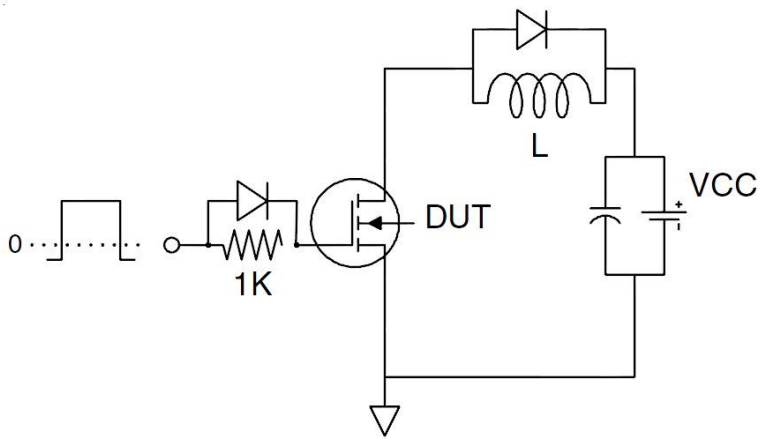
5. E_{AS} condition : Tj=25℃,V_{DD}=20V,V_G=10V,L=0.5mH,Rg=25Ω.

Test circuit

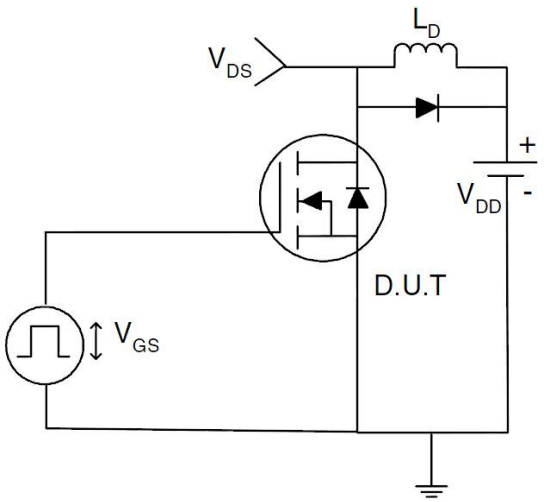
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

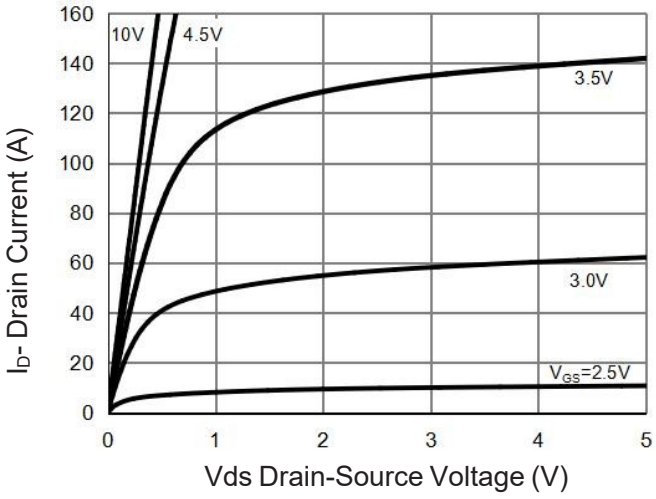


Figure 1 Output Characteristics

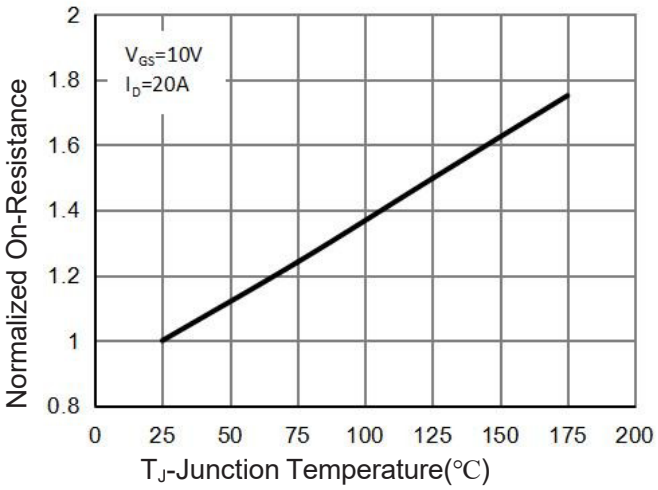


Figure 4 Rdson-JunctionTemperature

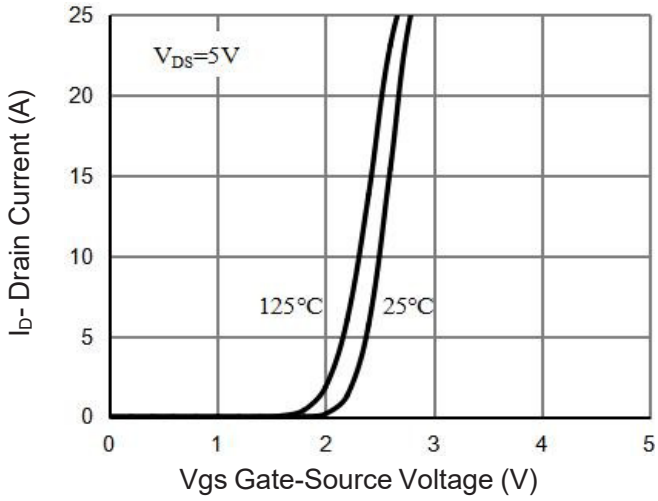


Figure 2 Transfer Characteristics

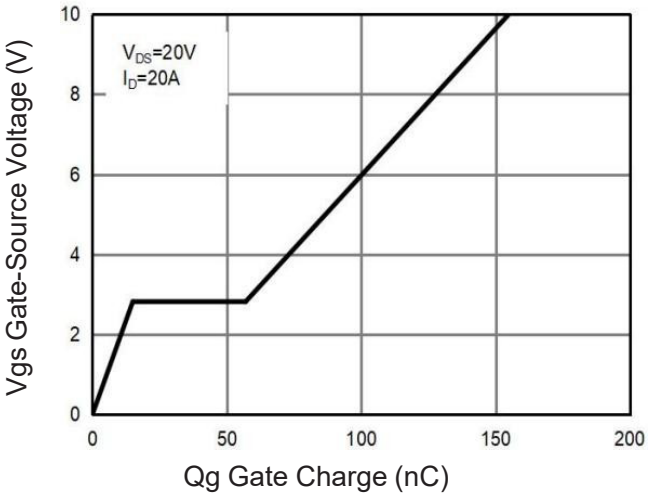


Figure 5 Gate Charge

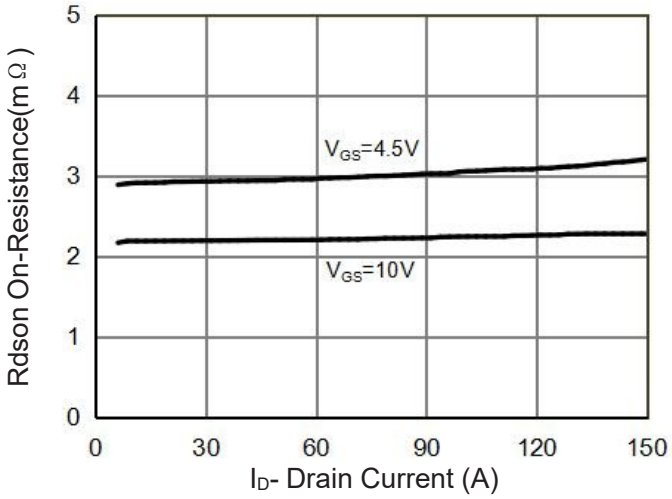


Figure 3 Rdson- Drain Current

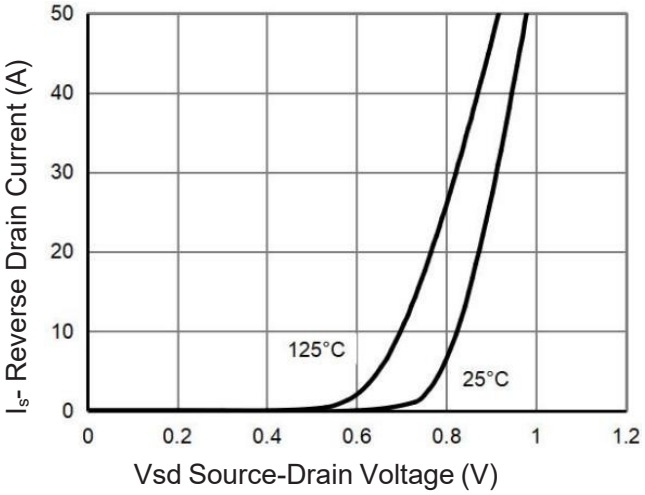


Figure 6 Source- Drain Diode Forward

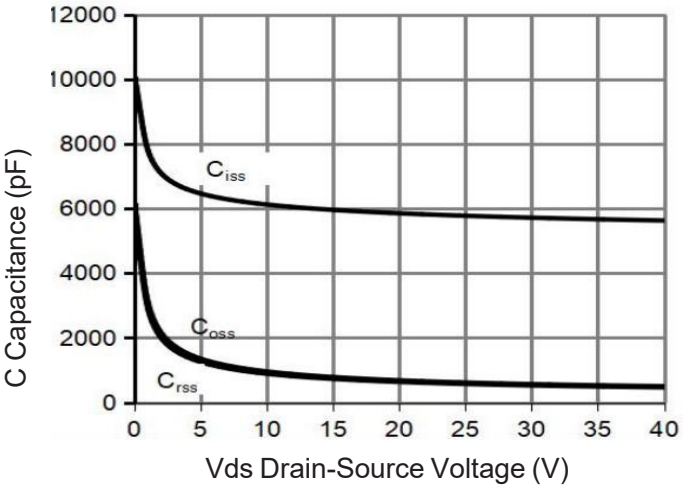


Figure 7 Capacitance vs Vds

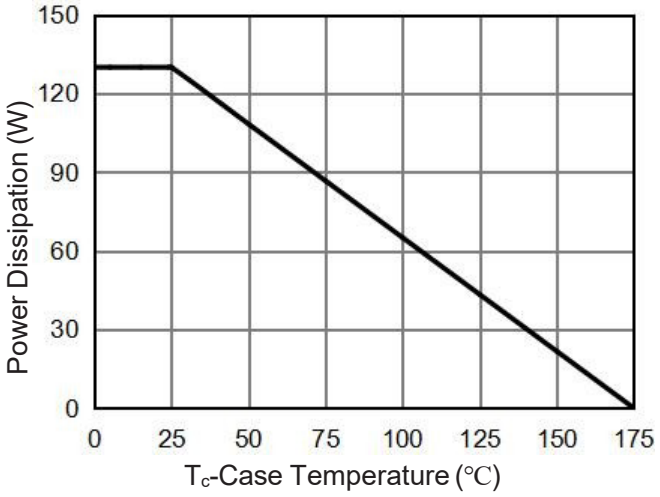


Figure 9 Power De-rating

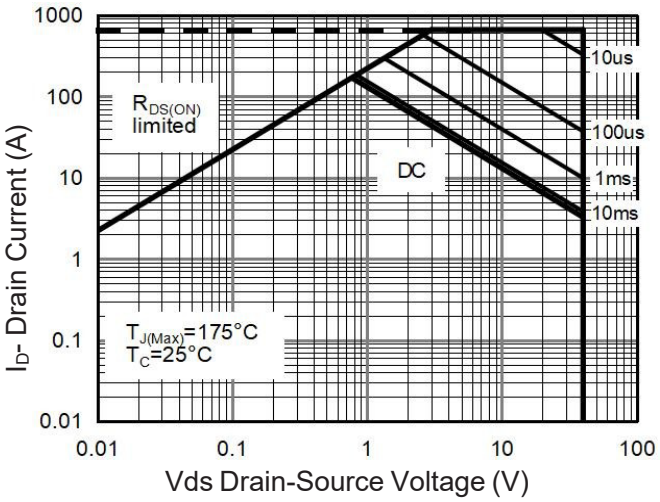


Figure 8 Safe Operation Area

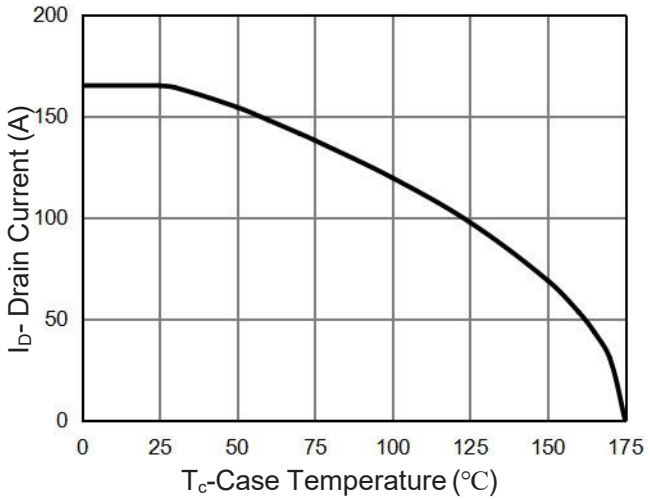


Figure 10 ID Current- JunctionTemperature

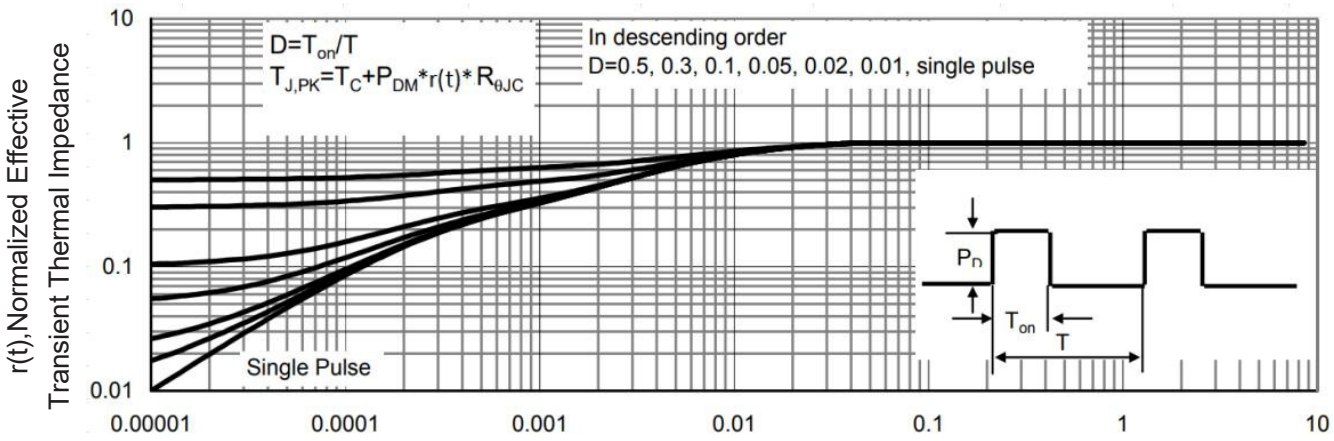


Figure 11 Normalized Maximum Transient Thermal Impedance