

Description

The VSM200N04 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

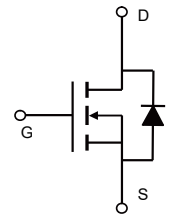
- $V_{DS} = 40V$, $I_D = 200A$
 $R_{DS(ON)} = 1.75m\Omega$ (typical) @ $V_{GS} = 10V$
 $R_{DS(ON)} = 2.7m\Omega$ (typical) @ $V_{GS} = 4.5V$
- High density cell design for ultra low $R_{DS(ON)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



TO-220



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM200N04	VSM200N04-TC	TO-220	-	-	-

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	200	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	189	A
Pulsed Drain Current	I_{DM}	800	A
Maximum Power Dissipation	P_D	280	W
Derating factor		1.87	W/ $^\circ C$
Single pulse avalanche energy (Note 5)	E_{AS}	2000	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	0.54	$^\circ C/W$
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Electrical Characteristics ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

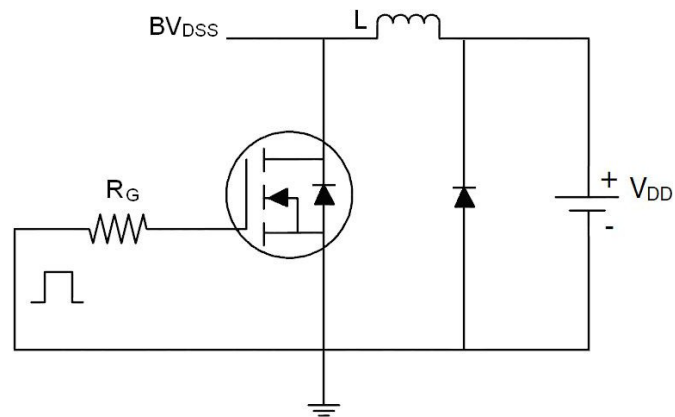
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.6	2.2	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=20A$	-	1.75	2.2	m Ω
		$V_{GS}=4.5V, I_D=20A$	-	2.7	3.6	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=20A$	-	40	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{iss}	$V_{DS}=20V, V_{GS}=0V,$ $F=1.0MHz$	-	10045	-	pF
Output Capacitance	C_{oss}		-	1058	-	pF
Reverse Transfer Capacitance	C_{rss}		-	931	-	pF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=20V, R_L=0.5\Omega,$ $R_G=3\Omega, V_{GS}=10V$	-	19	-	nS
Turn-on Rise Time	t_r		-	55	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	175	-	nS
Turn-Off Fall Time	t_f		-	38	-	nS
Total Gate Charge	Q_g	$I_D=20A, V_{DD}=20V, V_{GS}=10V$	-	213	-	nC
Gate-Source Charge	Q_{gs}		-	24.5	-	nC
Gate-Drain Charge	Q_{gd}		-	55	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=20A$	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	200	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}C, I_F = 40A$ $di/dt = 100A/\mu s^{(Note3)}$	-	46	-	nS
Reverse Recovery Charge	Q_{rr}		-	74	-	nC

Notes:

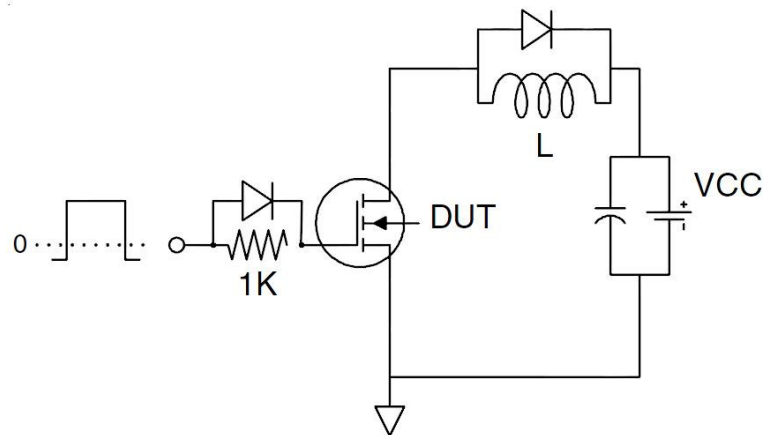
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=20V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test circuit

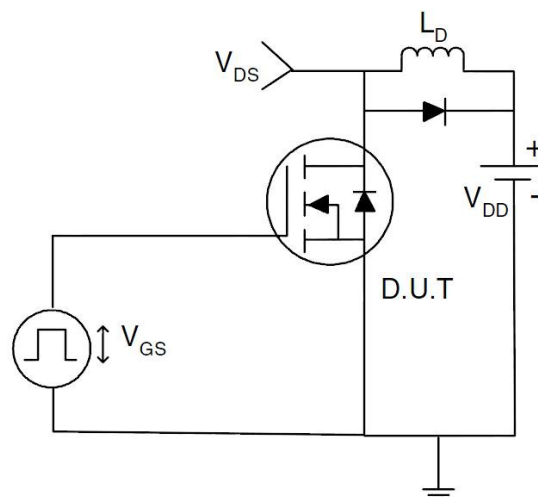
1) E_{AS} test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:



Typical Electrical and Thermal Characteristics (Curves)

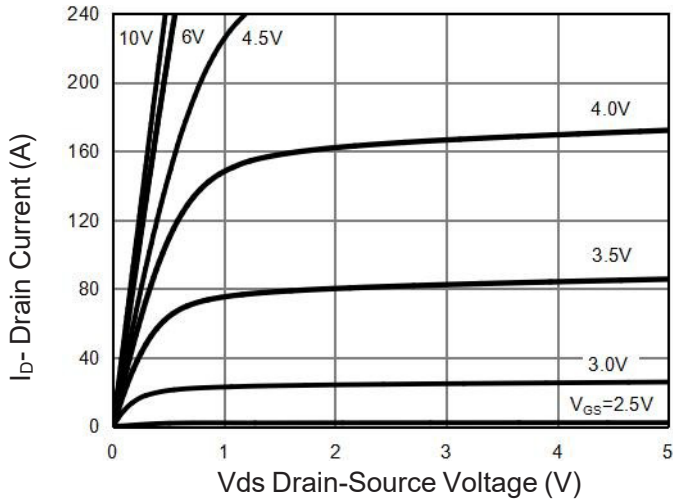


Figure 1 Output Characteristics

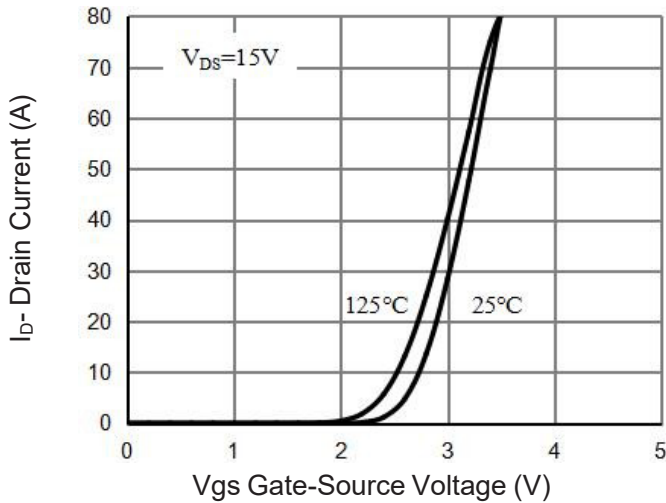


Figure 2 Transfer Characteristics

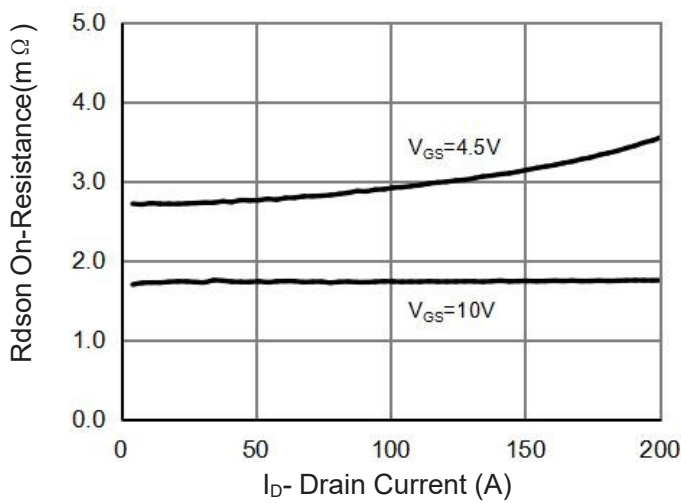


Figure 3 $R_{DS(on)}$ - Drain Current

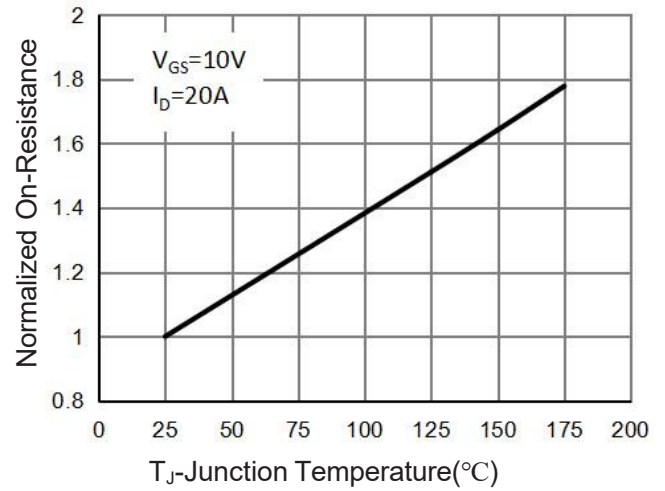


Figure 4 $R_{DS(on)}$ -Junction Temperature

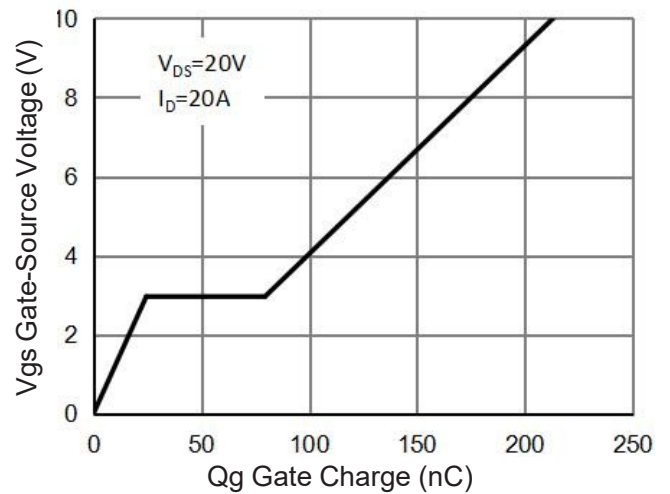


Figure 5 Gate Charge

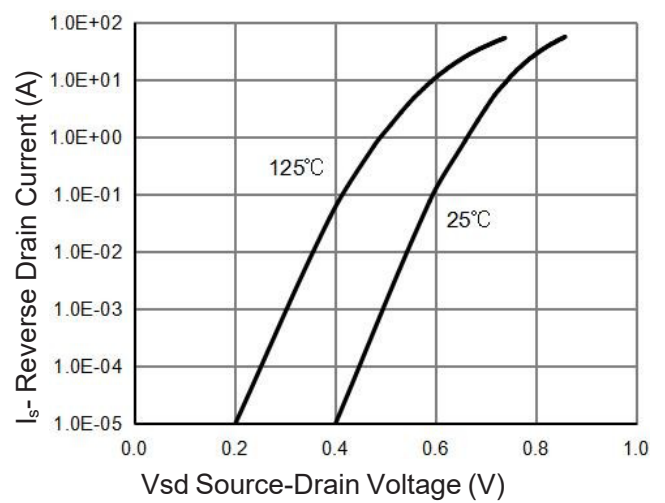
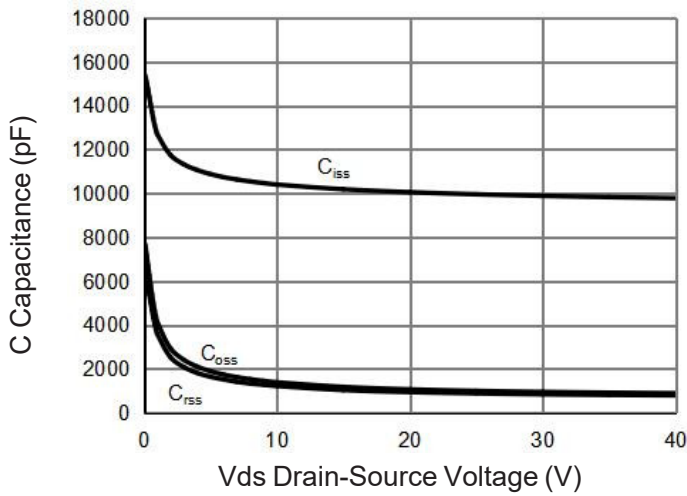
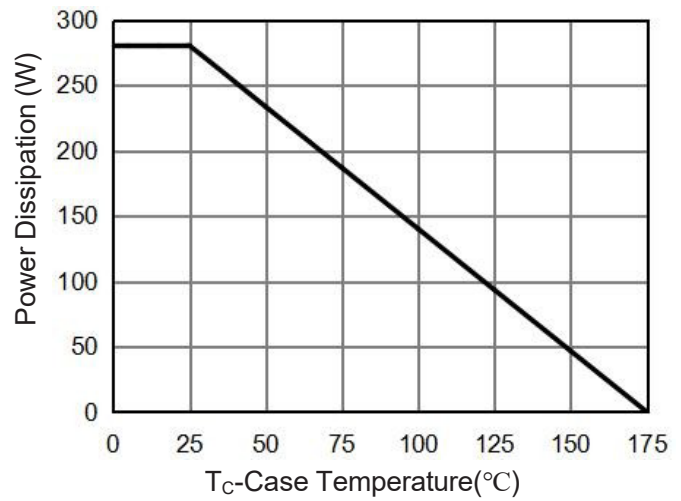
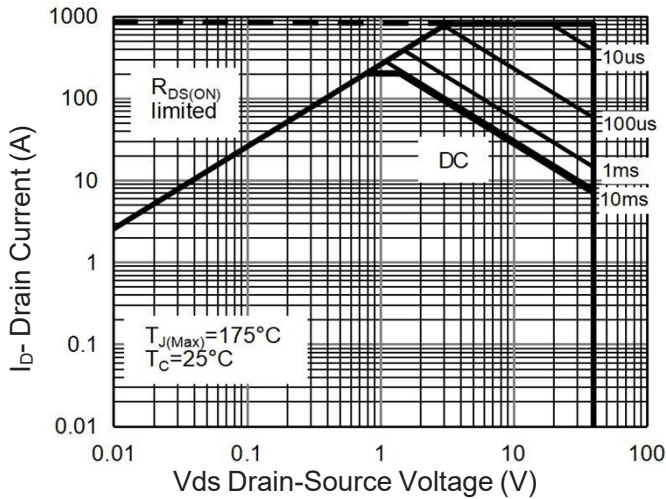
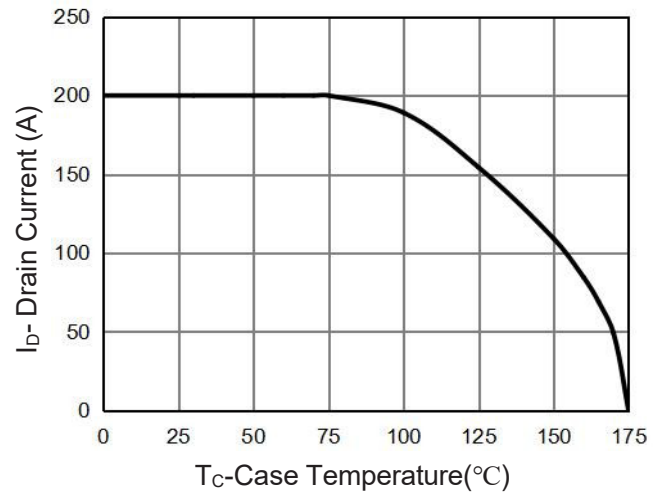
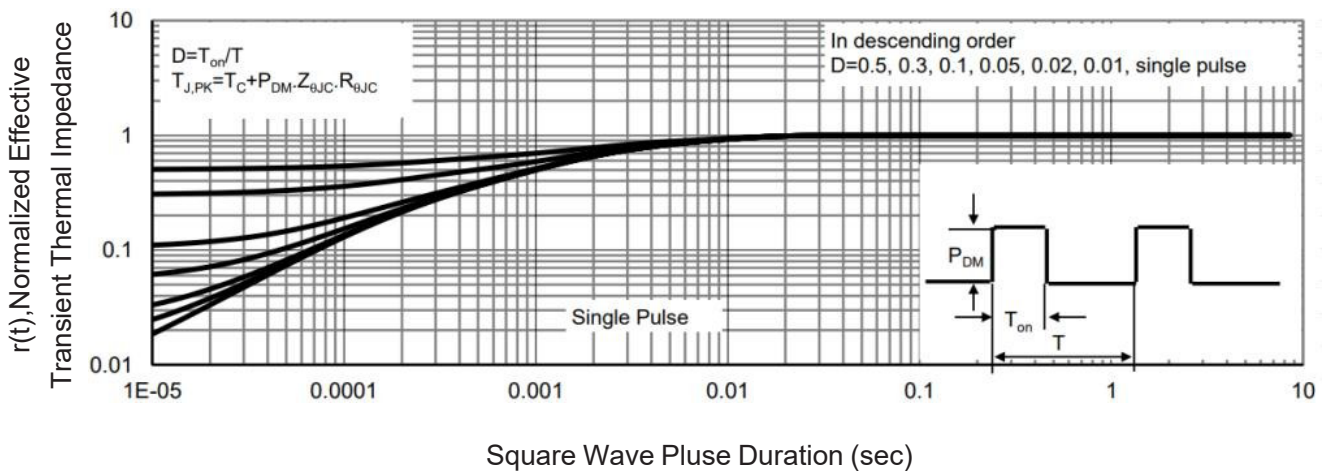


Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 Power De-rating

Figure 8 Safe Operation Area

Figure 10 Current De-rating

Figure 11 Normalized Maximum Transient Thermal Impedance