Description

The VSM350N04 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

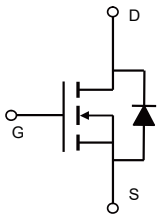
General Features

- V_{DS} = 40V,I_D = 350A
  $R_{DS(ON)}$ < 2.4mΩ @ V_{GS}=10V (Typ: 1.9mΩ)
- Excellent logic level drive capability
- High density cell design for ultra low $R_{DS(ON)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Power switching applications
- Hard switched and high frequency circuits
- Uninterruptible power supply

TO-220



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM350N04	VSM350N04-TC	TO-220	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	350	A
Drain Current-Continuous(100℃)	I_D (100℃)	248	A
Pulsed Drain Current (T_C=25℃)	I_{DM}	1400	A
Maximum Power Dissipation	P_D	576	W
Derating factor		3.846	W/℃
Single pulse avalanche energy (Note 1)	E_{AS}	3844	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case	$R_{\theta JC}$	0.26	℃/W

Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	40	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

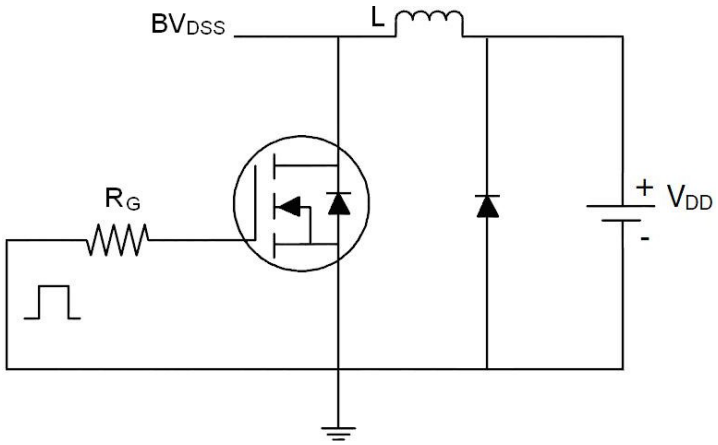
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.3	1.9	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=200A	-	1.9	2.4	mΩ
Forward Transconductance	g_{FS}	V_{DS}=10V,I_D=200A	-	75	-	S
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=20V,V_{GS}=0V, F=1.0MHz	-	10740	-	pF
Output Capacitance	C_{oss}		-	1643	-	pF
Reverse Transfer Capacitance	C_{rss}		-	730	-	pF
Switching Characteristics (Note 3)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=20V,R_L=0.5Ω, V_{GS}=10V,R_{GEN}=3Ω	-	20	-	nS
Turn-on Rise Time	t_r		-	55	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	175	-	nS
Turn-Off Fall Time	t_f		-	38	-	nS
Total Gate Charge	Q_g	V_{DS}=20V,I_D=200A, V_{GS}=10V	-	196.7	-	nC
Gate-Source Charge	Q_{gs}		-	39.3	-	nC
Gate-Drain Charge	Q_{gd}		-	31.4	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=200A	-	-	1.2	V
Diode Forward Current	I_S		-	-	350	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, I_F = 200A di/dt = 100A/μs	-	60	-	nS
Reverse Recovery Charge	Qrr		-	120	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

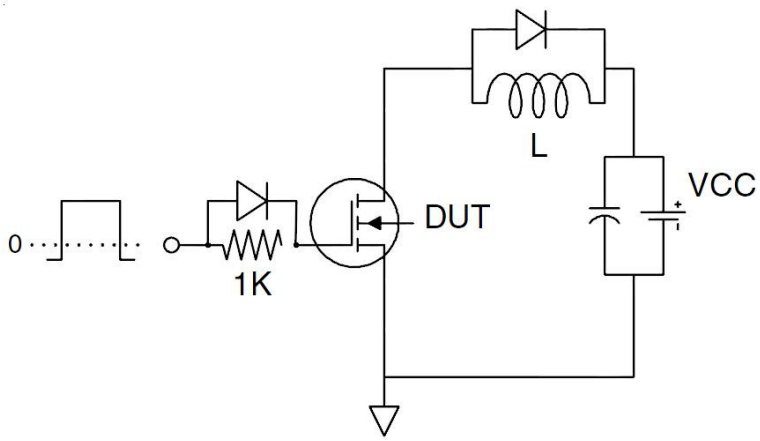
1. EAS condition : Tj=25℃,V_{DD}=20V,V_G=15V,L=0.5mH,Rg=25Ω.
2. The value of $R_{\theta JA}$ is measured in a still air environment with T_A =25°C. The maximum allowed junction temperature of 175°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.
3. Guaranteed by design, not subject to production.
4. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C. The SOA curve provides a single pulse rating.

Test Circuit

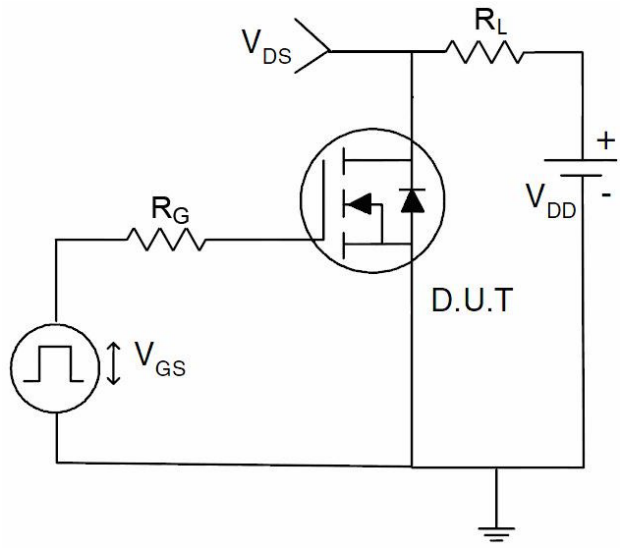
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

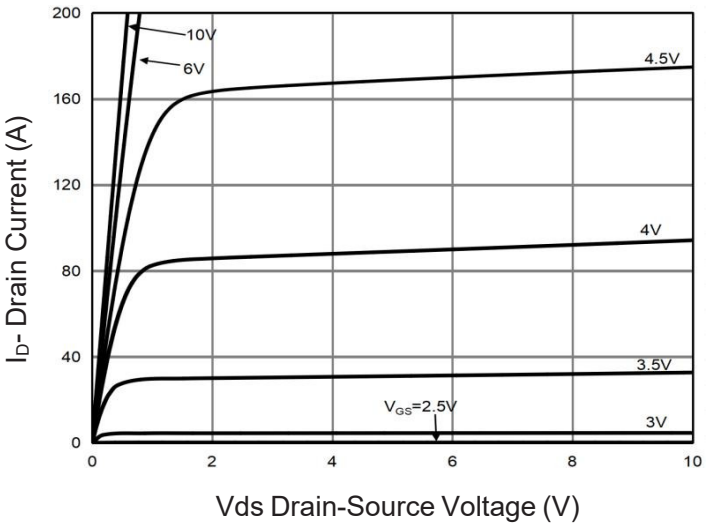


Figure 1 Output Characteristics

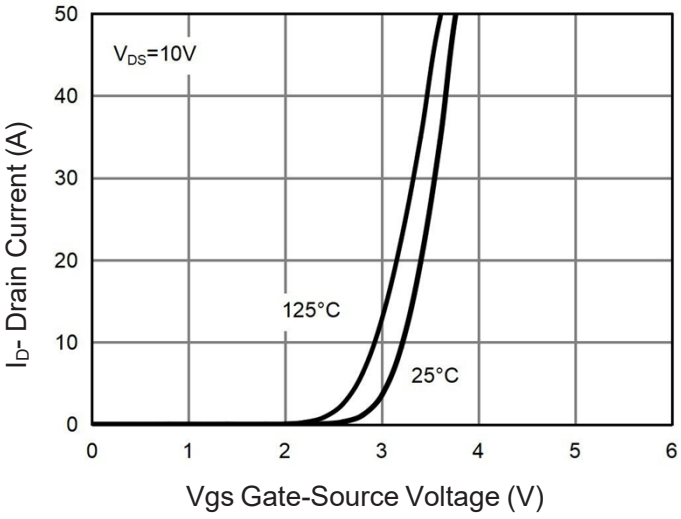


Figure 2 Transfer Characteristics

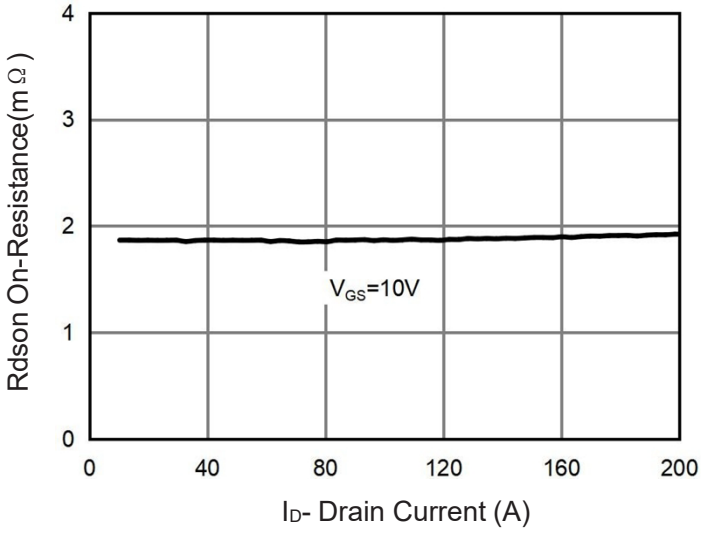


Figure 3 Rdson- Drain Current

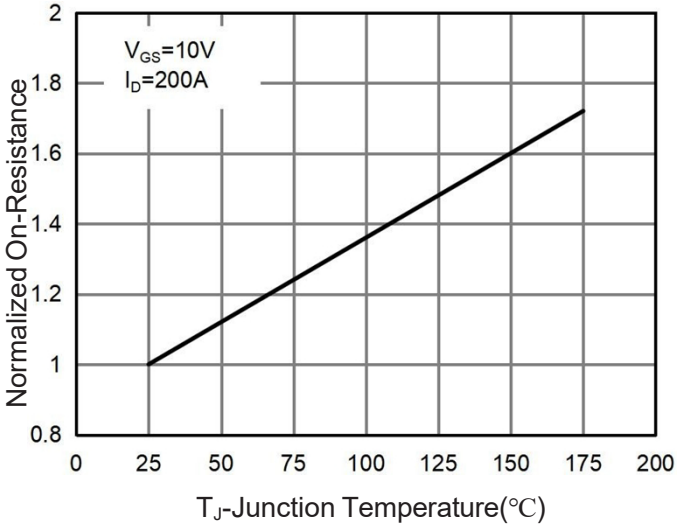


Figure 4 Rdson-JunctionTemperature

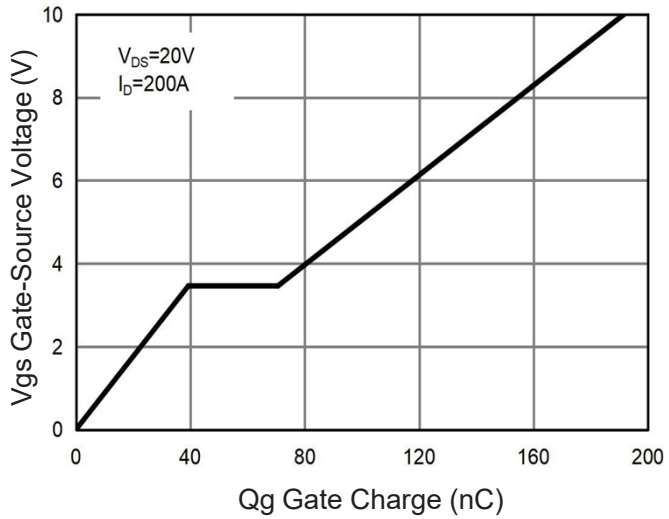


Figure 5 Gate Charge

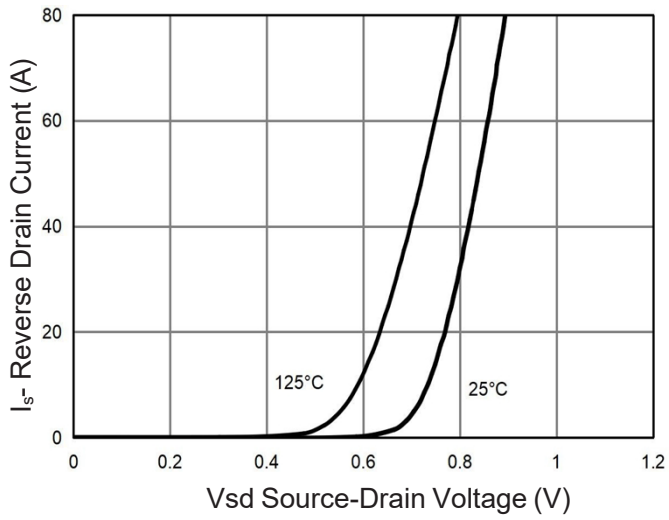


Figure 6 Source- Drain Diode Forward

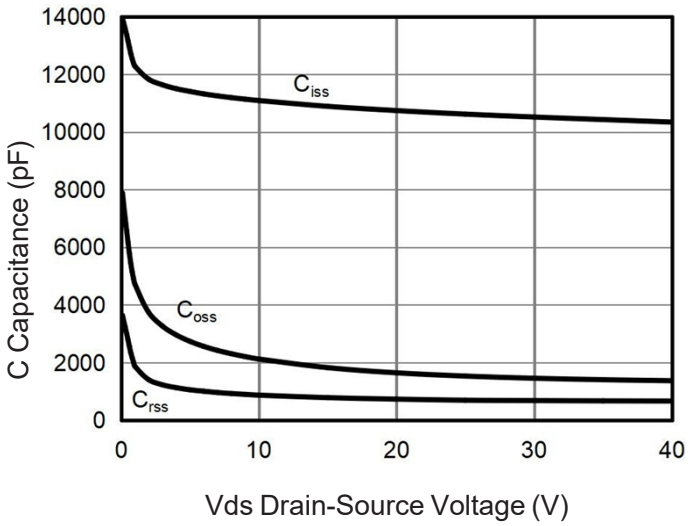


Figure 7 Capacitance vs Vds

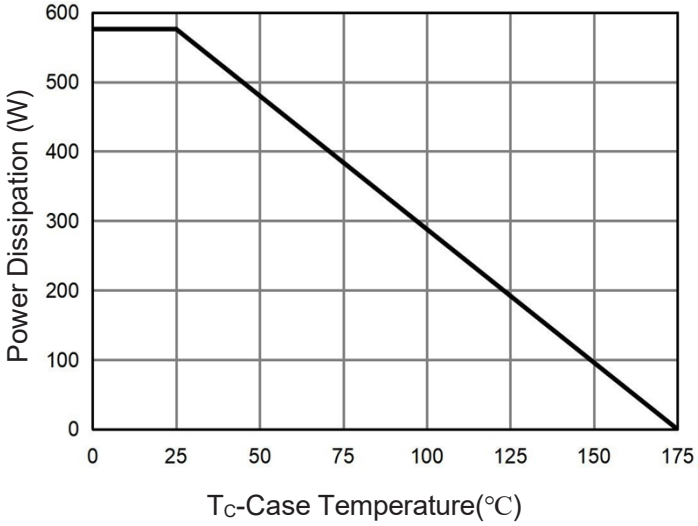


Figure 9 Power De-rating

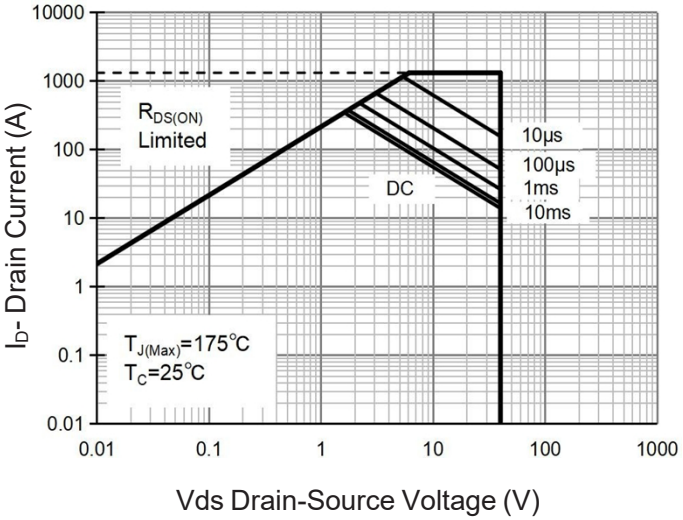


Figure 8 Safe Operation Area (Note 4)

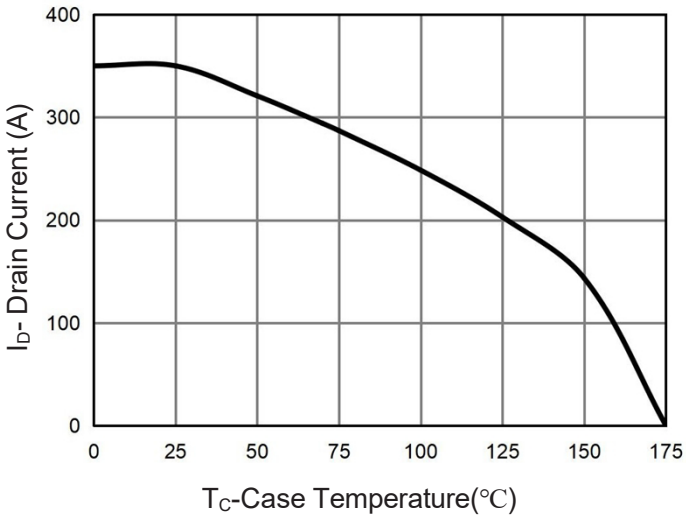


Figure10 Drain Current De-rating

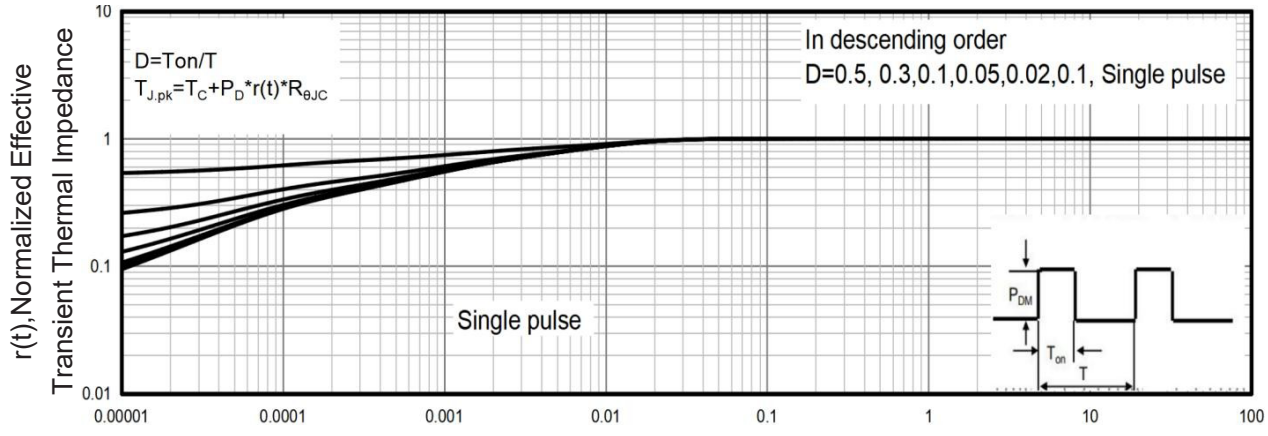


Figure 11 Normalized Maximum Transient Thermal Impedance