

Description

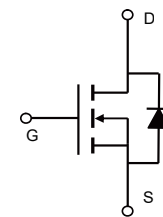
The VSM59N10 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

- $V_{DS} = 100V, I_D = 59A$
 $R_{DS(ON)} < 15m\Omega @ V_{GS}=10V$ (Typ:11m Ω)
- Special process technology for high ESD capability
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM59N10	VSM59N10-TC	TO-220	-	-	-

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	59	A
Drain Current-Continuous($T_C=100^{\circ}C$)	$I_D(100^{\circ}C)$	42	A
Pulsed Drain Current	I_{DM}	240	A
Maximum Power Dissipation	P_D	180	W
Derating factor		1.2	W/ $^{\circ}C$
Single pulse avalanche energy (Note 5)	E_{AS}	580	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^{\circ}C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.83	$^{\circ}\text{C/W}$
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

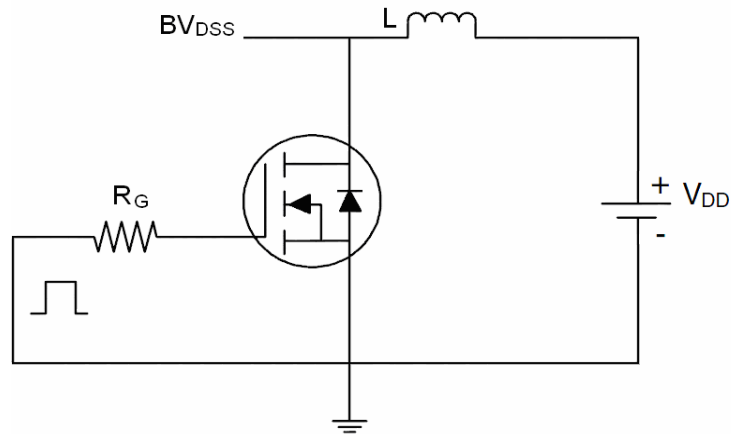
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	100	110	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2	3	4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =28A	-	11	15	mΩ
Forward Transconductance	g _{FS}	V _{DS} =25V, I _D =28A	32	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{ISS}	V _{DS} =25V, V _{GS} =0V, F=1.0MHz	-	4900	-	PF
Output Capacitance	C _{OSS}		-	400	-	PF
Reverse Transfer Capacitance	C _{rss}		-	390	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =50V, I _D =28A V _{GS} =10V, R _{GEN} =2.5Ω	-	12	-	nS
Turn-on Rise Time	t _r		-	55	-	nS
Turn-Off Delay Time	t _{d(off)}		-	45	-	nS
Turn-Off Fall Time	t _f		-	47	-	nS
Total Gate Charge	Q _g	V _{DS} =80V, I _D =28A, V _{GS} =10V	-	95	-	nC
Gate-Source Charge	Q _{gs}		-	18	-	nC
Gate-Drain Charge	Q _{gd}		-	25	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =59A	-	0.85	1.2	V
Diode Forward Current (Note 2)	I _S	-	-	-	59	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 59A di/dt = 100A/μs (Note3)	-	37	-	nS
Reverse Recovery Charge	Q _{rr}		-	58	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

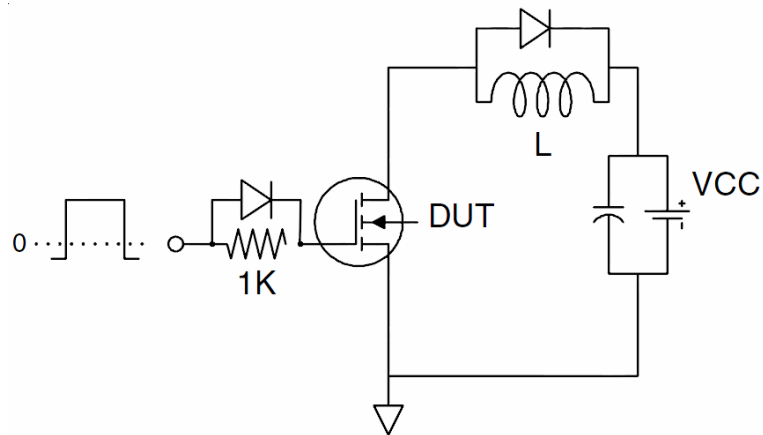
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test Circuit

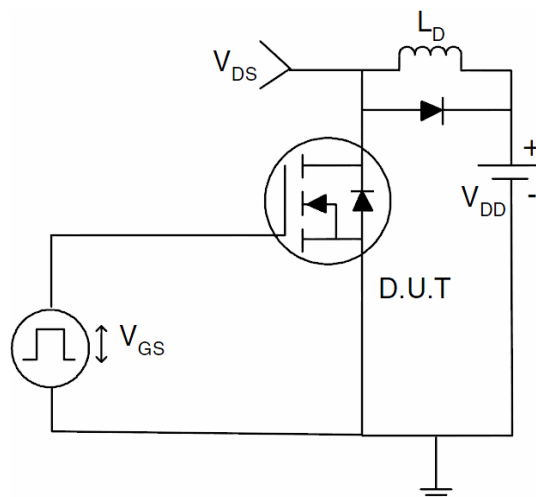
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

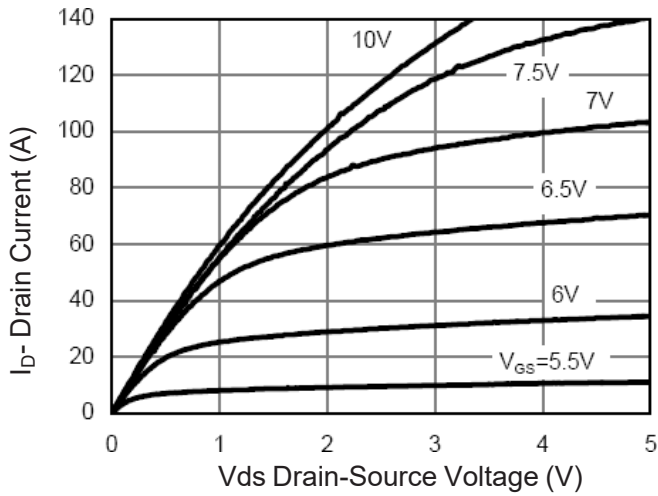


Figure 1 Output Characteristics

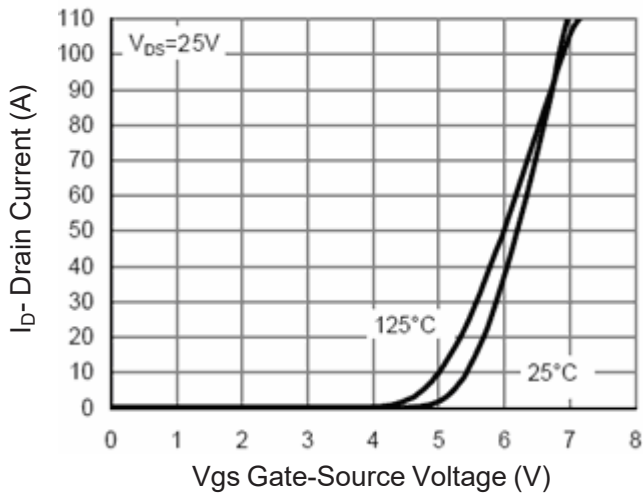


Figure 2 Transfer Characteristics

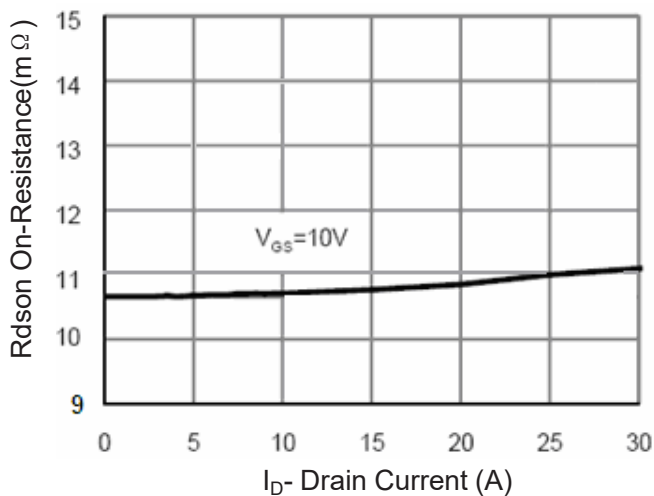


Figure 3 $R_{DS(on)}$ - Drain Current

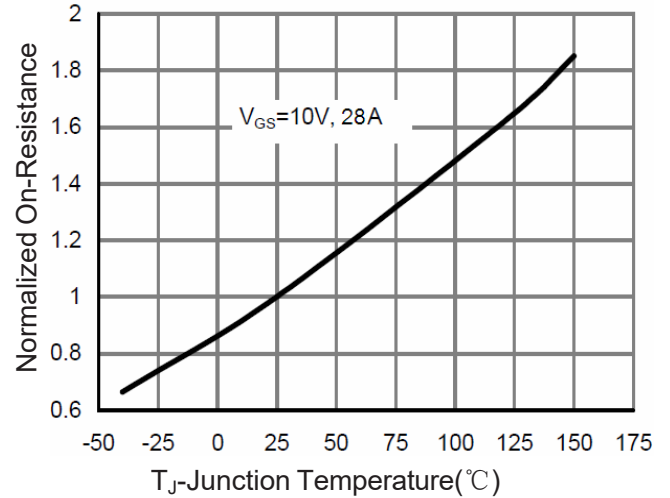


Figure 4 $R_{DS(on)}$ -Junction Temperature

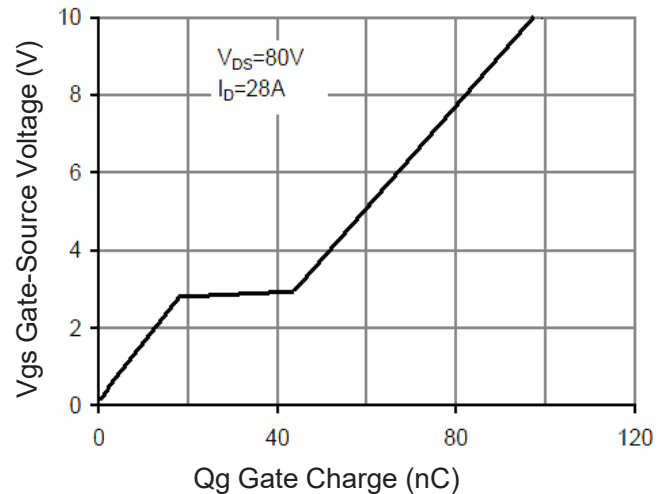


Figure 5 Gate Charge

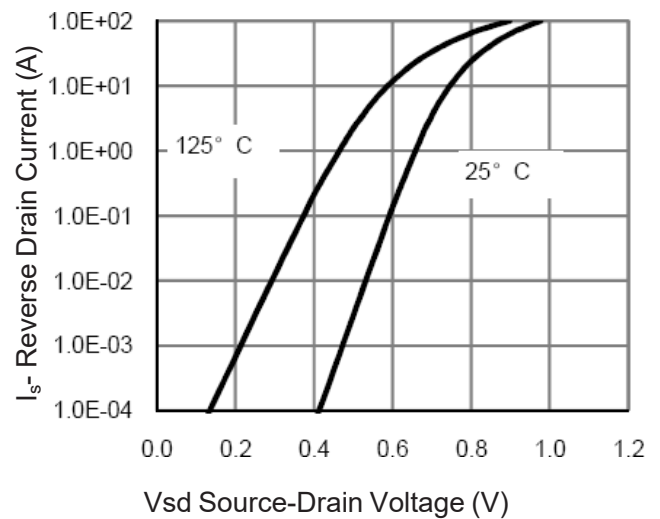
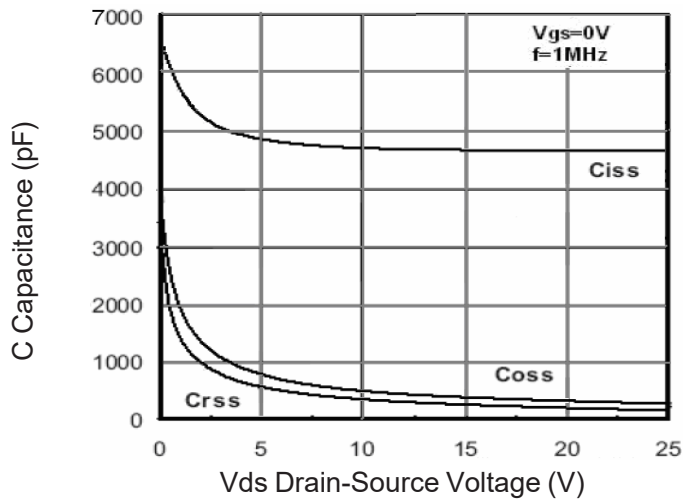
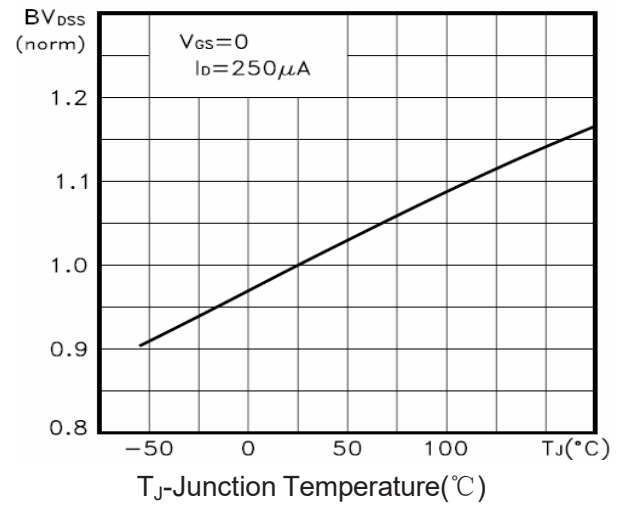
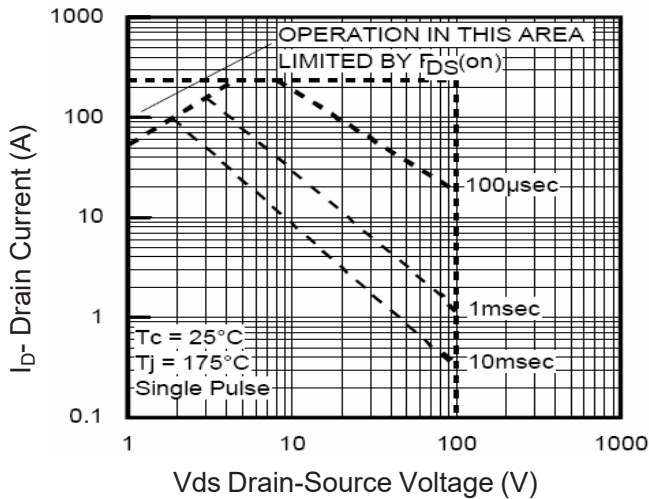
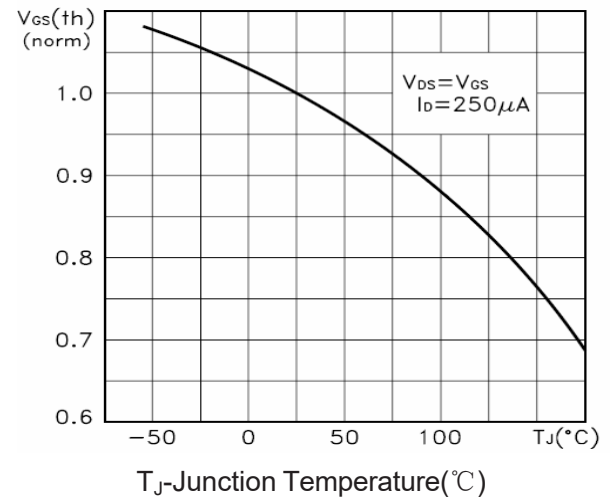
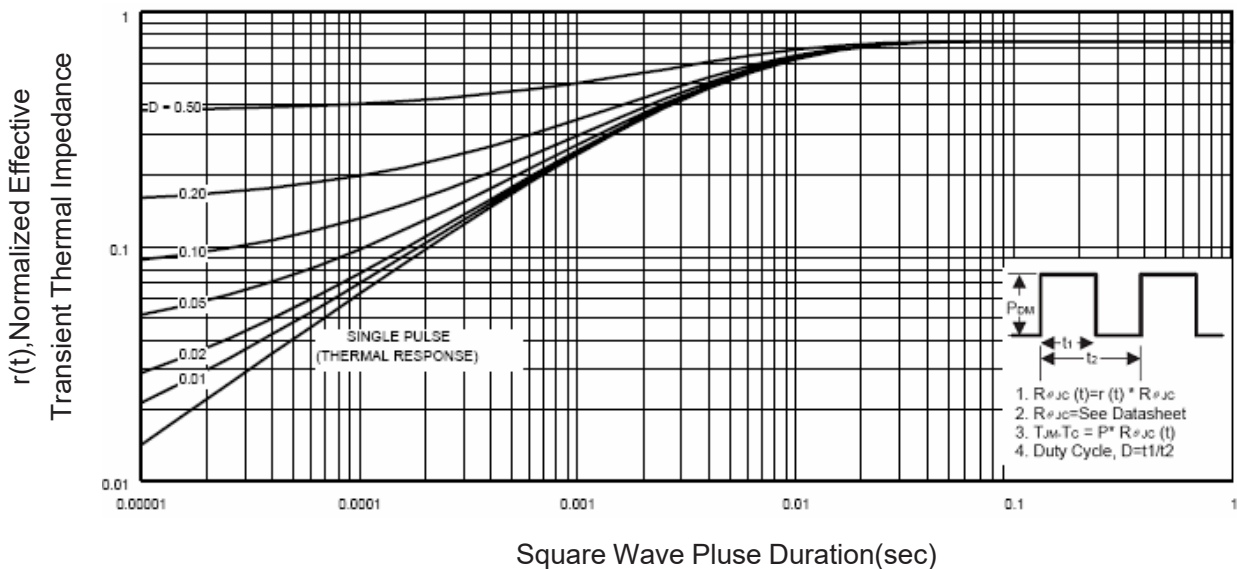


Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 BV_{DSS} vs Junction Temperature

Figure 8 Safe Operation Area

Figure 10 $V_{GS(th)}$ vs Junction Temperature

Figure 11 Normalized Maximum Transient Thermal Impedance