

Description

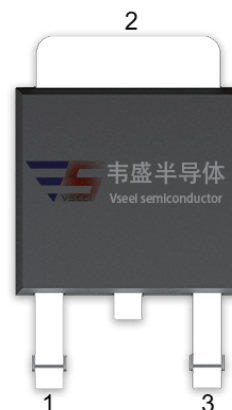
The VSM14N06 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. It is ESD protected.

General Features

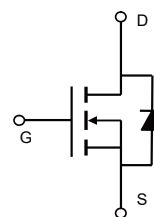
- $V_{DS} = 60V$, $I_D = 14.5A$
 $R_{DS(ON)} < 51m\Omega$ @ $V_{GS} = 10V$
 $R_{DS(ON)} < 62m\Omega$ @ $V_{GS} = 4.5V$
ESD Rating: 2800V HBM
- High density cell design for ultra low $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



TO-252



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM14N06	VSM14N06-T2	TO-252	-	-	-

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	14.5	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	12	A
Pulsed Drain Current	I_{DM}	58	A
Maximum Power Dissipation	P_D	24.2	W
Derating factor		0.16	W/ $^\circ C$
Single pulse avalanche energy (Note 5)	E_{AS}	25	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance,Junction-to-Case ^(Note 2)	$R_{\theta JC}$	6.2	$^{\circ}\text{C/W}$
Thermal Resistance,Junction-to-Ambient	$R_{\theta JA}$	50	$^{\circ}\text{C/W}$

Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

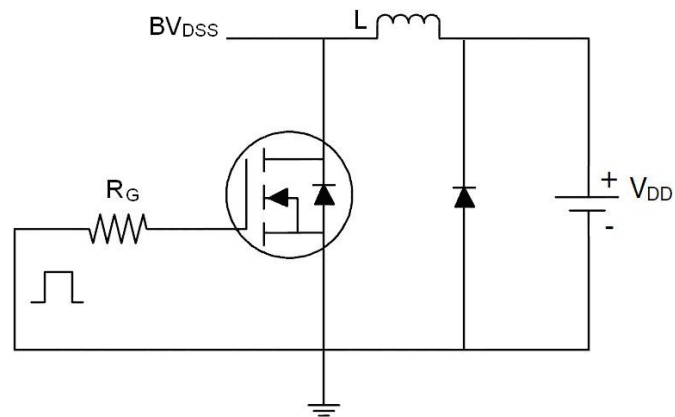
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±10	μA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.1	1.6	2.1	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =10A	-	44	51	mΩ
		V _{GS} =4.5V, I _D =8A	-	49	62	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =10A	-	12	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =30V, V _{GS} =0V, F=1.0MHz	-	617	-	pF
Output Capacitance	C _{oss}		-	43.4	-	pF
Reverse Transfer Capacitance	C _{rss}		-	35.7	-	pF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =30V, R _L =0.5Ω, R _G =10Ω, V _{GS} =10V	-	7	-	nS
Turn-on Rise Time	t _r		-	11	-	nS
Turn-Off Delay Time	t _{d(off)}		-	26	-	nS
Turn-Off Fall Time	t _f		-	9	-	nS
Total Gate Charge	Q _g	I _D =4A, V _{DD} =30V, V _{GS} =10V	-	20	-	nC
Gate-Source Charge	Q _{gs}		-	2	-	nC
Gate-Drain Charge	Q _{gd}		-	4	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =10A	-	-	1.2	V
Diode Forward Current (Note 2)	I _S		-	-	14	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 10A	-	23	-	nS
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs(Note3)	-	10	-	nC

Notes:

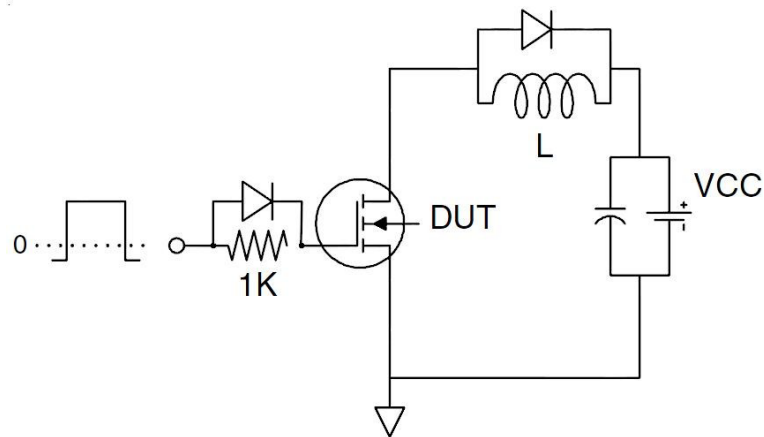
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=20V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test circuit

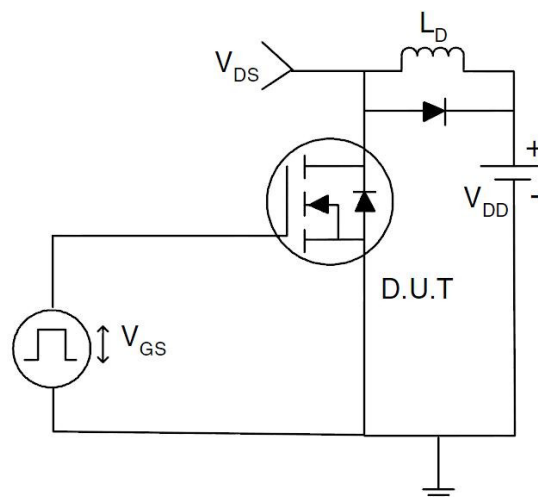
1) E_{AS} test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:



Typical Electrical and Thermal Characteristics (Curves)

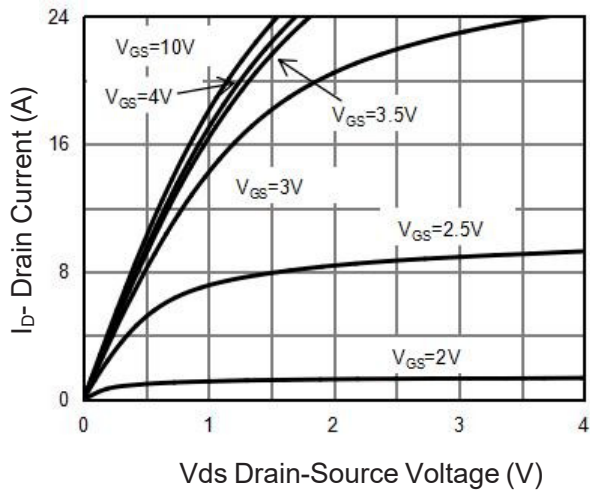


Figure 1 Output Characteristics

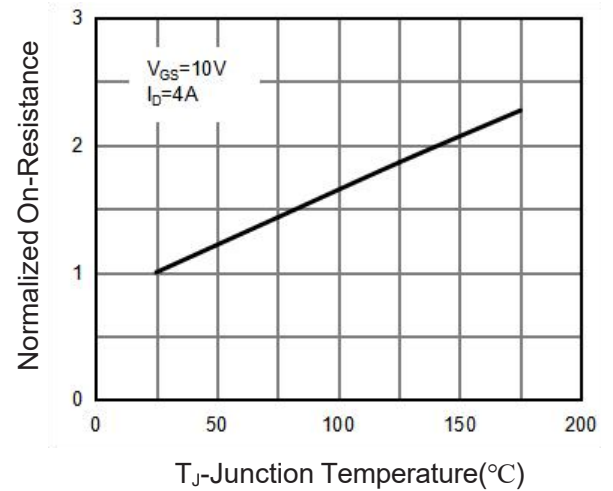


Figure 4 Rdson-Junction Temperature

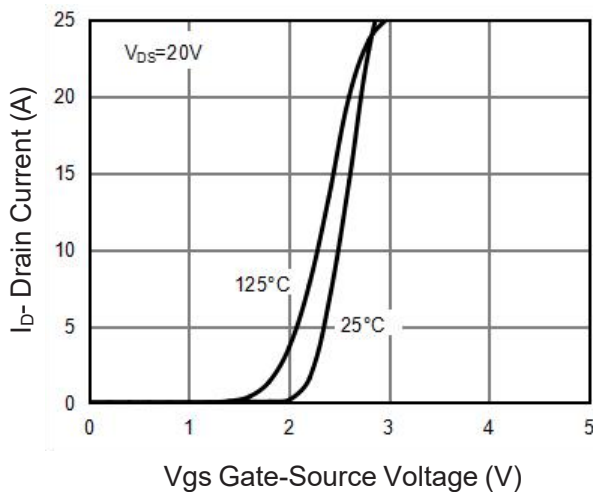


Figure 2 Transfer Characteristics

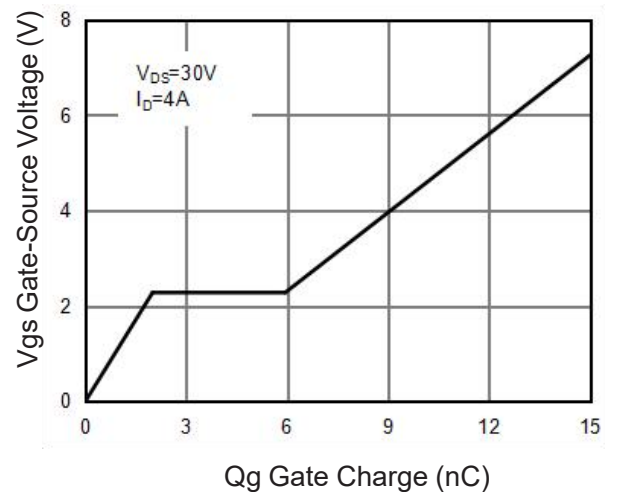


Figure 5 Gate Charge

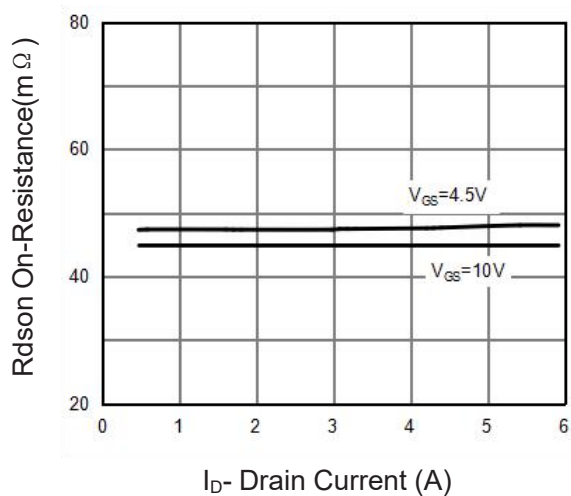


Figure 3 Rdson- Drain Current

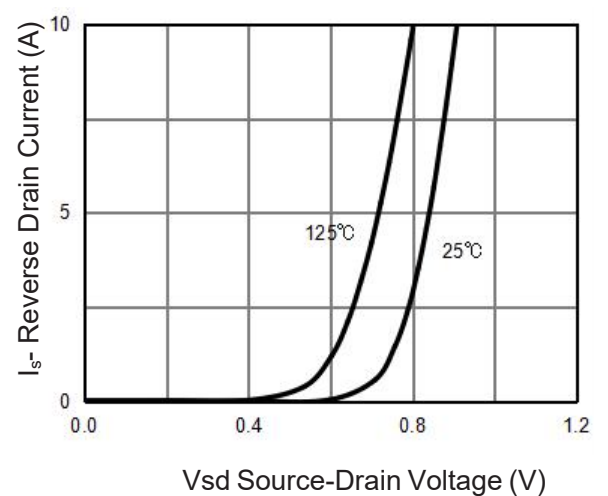
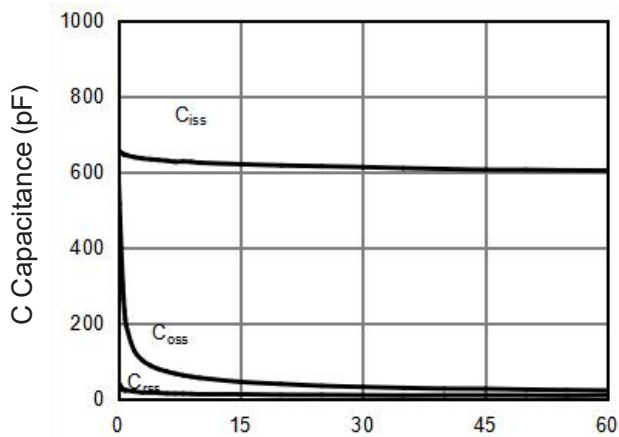
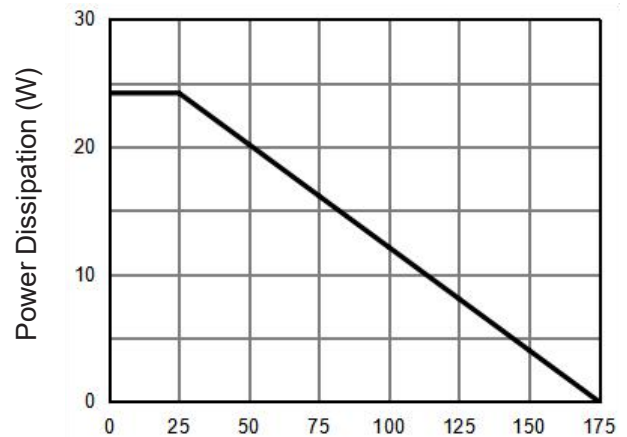


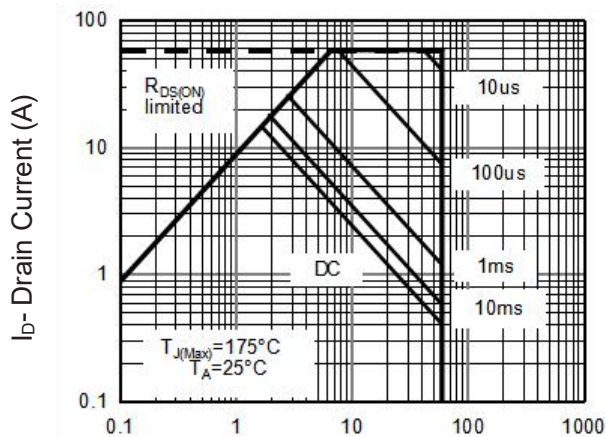
Figure 6 Source- Drain Diode Forward



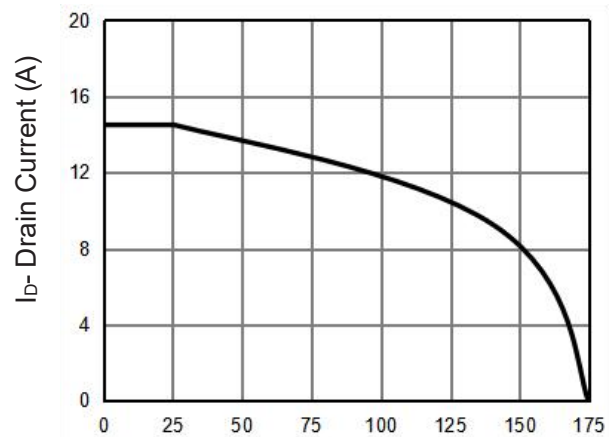
Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



T_C-Case Temperature(°C)
Figure 9 Power De-rating



Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area



T_C-Case Temperature(°C)
Figure 10 Current De-rating

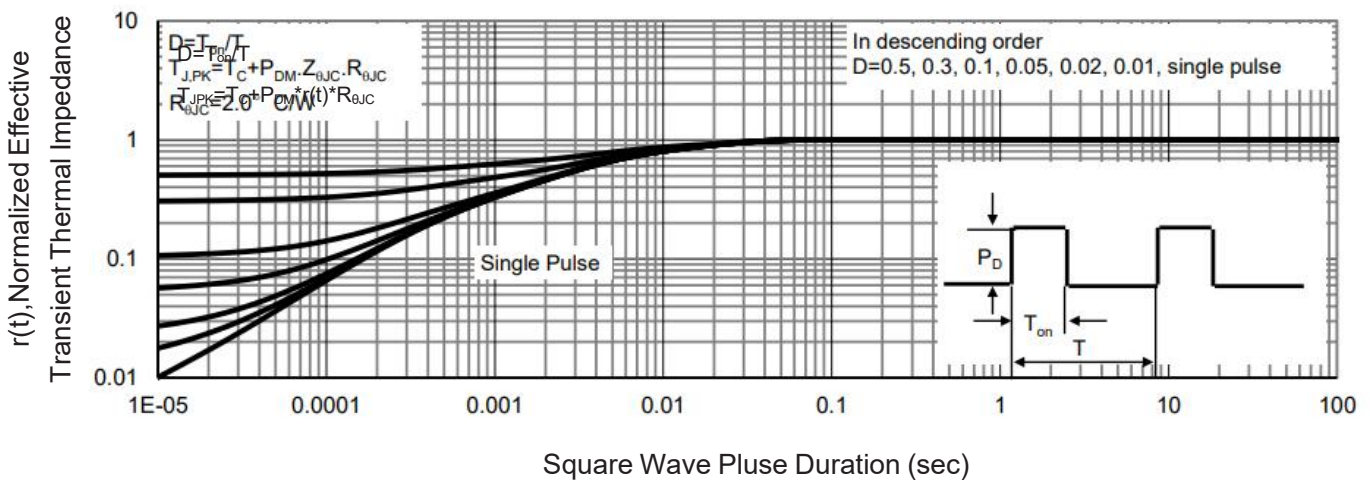


Figure 11 Normalized Maximum Transient Thermal Impedance