

Description

The VSM20N15 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

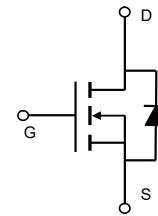
- $V_{DS} = 150V, I_D = 20A$
 $R_{DS(ON)} < 75m\Omega @ V_{GS}=10V$ (Typ:62m Ω)
 $R_{DS(ON)} < 80m\Omega @ V_{GS}=4.5V$ (Typ:68m Ω)
- High density cell design for ultra low $R_{DS(ON)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Boost converters
- LED backlighting
- Uninterruptible power supply



TO-252



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM20N15	VSM20N15-T2	TO-252	-	-	-

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Limit	Unit
V_{DS}	Drain-Source Voltage	150	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current-Continuous	20	A
$I_D (100^{\circ}C)$	Drain Current-Continuous($T_C=100^{\circ}C$)	14	A
I_{DM}	Pulsed Drain Current	40	A
P_D	Maximum Power Dissipation	90	W
	Derating factor	0.6	W/ $^{\circ}C$
E_{AS}	Single pulse avalanche energy (Note 5)	80	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	$^{\circ}C$

Thermal Characteristic

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 2)	1.7	$^{\circ}C/W$
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Electrical Characteristics ($T_C=25^{\circ}C$ unless otherwise noted)

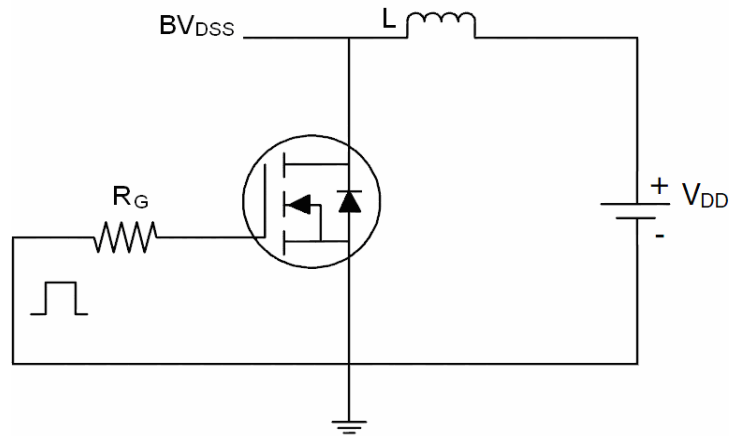
Symbol		Parameter	Condition	Min	Typ	Max	Unit
Off Characteristics							
BV _{DSS}	Drain-Source Breakdown Voltage		V _{GS} =0V I _D =250μA	150	165	-	V
I _{DSS}	Zero Gate Voltage Drain Current		V _{DS} =150V, V _{GS} =0V	-	-	1	μA
I _{GSS}	Gate-Body Leakage Current		V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)							
V _{GS(th)}	Gate Threshold Voltage		V _{DS} =V _{GS} , I _D =250μA	1.2	1.6	2.5	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V, I _D =10A	-	62	75	mΩ	
		V _{GS} =4.5V, I _D =10A	-	68	80	mΩ	
g _{FS}	Forward Transconductance		V _{DS} =5V, I _D =10A	-	20	-	S
Dynamic Characteristics (Note4)							
C _{iss}	Input Capacitance		V _{DS} =75V, V _{GS} =0V, F=1.0MHz	-	2500	-	PF
C _{oss}	Output Capacitance			-	68	-	PF
C _{rss}	Reverse Transfer Capacitance			-	54	-	PF
Switching Characteristics (Note 4)							
t _{d(on)}	Turn-on Delay Time		V _{DD} =75V, R _L =5Ω V _{GS} =10V, R _{GEN} =3Ω	-	18.5	-	nS
t _r	Turn-on Rise Time			-	10	-	nS
t _{d(off)}	Turn-Off Delay Time			-	22	-	nS
t _f	Turn-Off Fall Time			-	8	-	nS
Q _g	Total Gate Charge		V _{DS} =75V, I _D =10A, V _{GS} =10V	-	60	-	nC
Q _{gs}	Gate-Source Charge			-	7.1	-	nC
Q _{gd}	Gate-Drain Charge			-	17	-	nC
Drain-Source Diode Characteristics							
V _{SD}	Diode Forward Voltage (Note 3)		V _{GS} =0V, I _S =20A	-	-	1.2	V
I _S	Diode Forward Current (Note 2)		-	-	-	20	A
t _{rr}	Reverse Recovery Time		T _J = 25°C, I _F = 10A di/dt = 100A/μs (Note3)	-	34	-	nS
Q _{rr}	Reverse Recovery Charge			-	55	-	nC
t _{on}	Forward Turn-On Time		Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

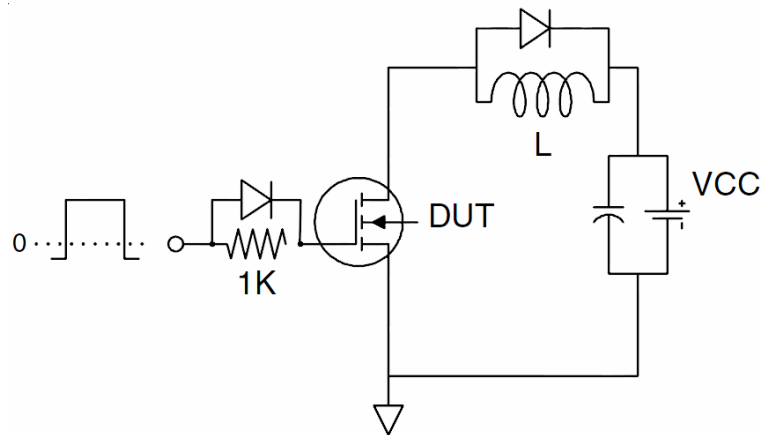
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}C, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test Circuit

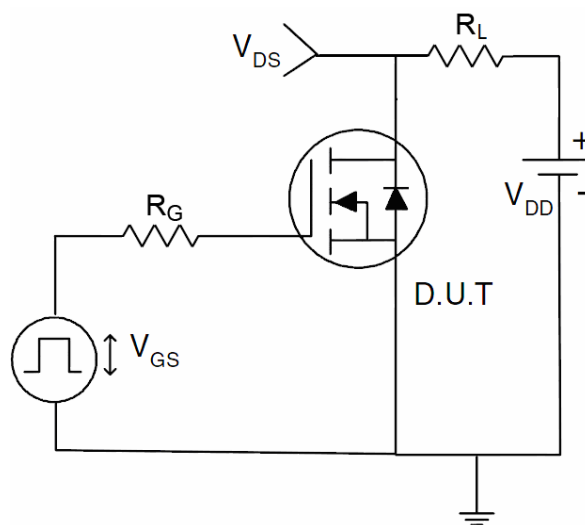
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

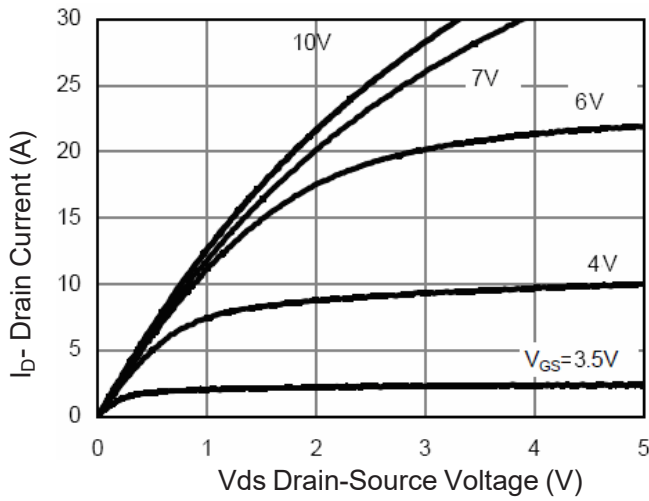


Figure 1 Output Characteristics

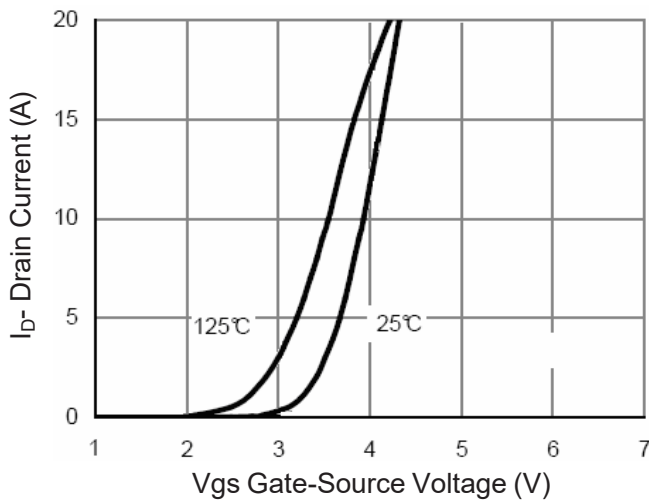


Figure 2 Transfer Characteristics

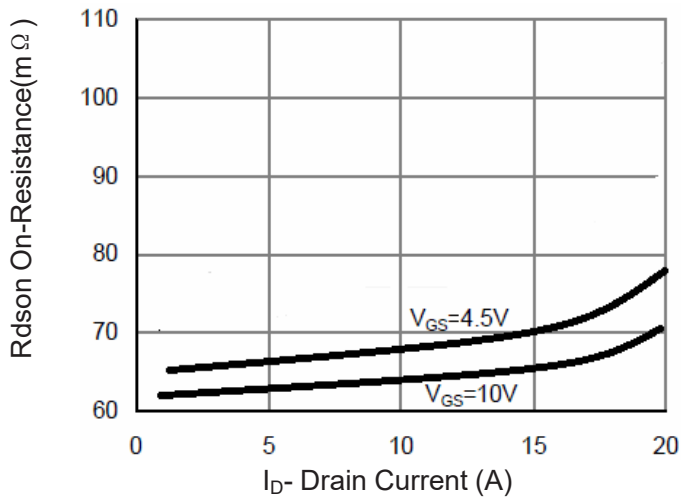


Figure 3 $R_{DS(on)}$ - Drain Current

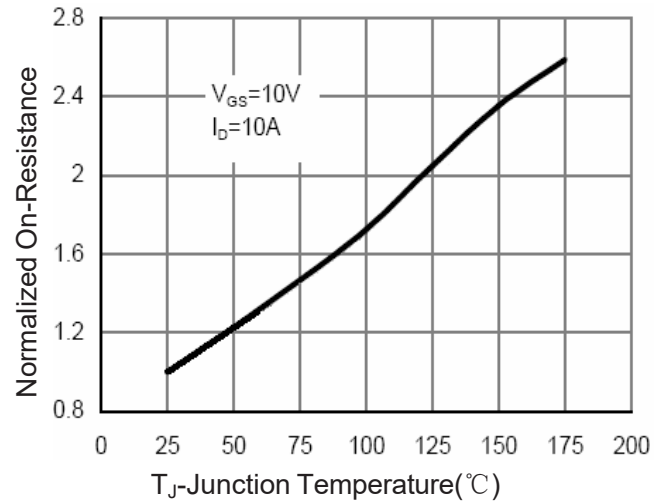


Figure 4 $R_{DS(on)}$ -Junction Temperature

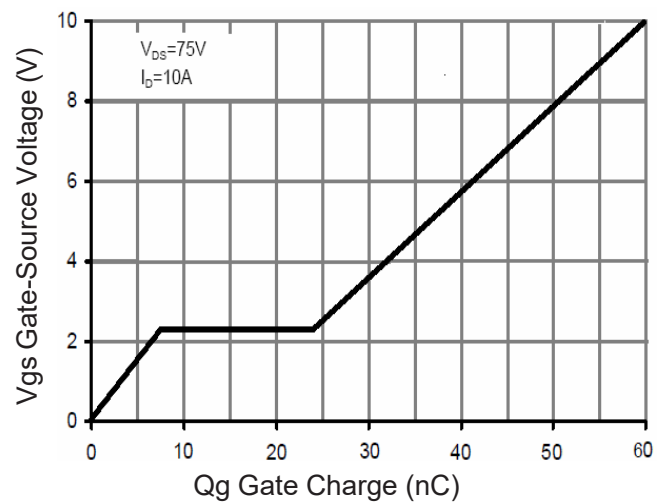


Figure 5 Gate Charge

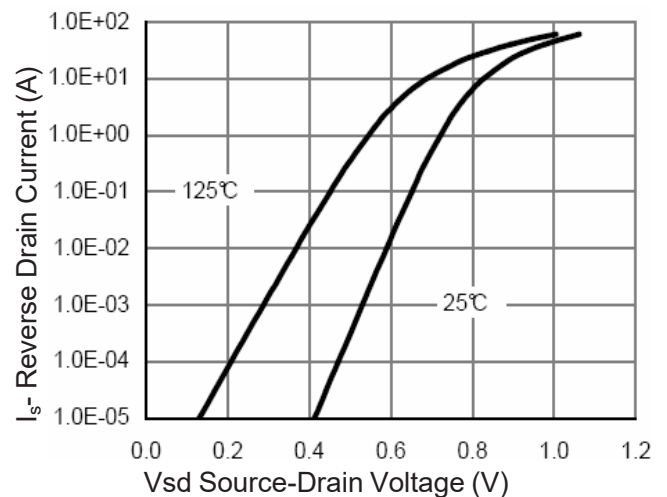
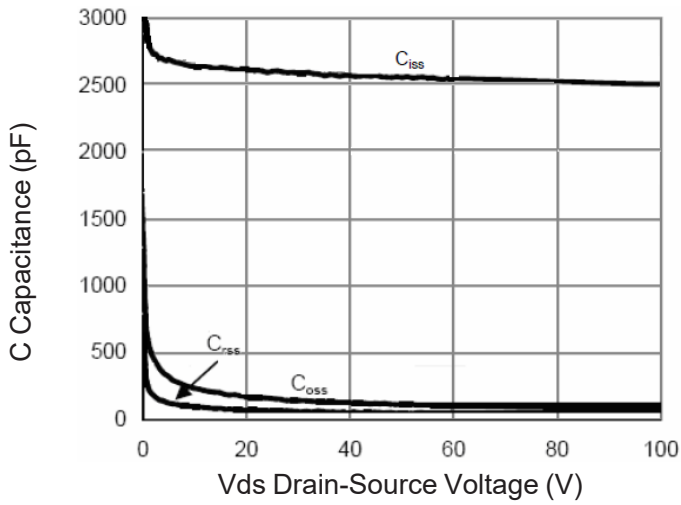
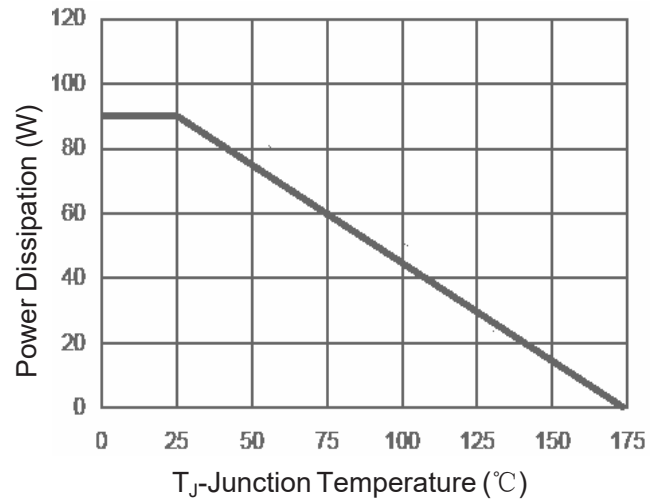
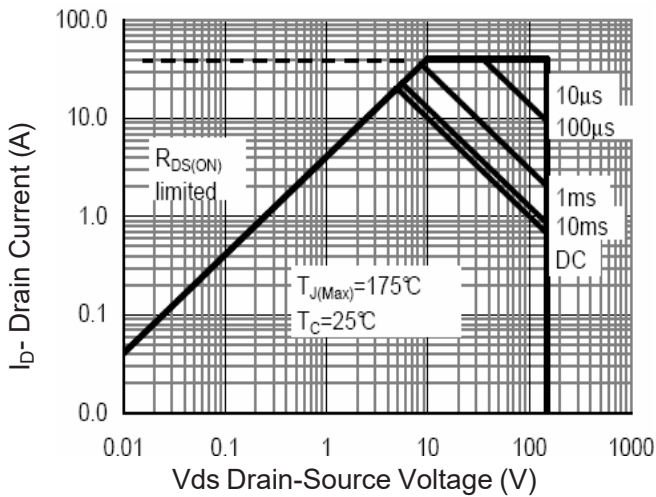
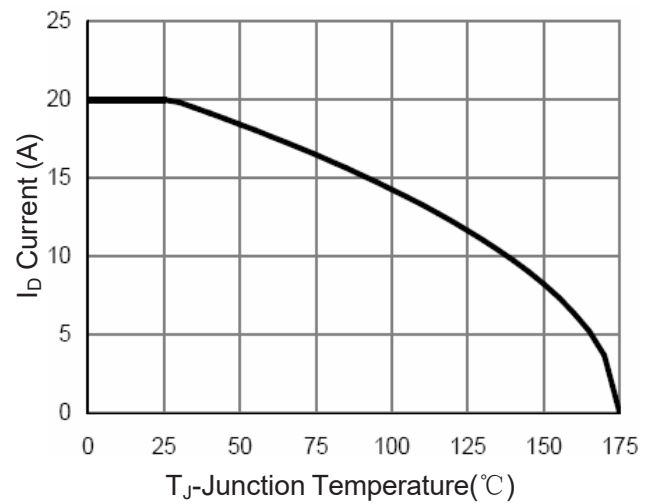
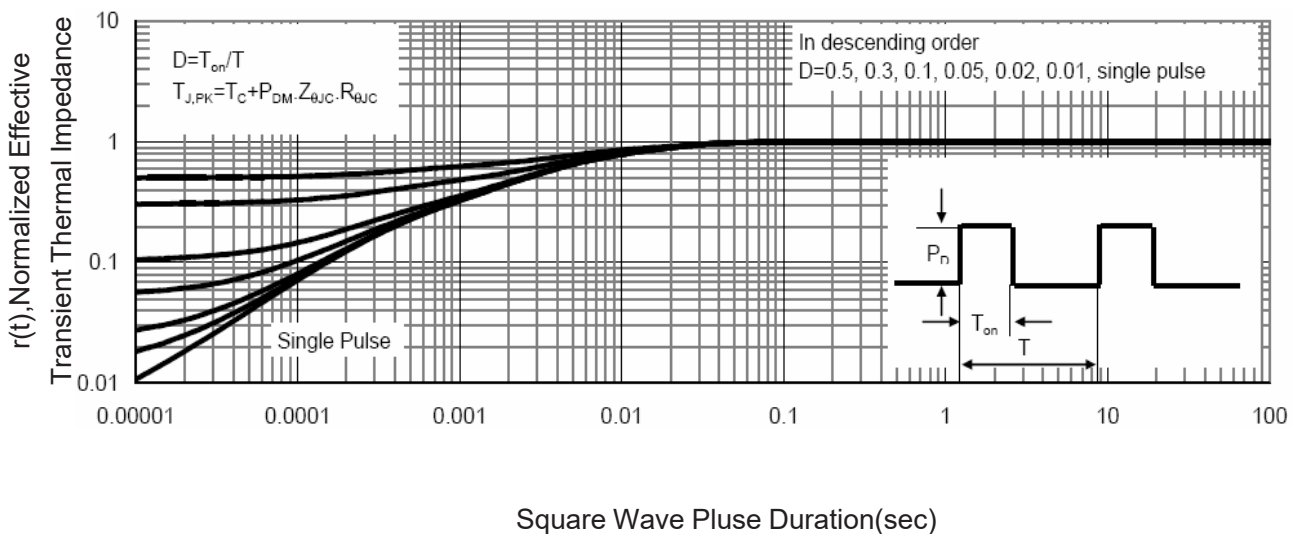


Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 Power De-rating

Figure 8 Safe Operation Area

Figure 10 ID Current- Junction Temperature

Figure 11 Normalized Maximum Transient Thermal Impedance