Description

The VSM30N04 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

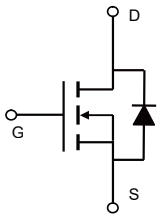
General Features

- V_{DS} = 40 V,I_D = 30 A
  $R_{DS(ON)}$ < 13 mΩ @ V_{GS}=10V (Typ: 9.8 mΩ)
  $R_{DS(ON)}$ < 18.2 mΩ @ V_{GS}=4.5V (Typ: 14 mΩ)
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Uninterruptible power supply

TO-252



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM30N04	VSM30N04-T2	TO-252	Ø330mm	16mm	2500units

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	30	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	26.9	A
Pulsed Drain Current	I_{DM}	120	A
Maximum Power Dissipation	P_D	45	W
Debating factor		0.303	W/℃
Single pulse avalanche energy (Note 1)	E_{AS}	92	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case	$R_{\theta JC}$	3.33	℃/W
Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	50	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

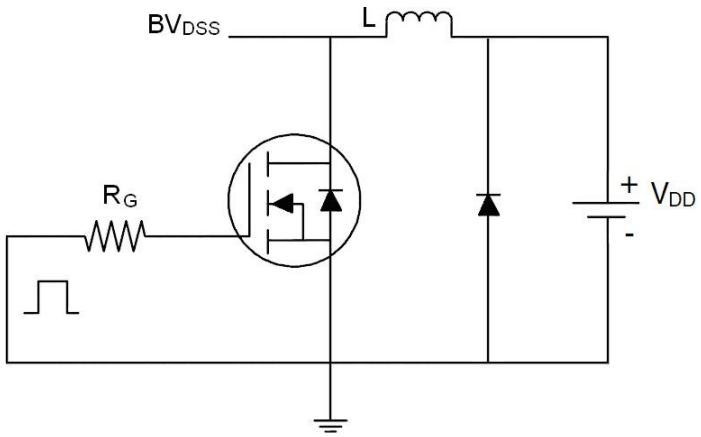
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.0	1.5	2.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	-	9.8	13	mΩ
		V_{GS}=4.5V, I_D=20A	-	14	18.2	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=15A	-	15	-	S
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=20V,V_{GS}=0V, F=1.0MHz	-	964	-	pF
Output Capacitance	C_{oss}		-	109	-	pF
Reverse Transfer Capacitance	C_{rss}		-	96	-	pF
Switching Characteristics (Note 3)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=20V, R_L=1.3Ω V_{GS}=10V,R_{GEN}=3Ω	-	5.5	-	nS
Turn-on Rise Time	t_r		-	14	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	24	-	nS
Turn-Off Fall Time	t_f		-	12	-	nS
Total Gate Charge	Q_g	V_{DS}=20V,I_D=15A, V_{GS}=10V	-	22.9	-	nC
Gate-Source Charge	Q_{gs}		-	3.5	-	nC
Gate-Drain Charge	Q_{gd}		-	5.3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=20A	-	-	1.2	V
Diode Forward Current	I_S		-	-	30	A

Notes:

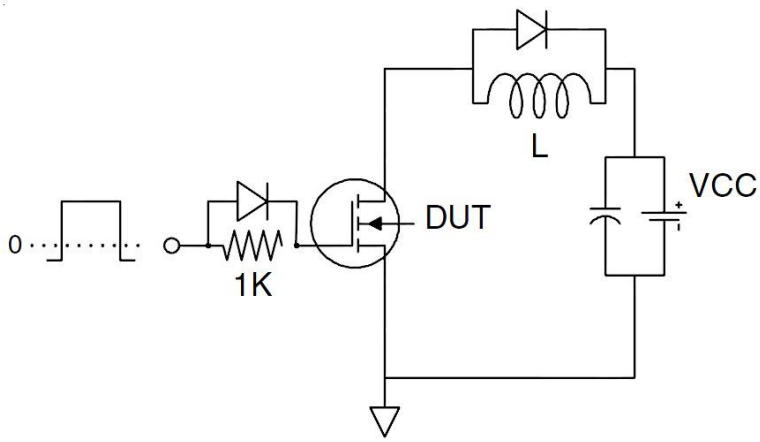
1. EAS condition : Tj=25℃,V_{DD}=32V,V_G=10V,L=0.5mH,Rg=25Ω.
2. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The maximum allowed junction temperature of 175°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.
3. Guaranteed by design, not subject to production.
4. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C. The SOA curve provides a single pulse rating.

Test circuit

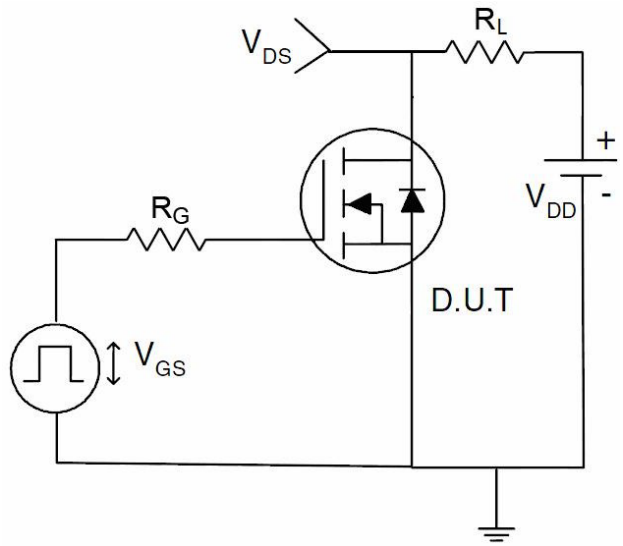
1) E_{AS} test Circuits



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

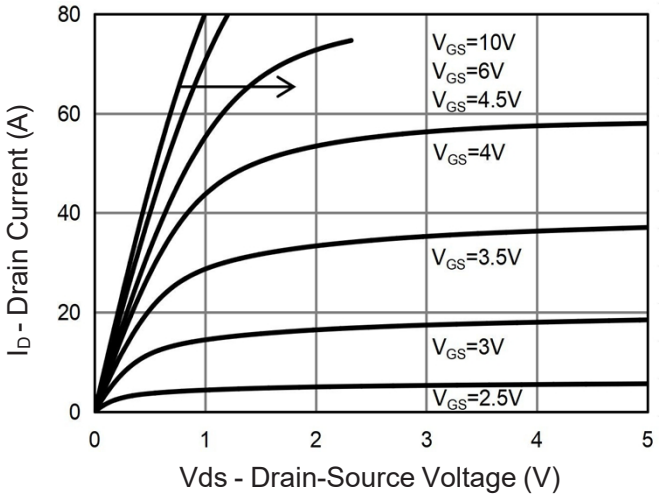


Figure 1 Output Characteristics

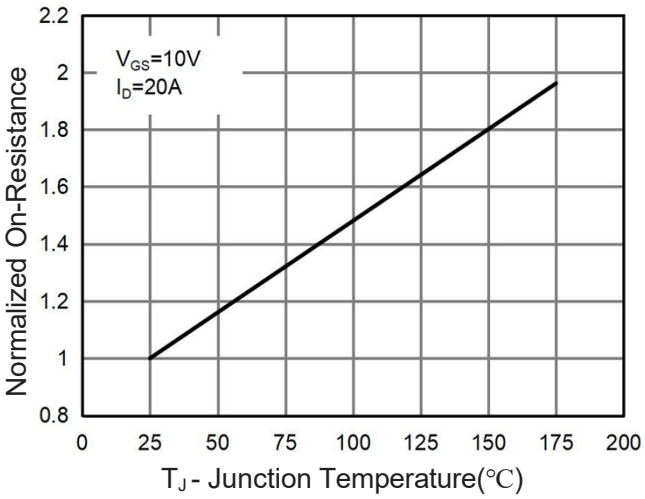


Figure 4 Rdson vs JunctionTemperature

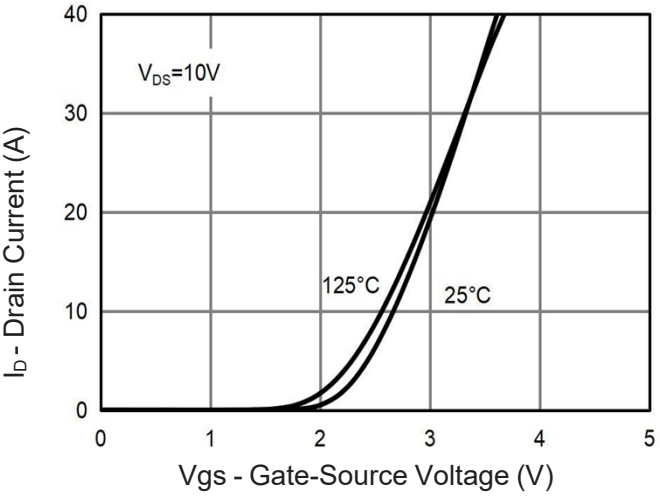


Figure 2 Transfer Characteristics

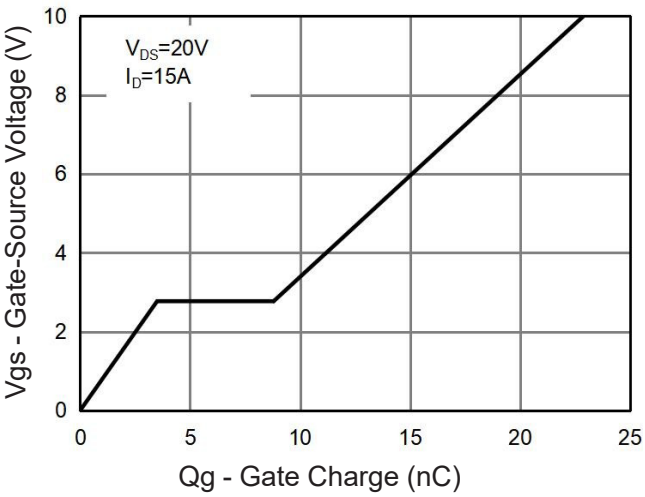


Figure 5 Gate Charge

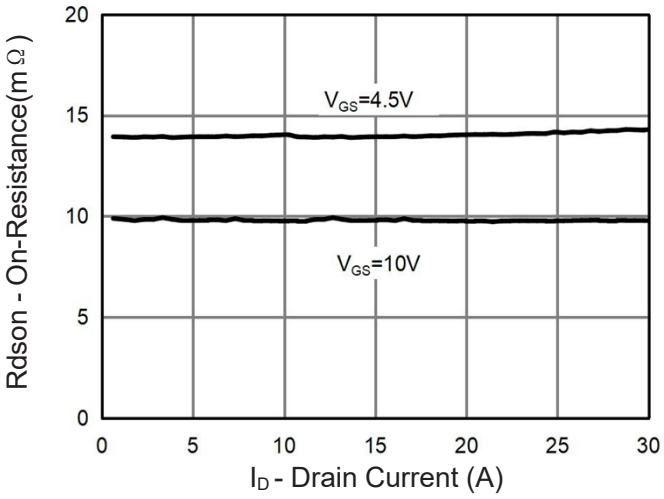


Figure 3 Rdson vs Drain Current

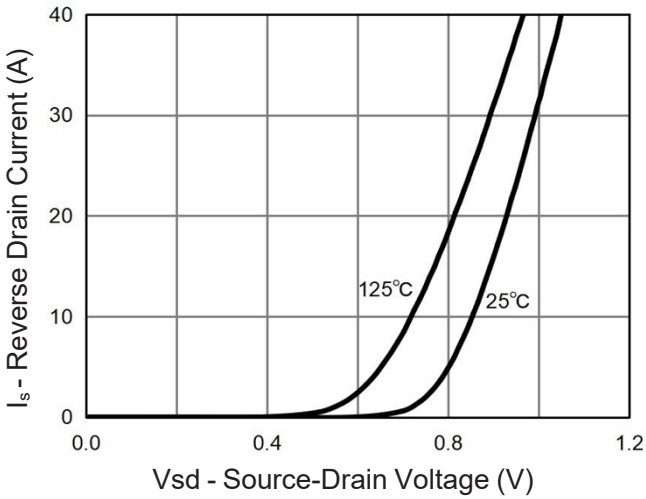


Figure 6 Source-Drain Diode Forward

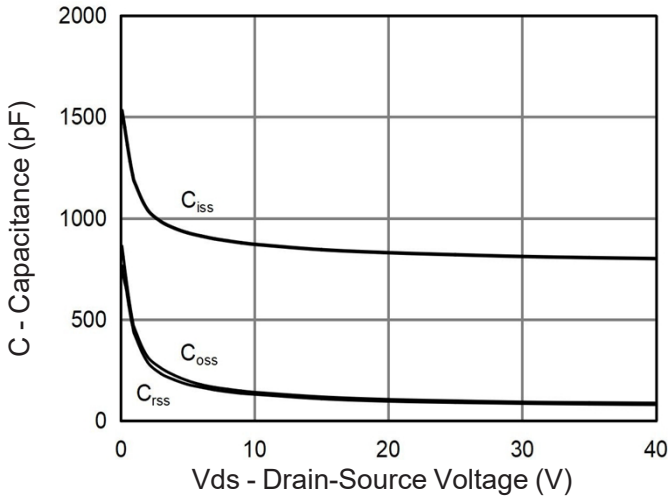


Figure 7 Capacitance vs Vds

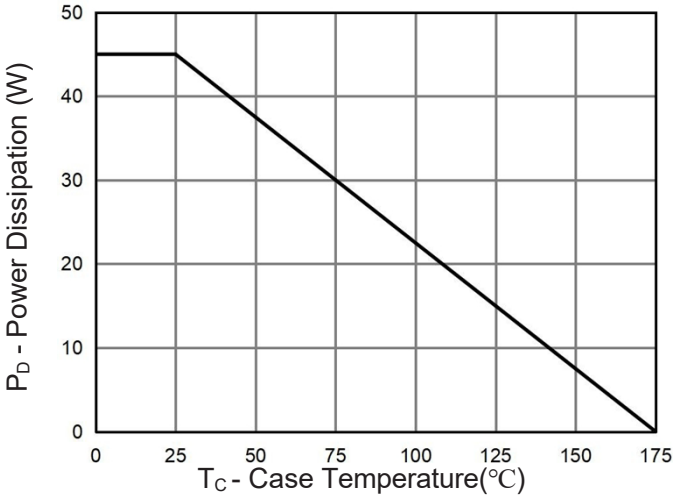


Figure 9 Power De-rating

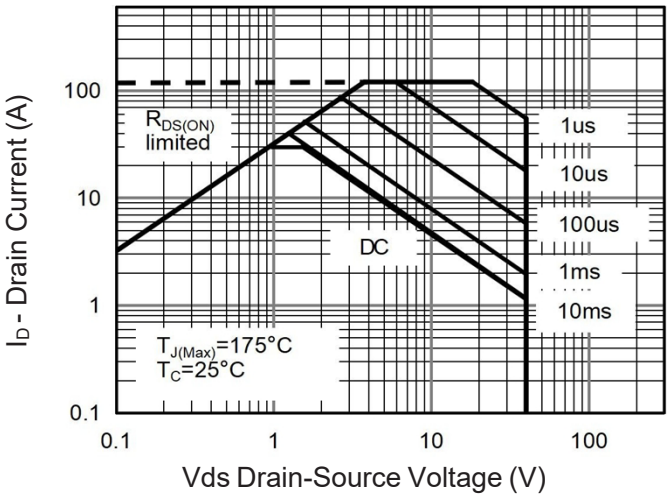


Figure 8 Safe Operation Area (Note 4)

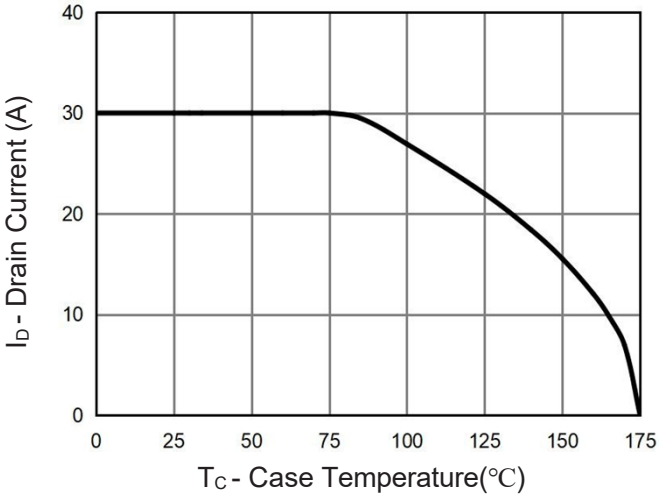


Figure 10 Drain Current De-rating

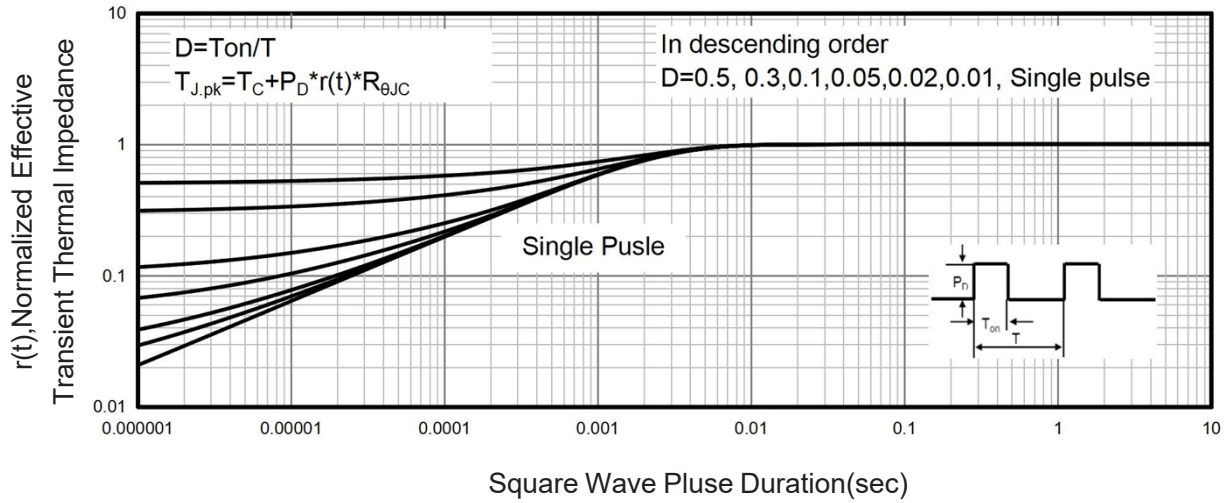


Figure 11 Normalized Maximum Transient Thermal Impedance