Description

The VSM30N10 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

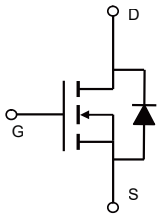
General Features

- V_{DS} = 100V,I_D =30A
  $R_{DS(ON)}$ < 32mΩ @ V_{GS}=10V (Typ:25mΩ)
  $R_{DS(ON)}$ < 35mΩ @ V_{GS}=4.5V (Typ:28mΩ)
- Special process technology for high ESD capability
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

TO-252



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM30N10	VSM30N10-T2	TO-252	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	30	A
Drain Current-Continuous(TC=100℃)	I_D (100℃)	21	A
Pulsed Drain Current (Note 1)	I_{DM}	120	A
Maximum Power Dissipation	P_D	85	W
Derating factor		0.57	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	200	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	1.8	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

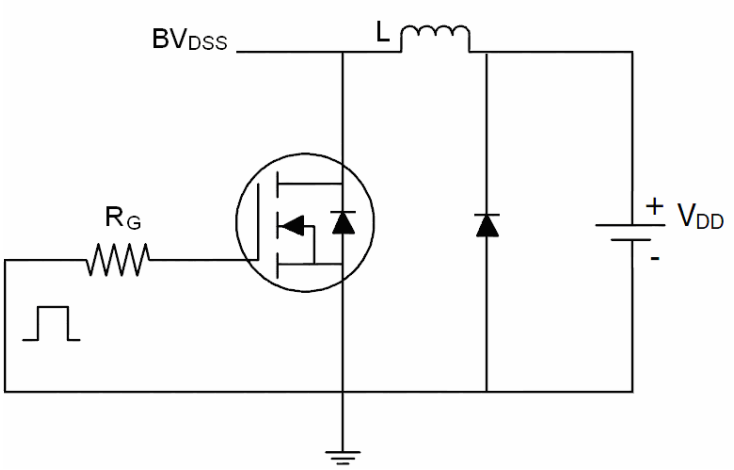
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=250μA	100	115	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=100V,V_{GS}=0V	-	-	1	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1.3	1.9	2.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=10V, I_D=10A	-	25	32	mΩ
		V_{GS}=4.5V, I_D=10A	-	28	35	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V,I_D=10A	-	15	-	S
Dynamic Characteristics (Note4)						
C_{lss}	Input Capacitance	V_{DS}=50V,V_{GS}=0V, F=1.0MHz	-	2479	-	PF
C_{oss}	Output Capacitance		-	96	-	PF
C_{rss}	Reverse Transfer Capacitance		-	79	-	PF
Switching Characteristics (Note 4)						
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=50V,R_L=5Ω V_{GS}=10V,R_{GEN}=3Ω	-	9	-	nS
t_r	Turn-on Rise Time		-	9	-	nS
$t_{d(off)}$	Turn-Off Delay Time		-	32	-	nS
t_f	Turn-Off Fall Time		-	8	-	nS
Q_g	Total Gate Charge	V_{DS}=50V,I_D=10A, V_{GS}=10V	-	67.2	-	nC
Q_{gs}	Gate-Source Charge		-	9.4	-	nC
Q_{gd}	Gate-Drain Charge		-	15.5	-	nC
Drain-Source Diode Characteristics						
V_{SD}	Diode Forward Voltage (Note 3)	V_{GS}=0V,I_S=10A	-	-	1.2	V
I_S	Diode Forward Current (Note 2)	-	-	-	30	A
t_{rr}	Reverse Recovery Time	TJ = 25°C, IF = 10A di/dt = 100A/μs (Note3)	-	32	-	nS
Qrr	Reverse Recovery Charge		-	53	-	nC
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

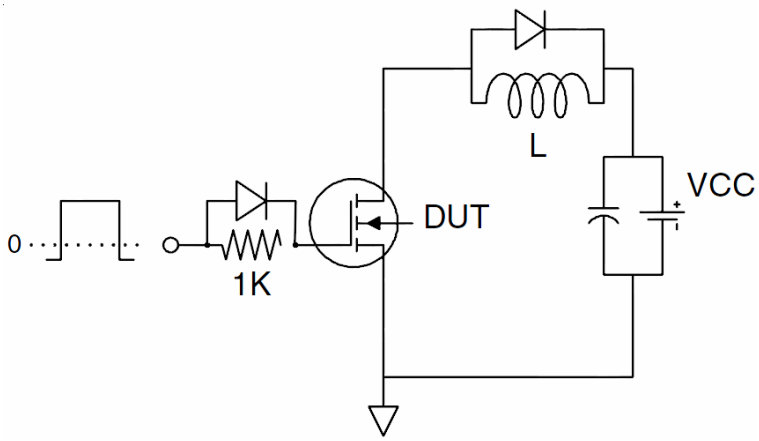
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS Condition : Tj=25℃,V_{DD}=50V,V_G=10V,L=0.5mH,Rg=25Ω

Test Circuit

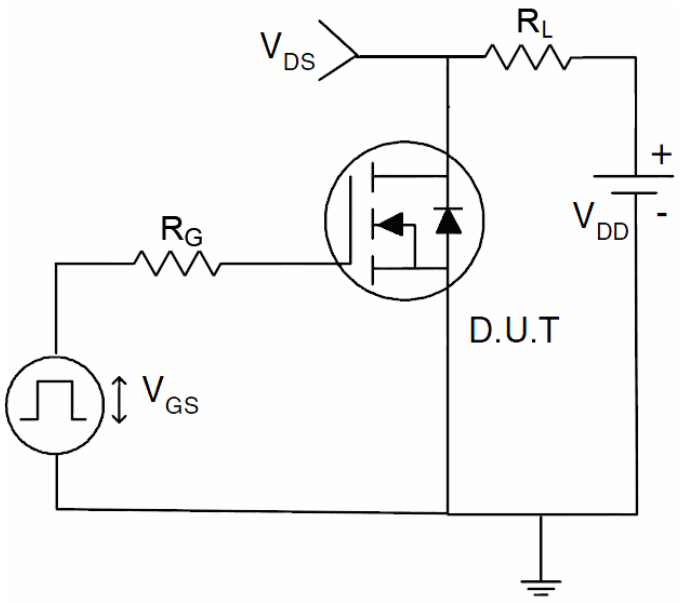
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

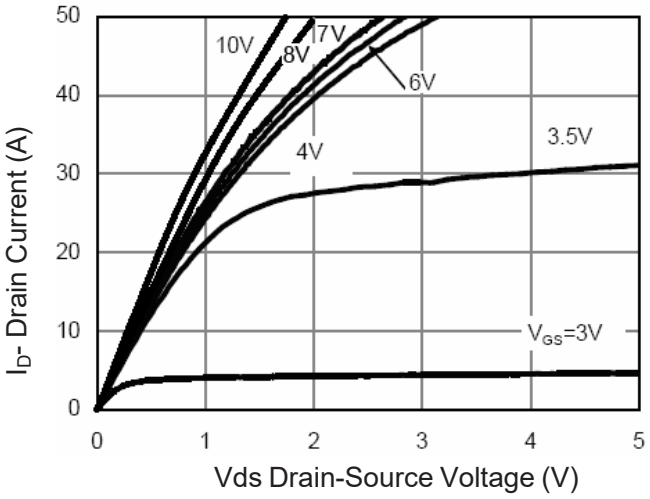


Figure 1 Output Characteristics

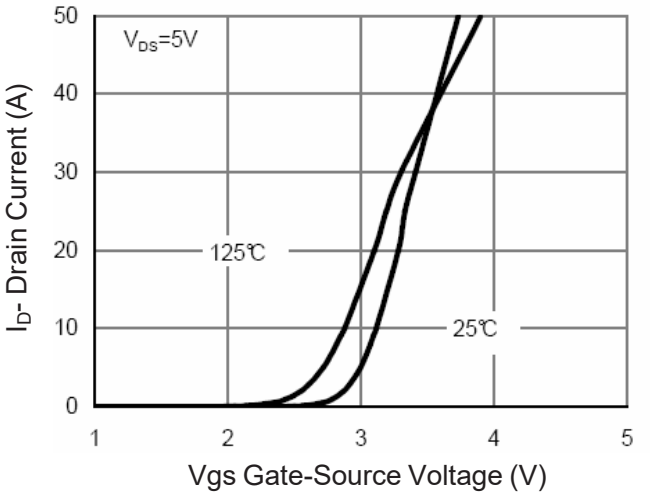


Figure 2 Transfer Characteristics

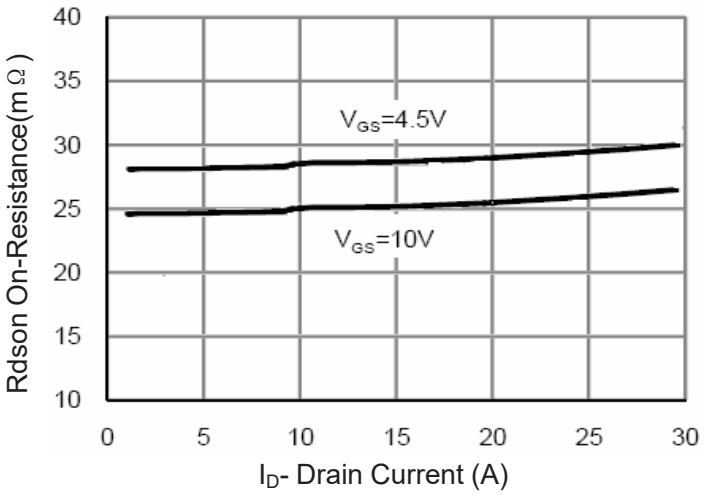


Figure 3 Rdson- Drain Current

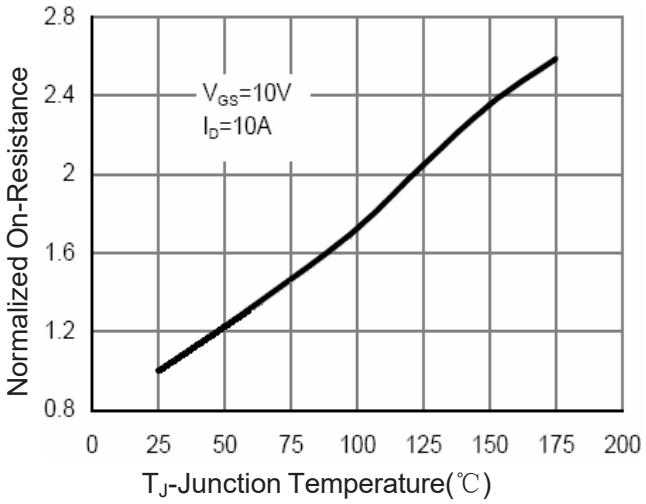


Figure 4 Rdson-JunctionTemperature

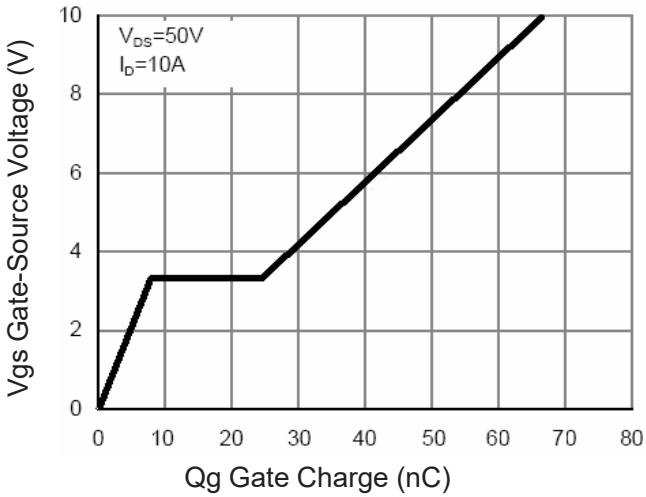


Figure 5 Gate Charge

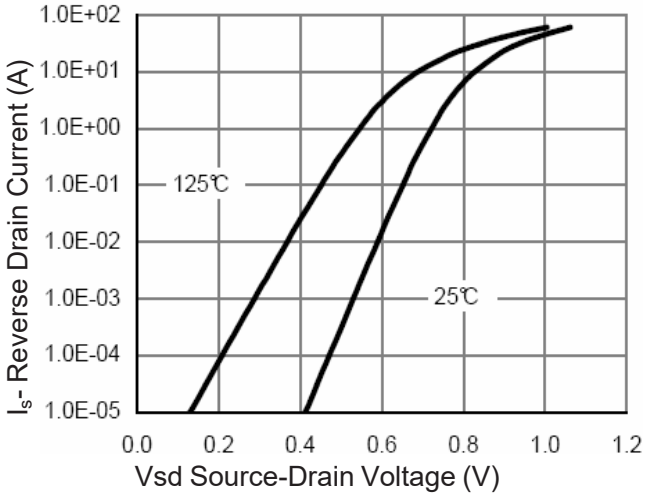


Figure 6 Source- Drain Diode Forward

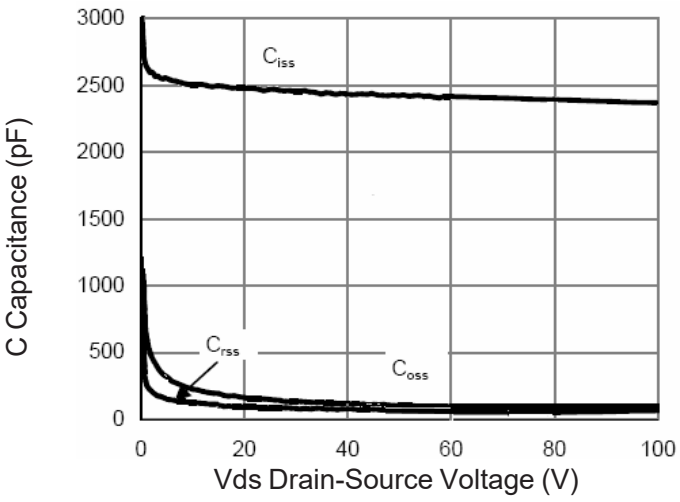


Figure 7 Capacitance vs Vds

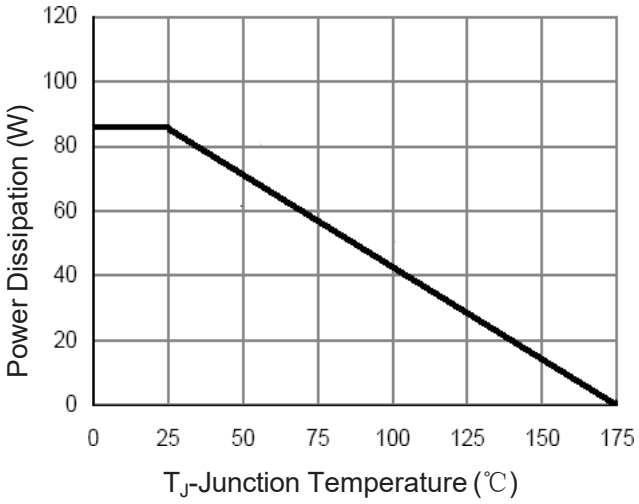


Figure 9 Power De-rating

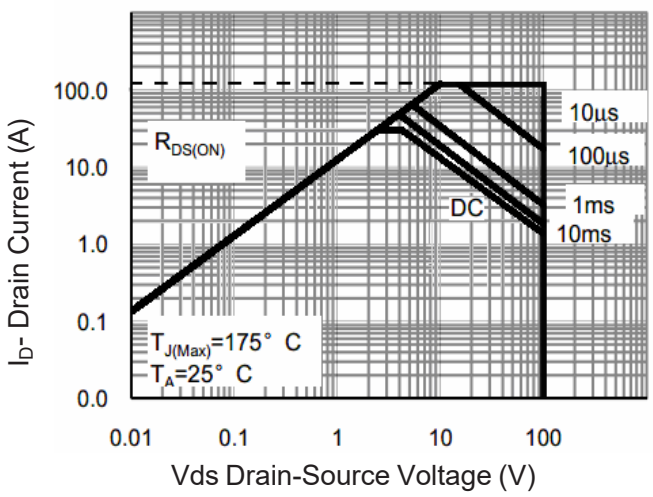


Figure 8 Safe Operation Area

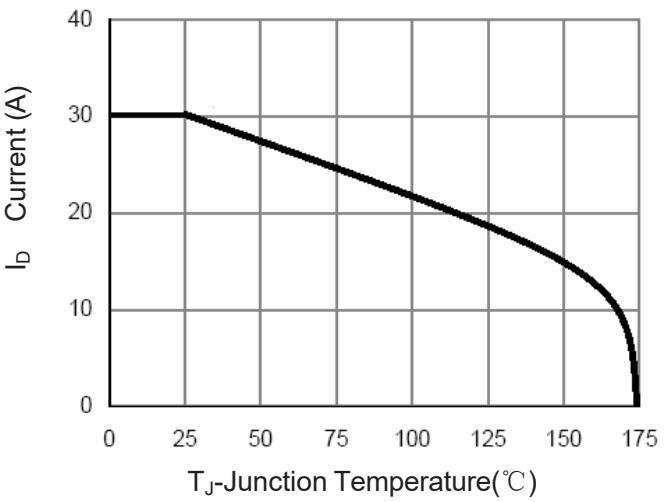


Figure 10ID Current- Junction Temperature

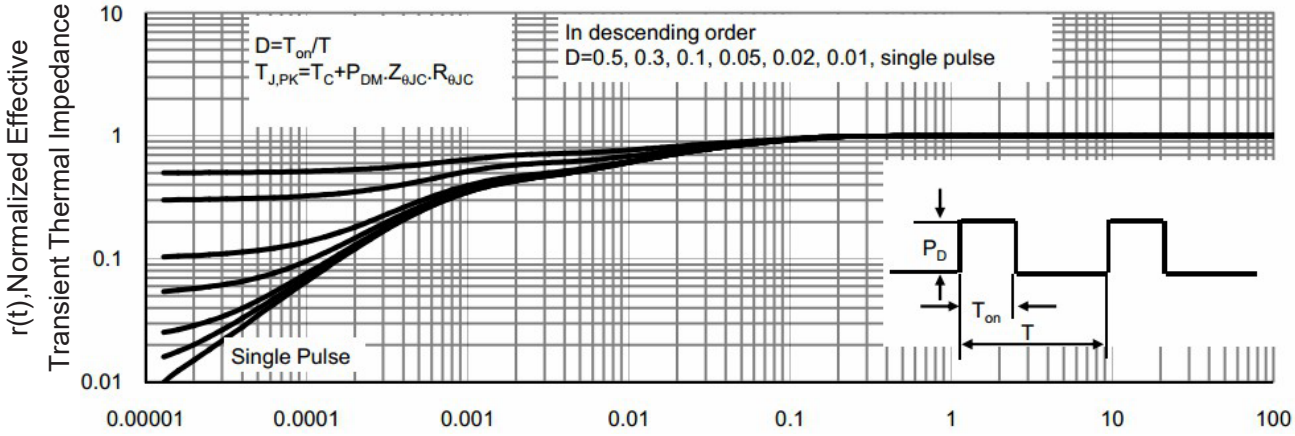


Figure 11 Normalized Maximum Transient Thermal Impedance