

Description

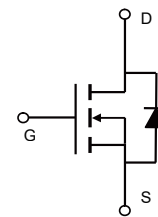
The VSM100N10 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

- $V_{DS} = 100V, I_D = 100A$
 $R_{DS(ON)} < 12m\Omega$ @ $V_{GS}=10V$ (Typ:9.9m Ω)
- Special process technology for high ESD capability
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM100N10	VSM100N10-T3	TO-263	-	-	-

Absolute Maximum Ratings ($T_c=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Limit	Unit
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current-Continuous	100	A
$I_D (100^{\circ}C)$	Drain Current-Continuous($T_C=100^{\circ}C$)	80	A
I_{DM}	Pulsed Drain Current	380	A
P_D	Maximum Power Dissipation	200	W
	Derating factor	1.33	W/ $^{\circ}C$
E_{AS}	Single pulse avalanche energy (Note 5)	720	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	$^{\circ}C$

Thermal Characteristic

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case ^(Note 2)	0.75	$^{\circ}\text{C/W}$
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Electrical Characteristics ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

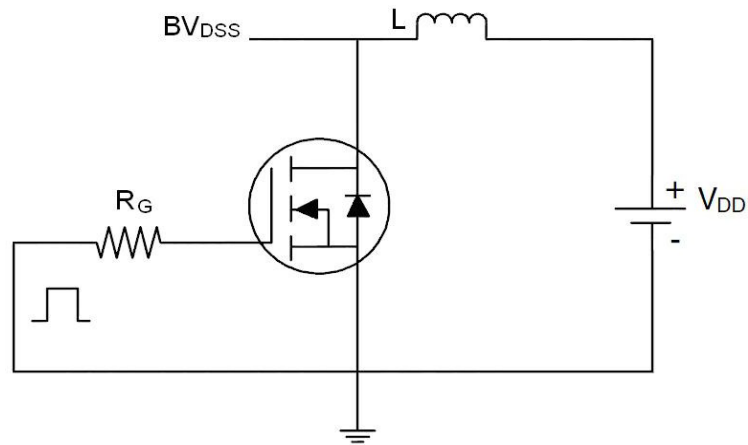
Symbol		Parameter	Condition	Min	Typ	Max	Unit
Off Characteristics							
BV _{DSS}	Drain-Source Breakdown Voltage		V _{GS} =0V I _D =250μA	100	110	-	V
I _{DSS}	Zero Gate Voltage Drain Current		V _{DS} =100V, V _{GS} =0V	-	-	1	μA
I _{GSS}	Gate-Body Leakage Current		V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)							
V _{GS(th)}	Gate Threshold Voltage		V _{DS} =V _{GS} , I _D =250μA	2	3	4	V
R _{DS(ON)}	Drain-Source On-State Resistance		V _{GS} =10V, I _D =40A	-	9.9	12	mΩ
g _{FS}	Forward Transconductance		V _{DS} =20V, I _D =40A	-	71	-	S
Dynamic Characteristics (Note4)							
C _{iss}	Input Capacitance		V _{DS} =50V, V _{GS} =0V, F=1.0MHz	-	4820	-	PF
C _{oss}	Output Capacitance			-	244	-	PF
C _{rss}	Reverse Transfer Capacitance			-	197	-	PF
Switching Characteristics (Note 4)							
t _{d(on)}	Turn-on Delay Time		V _{DD} =50V, I _D =40A V _{GS} =10V, R _{GEN} =2.5Ω	-	15	-	nS
t _r	Turn-on Rise Time			-	50	-	nS
t _{d(off)}	Turn-Off Delay Time			-	40	-	nS
t _f	Turn-Off Fall Time			-	55	-	nS
Q _g	Total Gate Charge		V _{DS} =50V, I _D =40A, V _{GS} =10V	-	123	-	nC
Q _{gs}	Gate-Source Charge			-	27	-	nC
Q _{gd}	Gate-Drain Charge			-	44	-	nC
Drain-Source Diode Characteristics							
V _{SD}	Diode Forward Voltage (Note 3)		V _{GS} =0V, I _S =40A	-	-	1.2	V
I _S	Diode Forward Current (Note 2)		-	-	-	100	A
t _{rr}	Reverse Recovery Time		TJ = 25°C, IF = 40A	-	38	80	nS
Q _{rr}	Reverse Recovery Charge		di/dt = 100A/μs(Note3)	-	53	100	nC
t _{on}	Forward Turn-On Time		Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

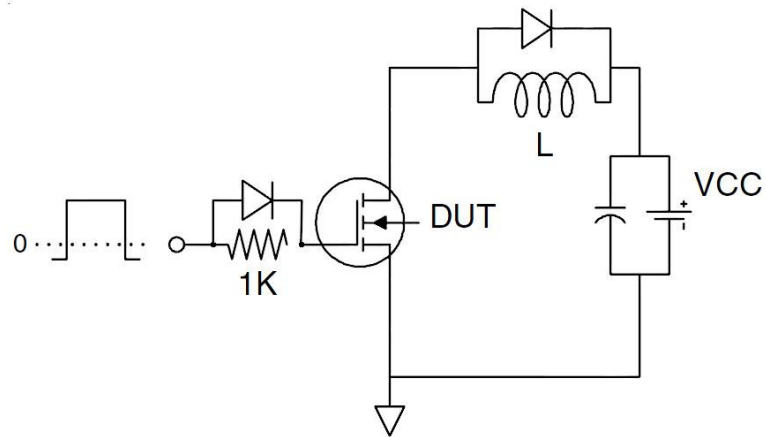
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test Circuit

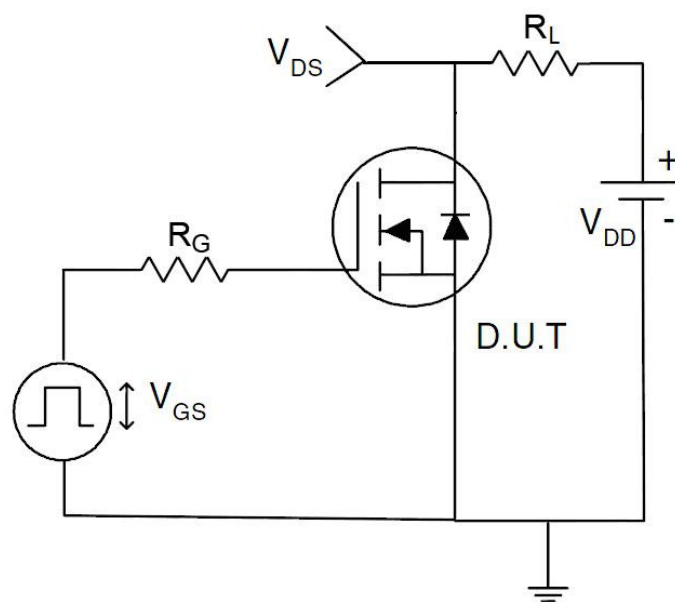
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

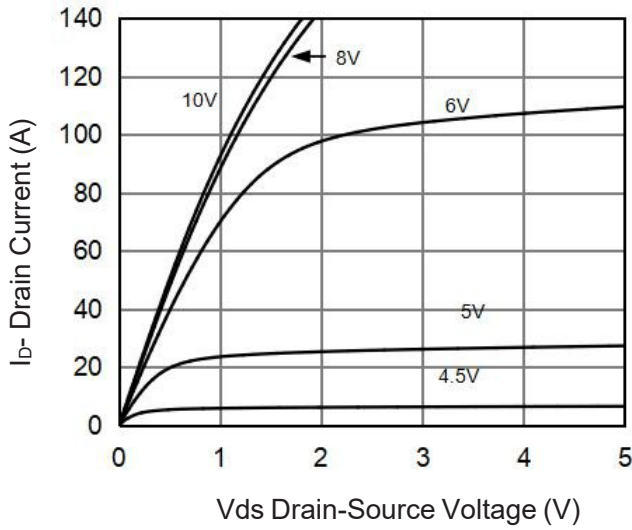


Figure 1 Output Characteristics

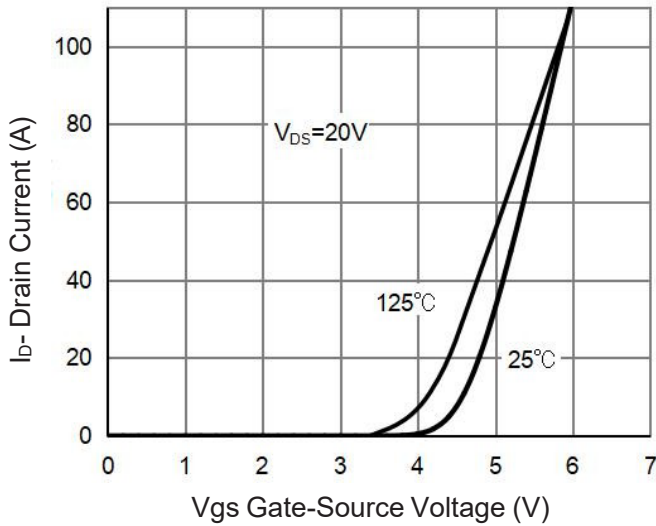


Figure 2 Transfer Characteristics

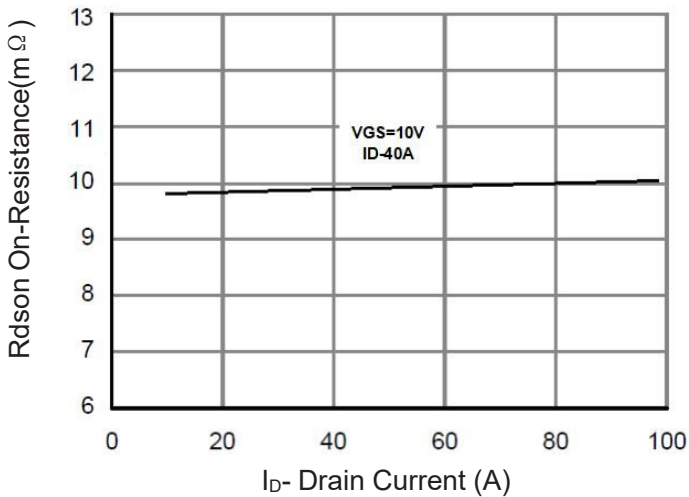


Figure 3 Rdson- Drain Current

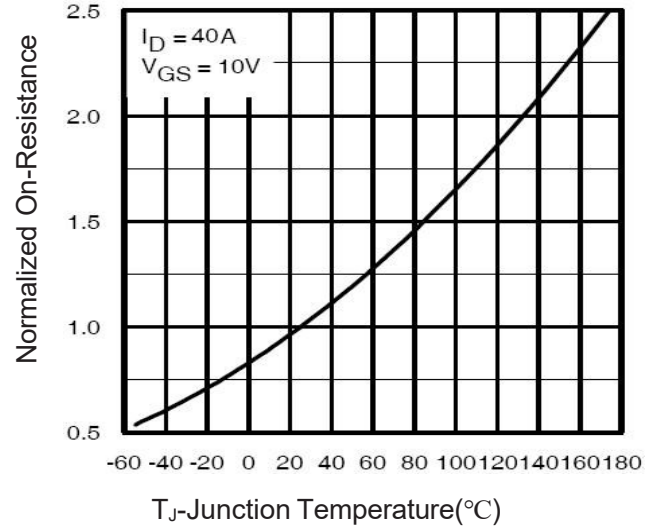


Figure 4 Rdson-Junction Temperature

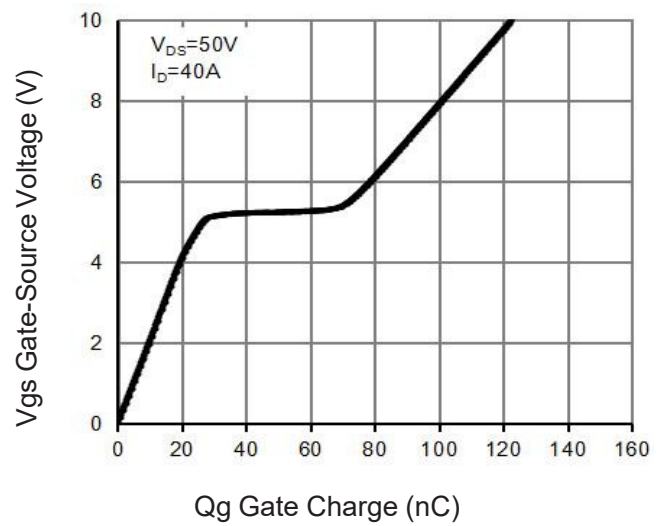


Figure 5 Gate Charge

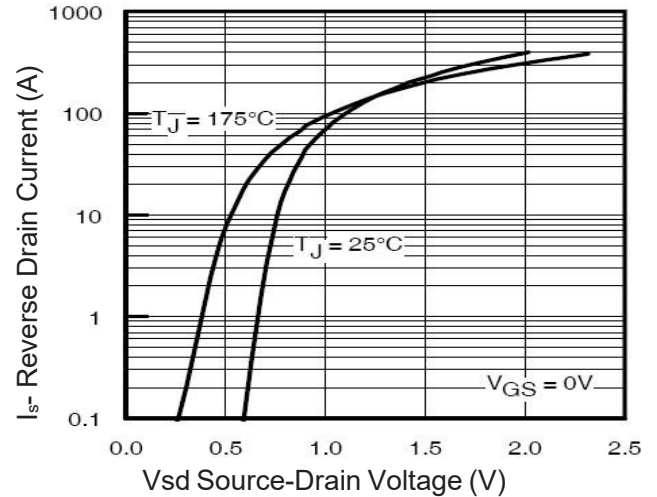
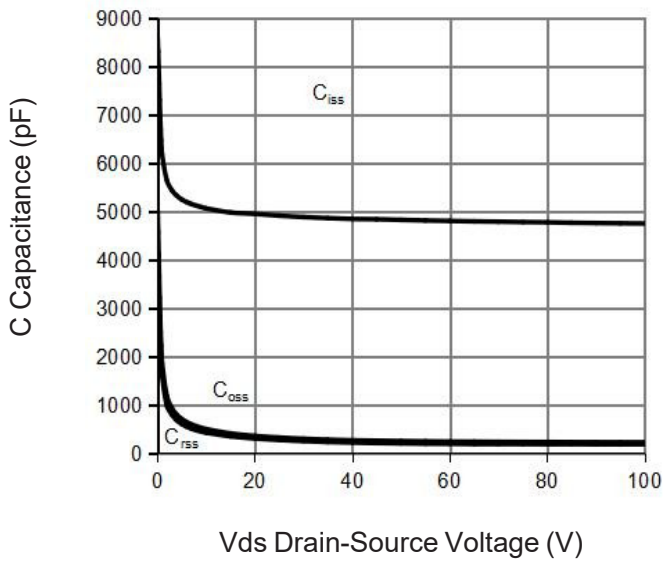
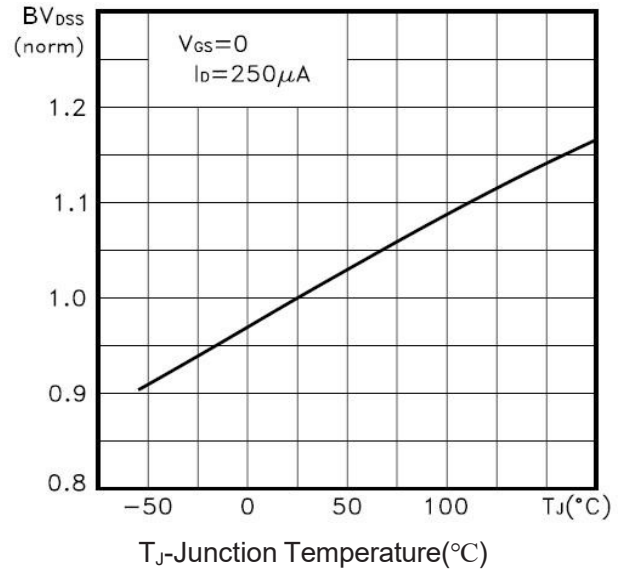
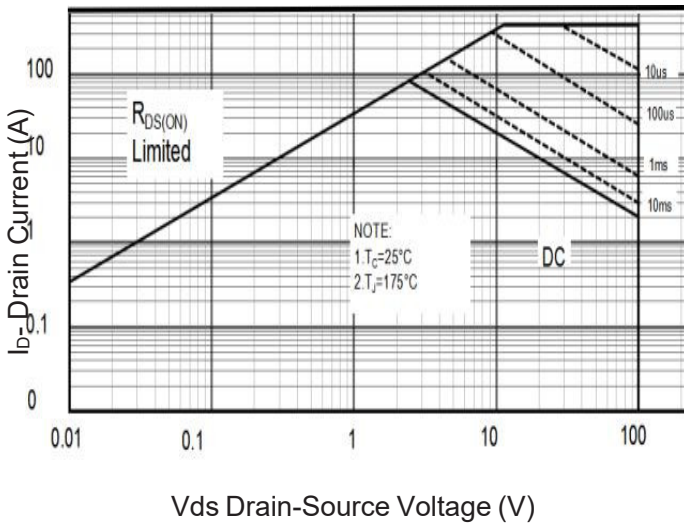
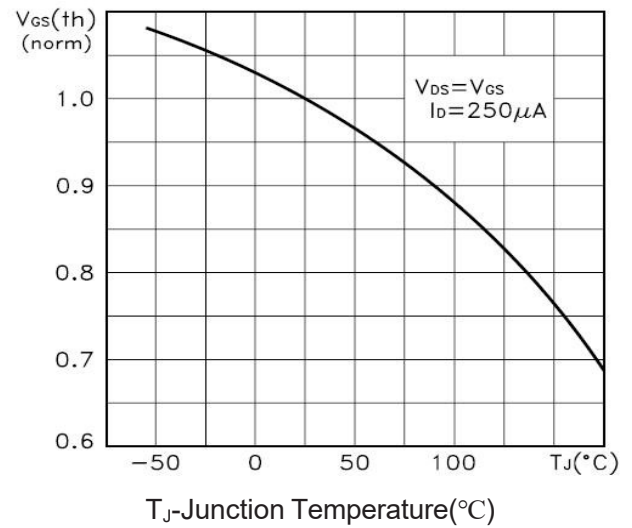
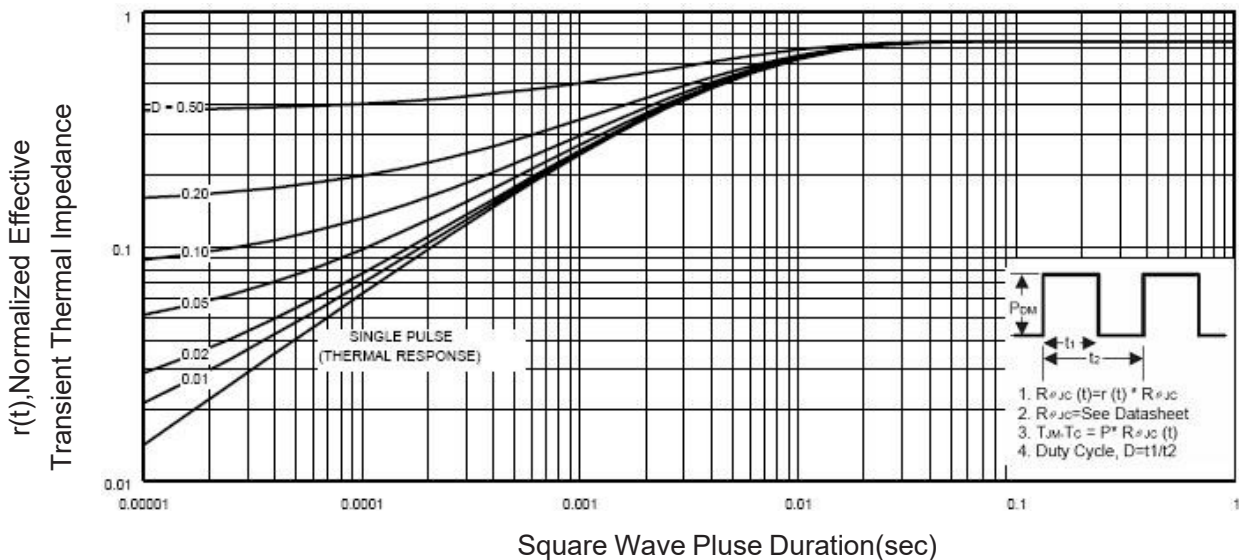


Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 BV_{DSS} vs Junction Temperature

Figure 8 Safe Operation Area

Figure 10 V_{GS(th)} vs Junction Temperature

Figure 11 Normalized Maximum Transient Thermal Impedance