

Description

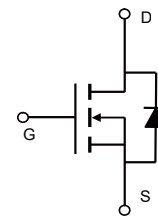
The VSM50N20 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

- $V_{DS}=200V, I_D=50A$
 $R_{DS(ON)} < 40m\Omega @ V_{GS}=10V$ (Typ:30m Ω)
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM50N20	VSM50N20-T3	TO-263	-	-	-

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	200	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	50	A
Drain Current-Continuous($T_C=100^{\circ}C$)	$I_D(100^{\circ}C)$	35	A
Pulsed Drain Current	I_{DM}	200	A
Maximum Power Dissipation	P_D	270	W
Single pulse avalanche energy (Note 5)	E_{AS}	500	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^{\circ}C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	0.6	$^{\circ}C/W$
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

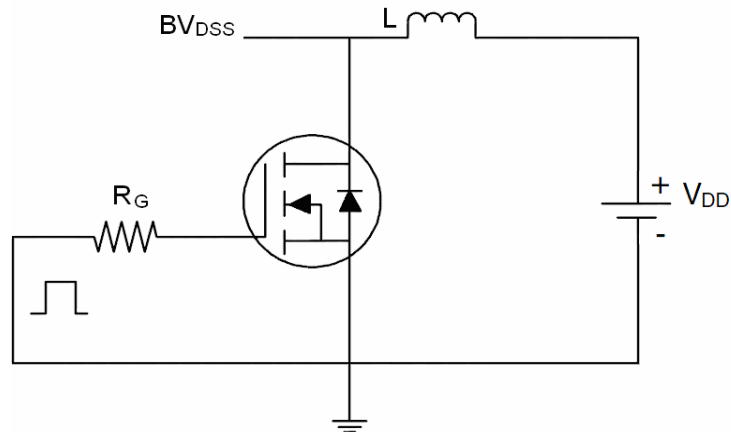
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	200	220	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=200V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=28A$	-	30	40	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=10V, I_D=20A$	25	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0MHz$		5460		PF
Output Capacitance	C_{oss}			603		PF
Reverse Transfer Capacitance	C_{rss}			161		PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=100V, I_D=28A$ $V_{GS}=10V, R_{GEN}=2.5\Omega$	-	17	-	nS
Turn-on Rise Time	t_r		-	60	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	55	-	nS
Turn-Off Fall Time	t_f		-	48	-	nS
Total Gate Charge	Q_g	$V_{DS}=100V, I_D=28A,$ $V_{GS}=10V$		150		nC
Gate-Source Charge	Q_{gs}			25		nC
Gate-Drain Charge	Q_{gd}			50		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=20A$	-	-	1.2	V
Diode Forward Current (Note 2)	I_S	-	-	-	50	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}C, I_F = 28A$ $di/dt = 100A/\mu s$ (Note3)	-	100	-	nS
Reverse Recovery Charge	Q_{rr}		-	320	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

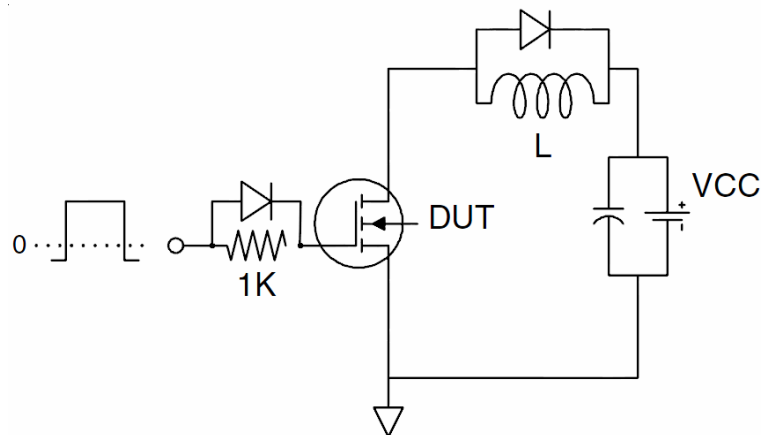
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test Circuit

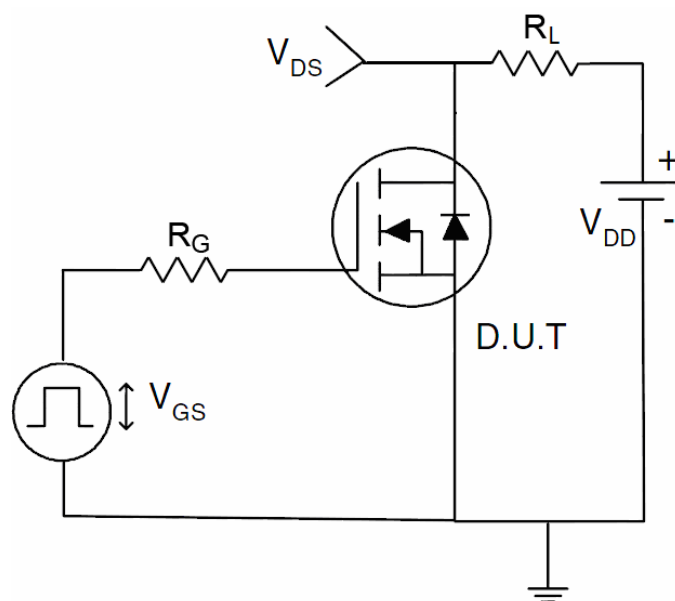
1) E_{AS} test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:



Typical Electrical and Thermal Characteristics (Curves)

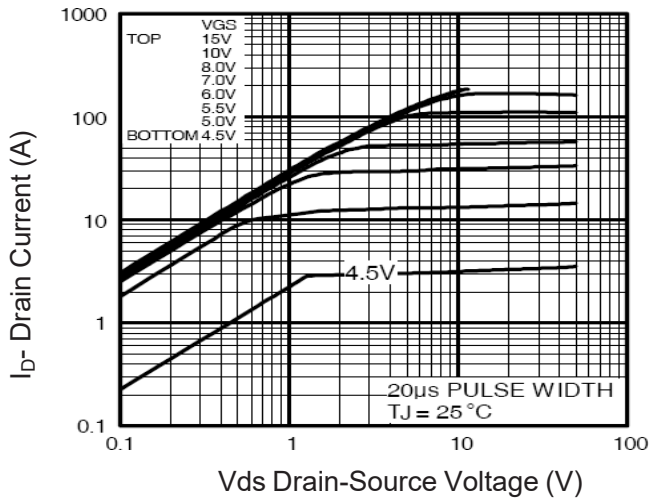


Figure 1 Output Characteristics

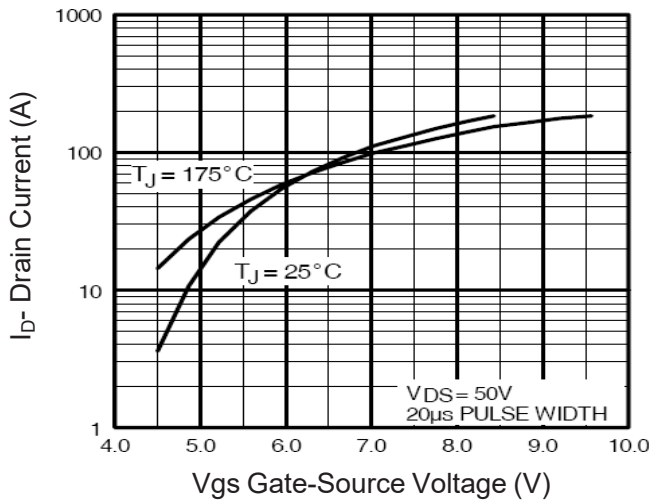


Figure 2 Transfer Characteristics

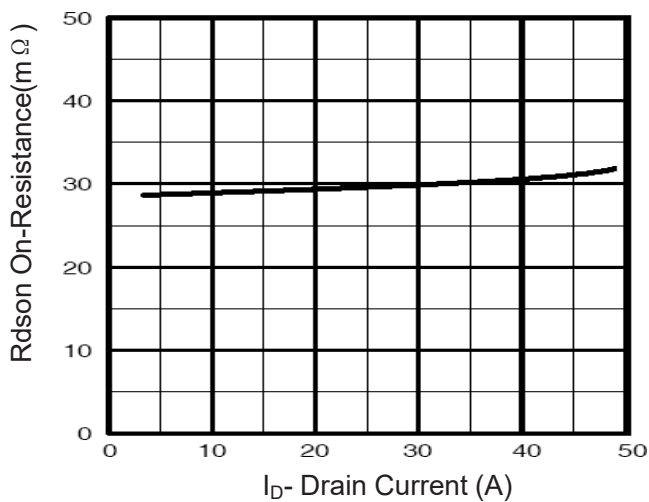


Figure 3 $R_{DS(on)}$ - Drain Current

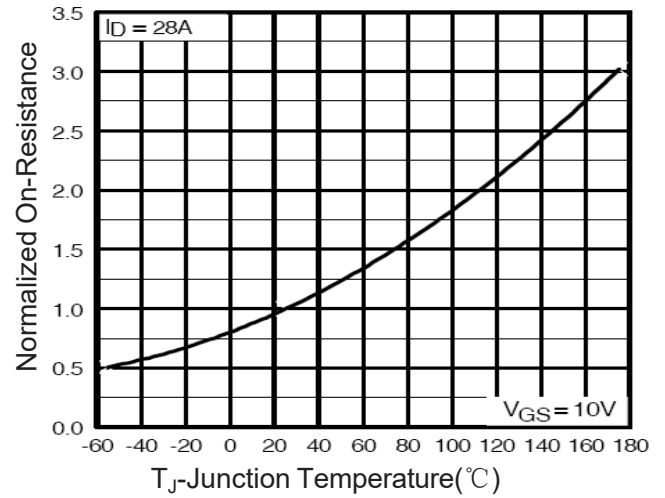


Figure 4 $R_{DS(on)}$ -Junction Temperature

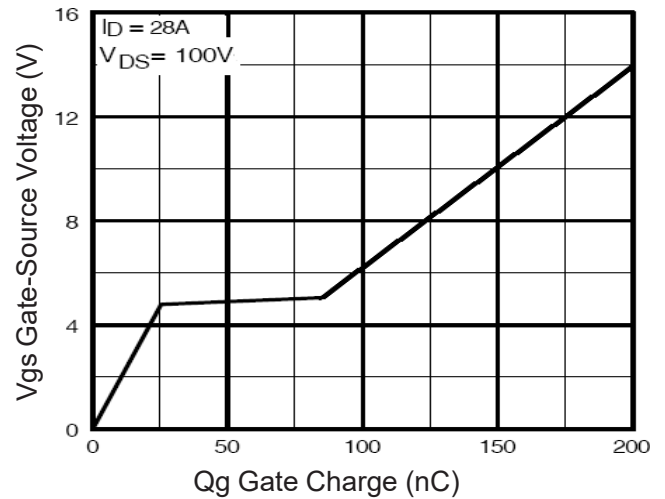


Figure 5 Gate Charge

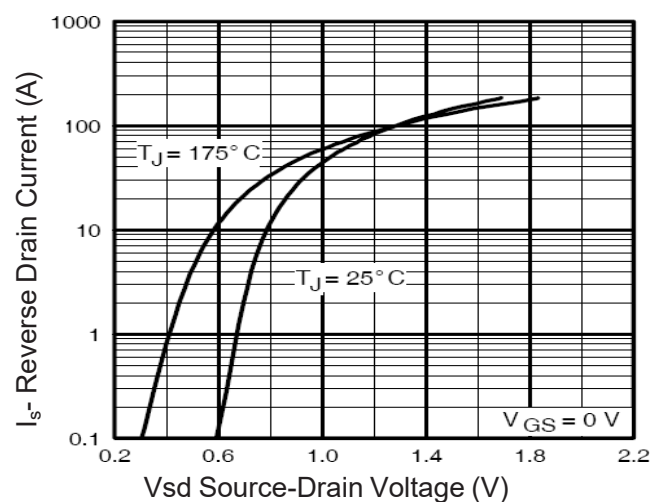
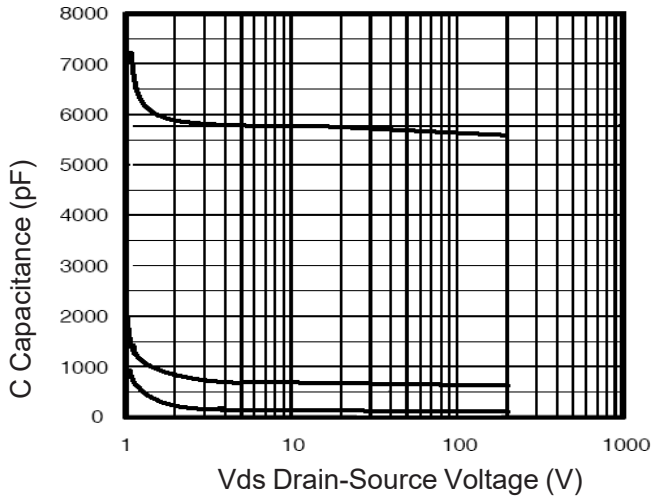
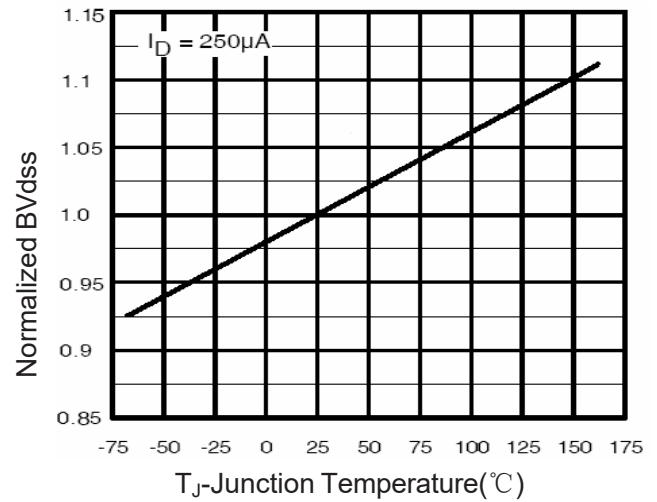
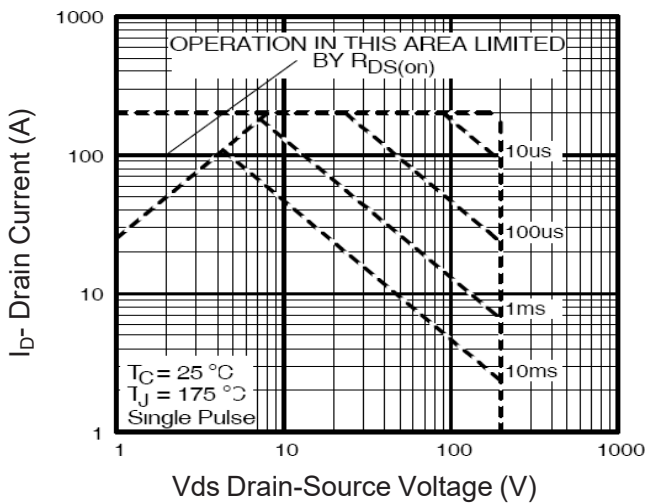
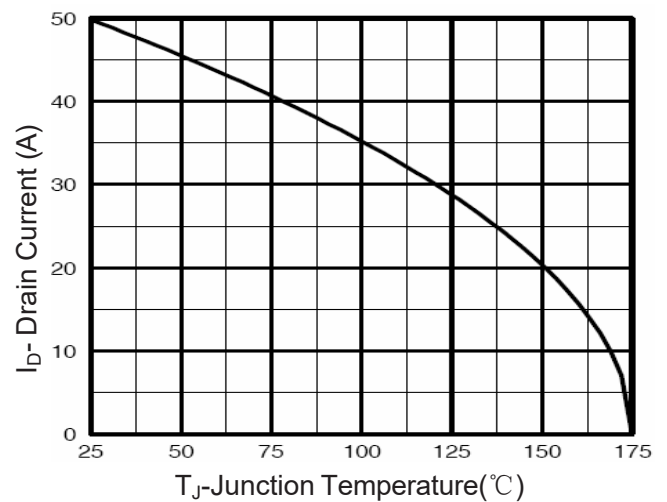
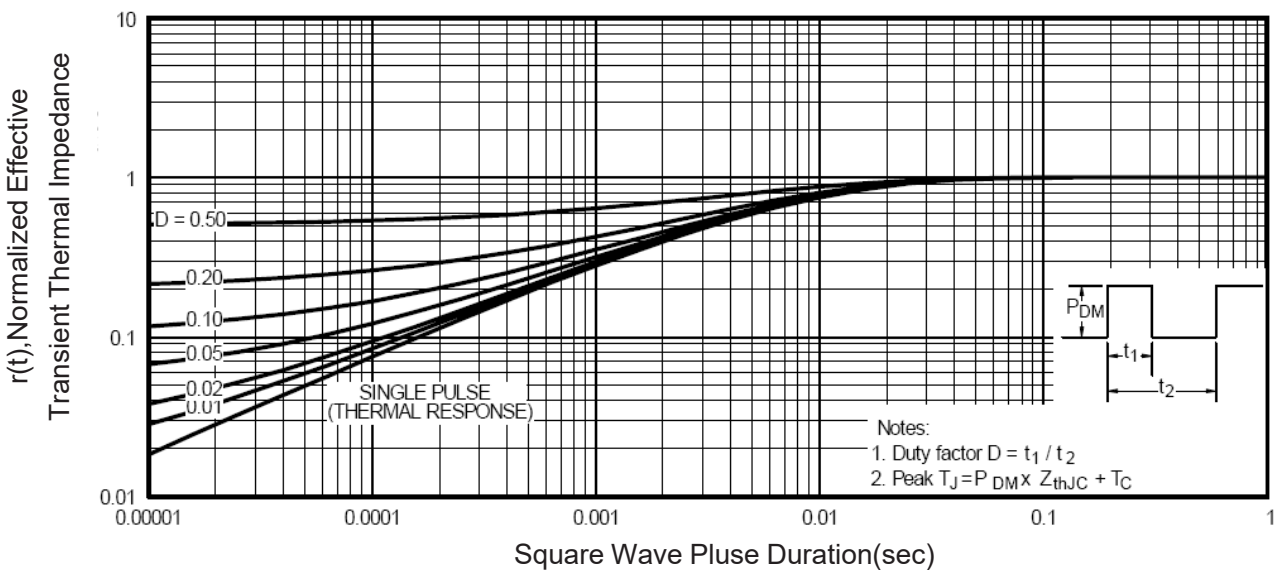


Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 BV_{DSS} vs Junction Temperature

Figure 8 Safe Operation Area

Figure 10 ID Current De-rating

Figure 11 Normalized Maximum Transient Thermal Impedance