

Description

The VSM280N06 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

Application

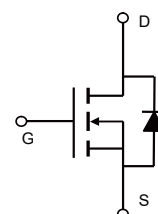
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

General Features

- $V_{DS} = 60V$, $I_D = 280A$
 $R_{DS(ON)} < 2.2m\Omega$ @ $V_{GS} = 10V$
- High density cell design for ultra low $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability



TOLL



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM280N06	VSM280N06-OL	TOLL	-	-	-

Absolute Maximum Ratings ($T_c = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	280	A
Drain Current-Continuous($T_c = 100^\circ C$)	$I_D(100^\circ C)$	224	A
Pulsed Drain Current	I_{DM}	1120	A
Maximum Power Dissipation	P_D	296	W
Derating factor		1.97	W/ $^\circ C$
Single pulse avalanche energy (Note 5)	E_{AS}	2040	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case(Note 2)	$R_{\theta JC}$	0.51	$^\circ C/W$
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Electrical Characteristics ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

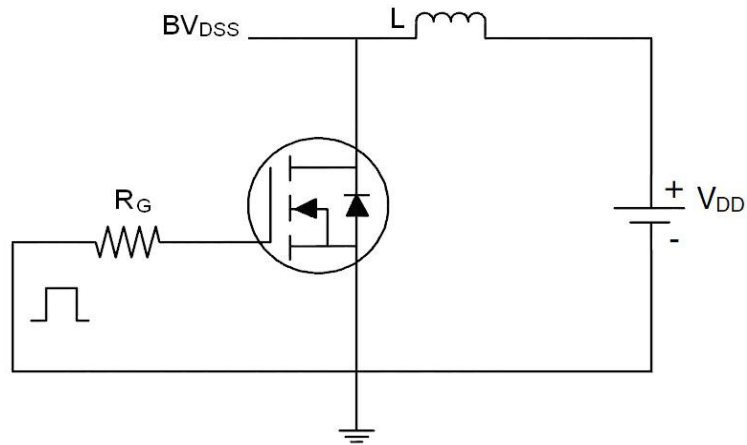
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2	3	4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =40A	-	1.9	2.2	mΩ
Forward Transconductance	g _{FS}	V _{DS} =10V, I _D =40A	-	70	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =30V, V _{GS} =0V, F=1.0MHz	-	10816	-	PF
Output Capacitance	C _{oss}		-	820	-	PF
Reverse Transfer Capacitance	C _{rss}		-	694	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =30V, I _D =2A, R _L =15Ω, R _G =2.5Ω, V _{GS} =10V	-	35	-	nS
Turn-on Rise Time	t _r		-	25	-	nS
Turn-Off Delay Time	t _{d(off)}		-	70	-	nS
Turn-Off Fall Time	t _f		-	13	-	nS
Total Gate Charge	Q _g	I _D =30A, V _{DD} =30V, V _{GS} =10V	-	197	-	nC
Gate-Source Charge	Q _{gs}		-	46	-	nC
Gate-Drain Charge	Q _{gd}		-	57	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =40A	-	0.8	1.2	V
Diode Forward Current (Note 2)	I _S		-	-	280	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 40A di/dt = 100A/μs(Note3)	-	31		nS
Reverse Recovery Charge	Q _{rr}		-	80		nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

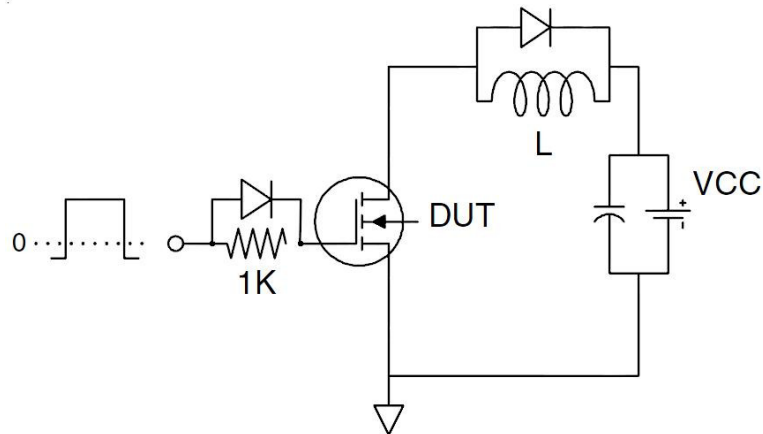
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=30V, V_G=10V, L=1mH, R_G=25\Omega$

Test circuit

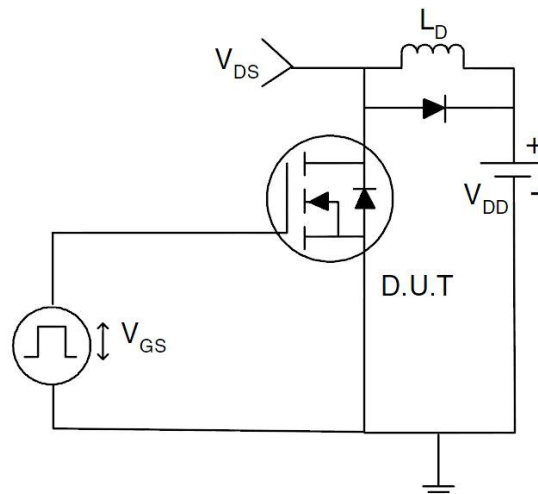
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

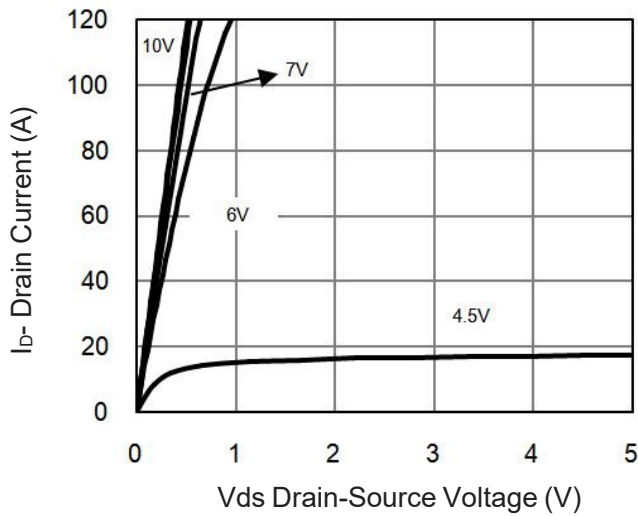


Figure 1 Output Characteristics

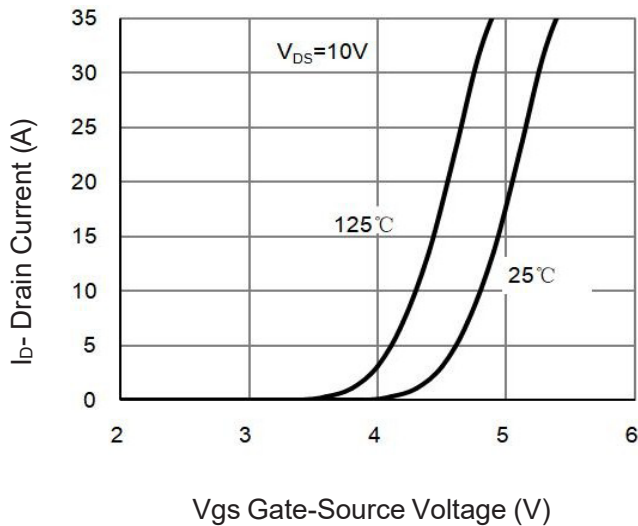


Figure 2 Transfer Characteristics

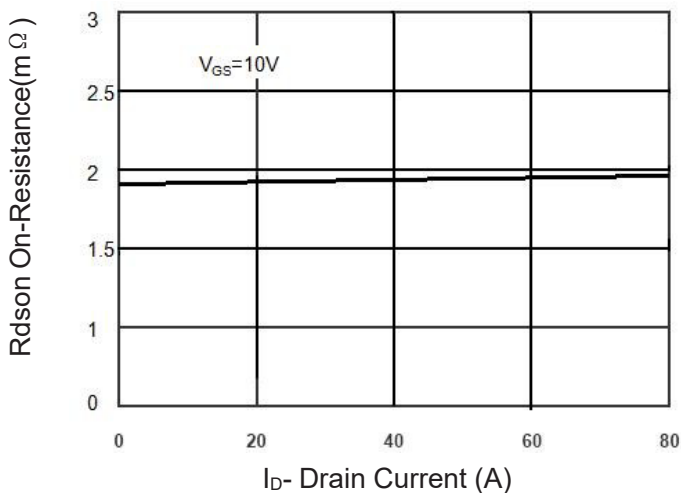


Figure 3 Rdson- Drain Current

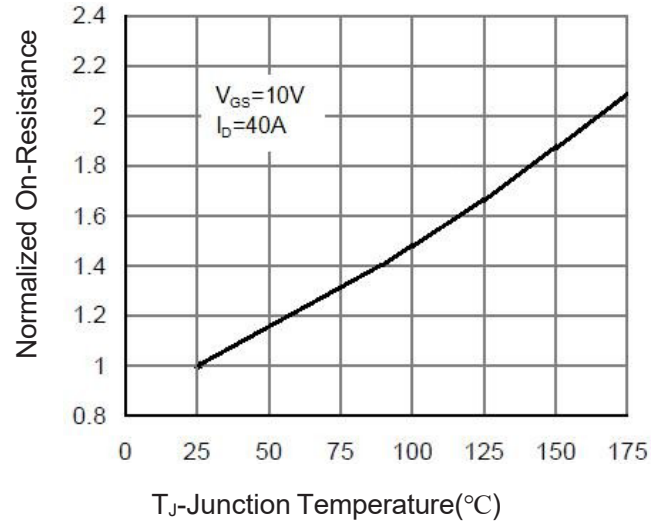


Figure 4 Rdson-Junction Temperature

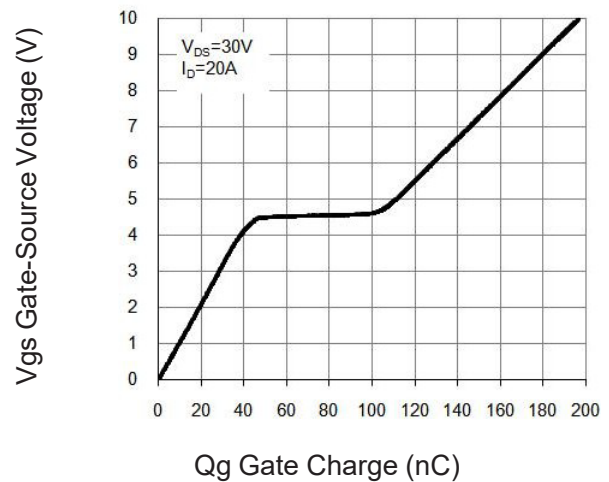


Figure 5 Gate Charge

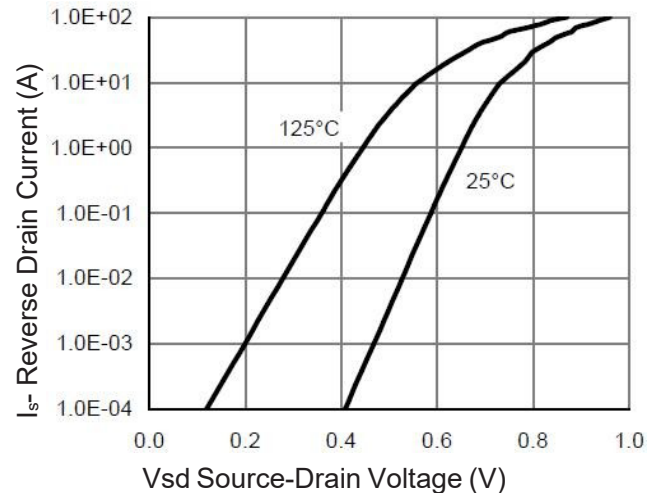
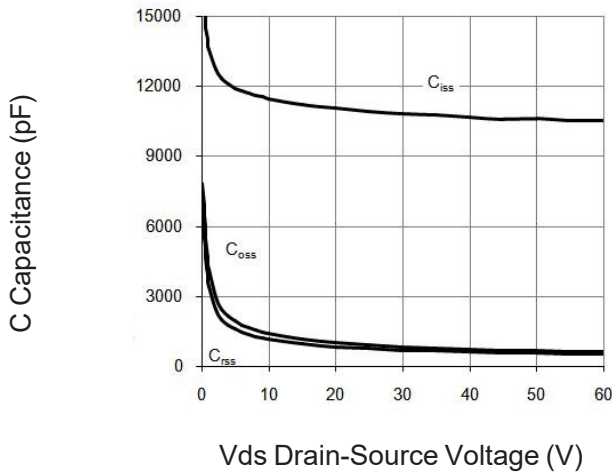
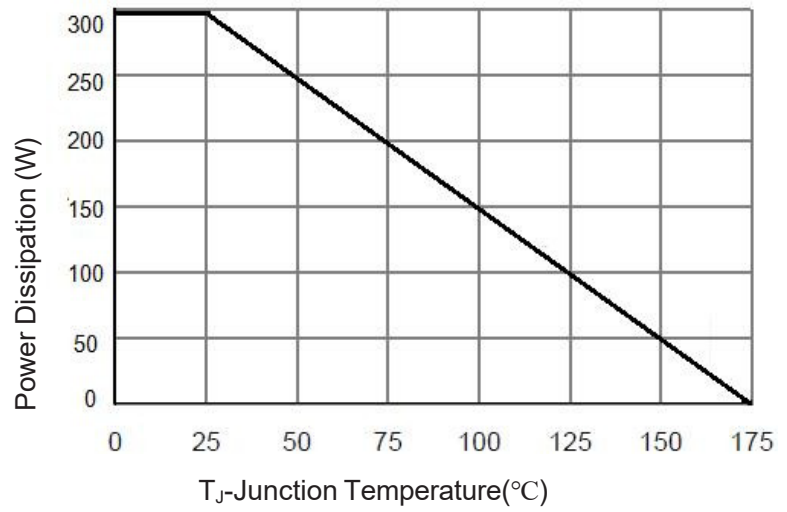


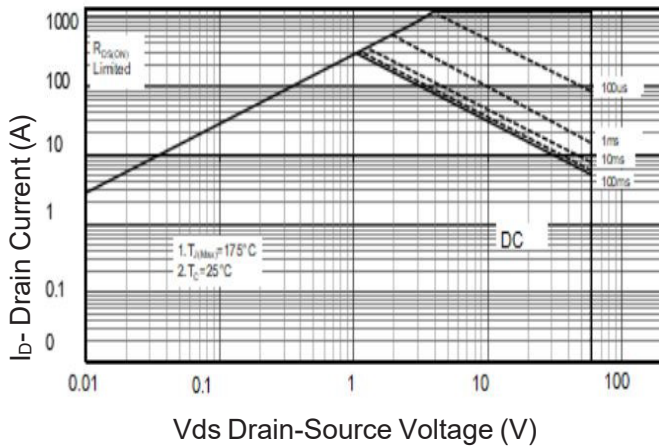
Figure 6 Source- Drain Diode Forward



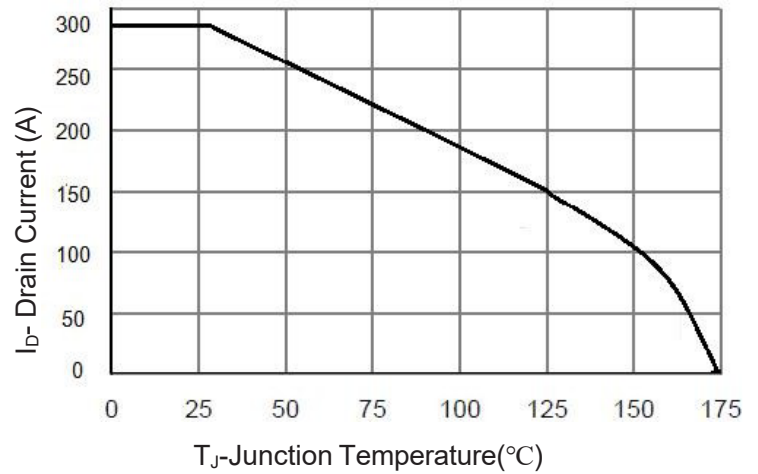
Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



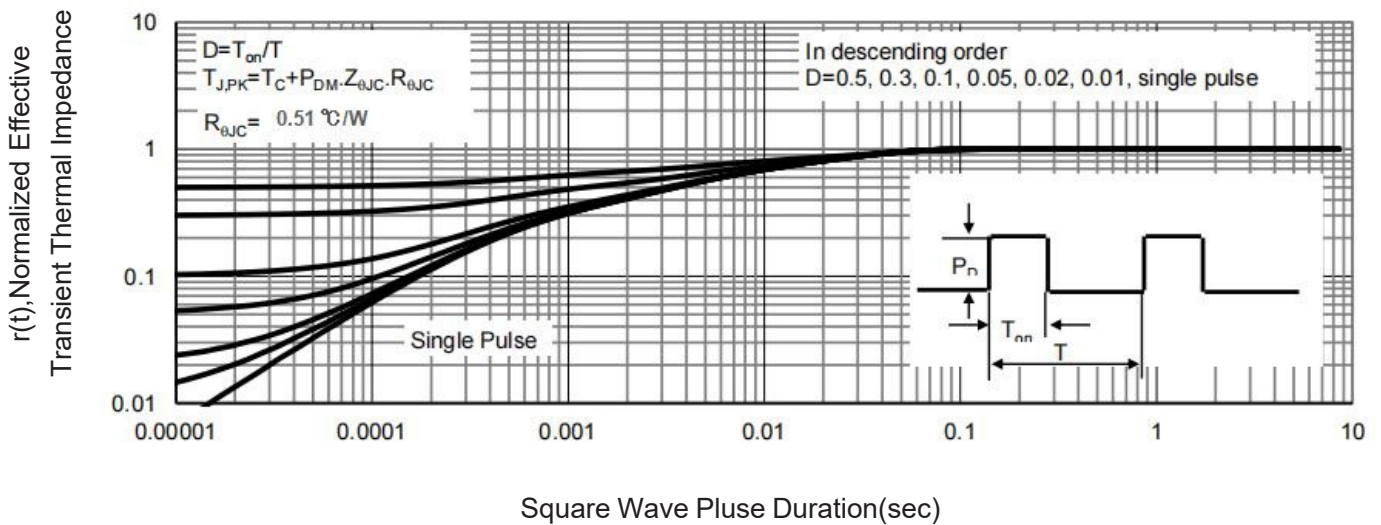
TJ-Junction Temperature(°C)
Figure 9 BV_{DSS} vs Junction Temperature



Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area



TJ-Junction Temperature(°C)
Figure 10 V_{GS(th)} vs Junction Temperature



Square Wave Pluse Duration(sec)
Figure 11 Normalized Maximum Transient Thermal Impedance