

Description

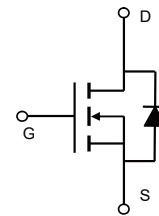
The series of devices uses **Super Trench II** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

General Features

- $V_{DS}=100V, I_D=110A$
 $R_{DS(ON)}=5.4m\Omega$, typical (TO-220)@ $V_{GS}=10V$
 $R_{DS(ON)}=5.2m\Omega$, typical (TO-263)@ $V_{GS}=10V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VST10N050	VST10N050-T3	TO-263	-	-	-

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	110	A
Drain Current-Continuous($T_C=100^{\circ}C$)	$I_D(100^{\circ}C)$	72	A
Pulsed Drain Current	I_{DM}	440	A
Maximum Power Dissipation	P_D	150	W
Derating factor		1.0	W/ $^{\circ}C$
Single pulse avalanche energy (Note 5)	E_{AS}	680	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^{\circ}C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	1.0	$^{\circ}\text{C/W}$
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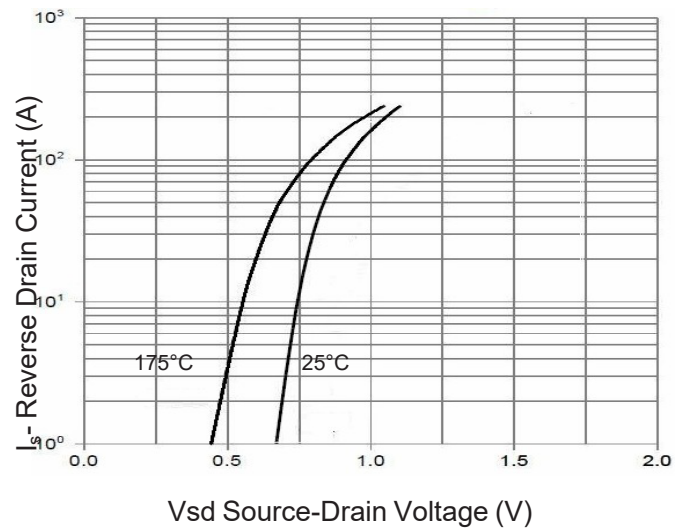
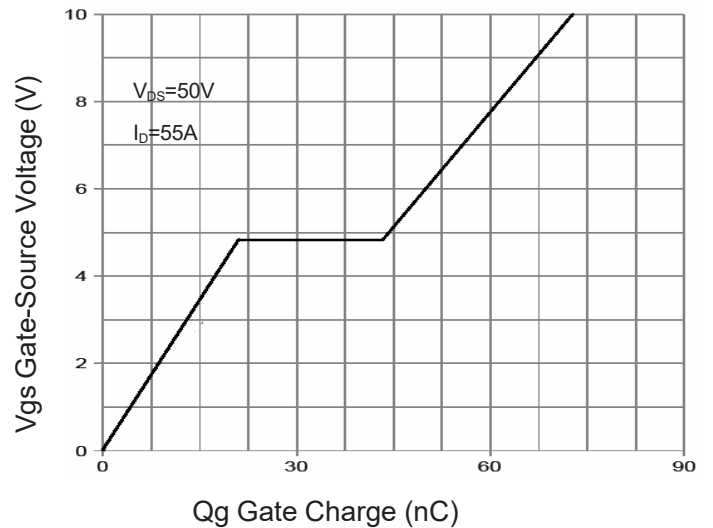
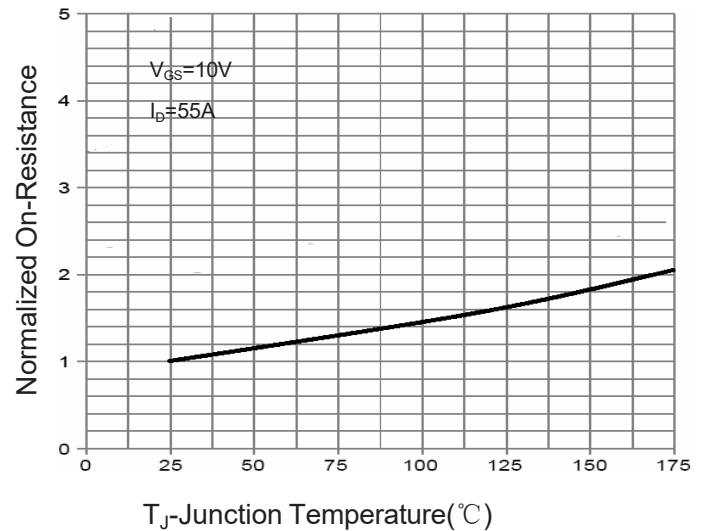
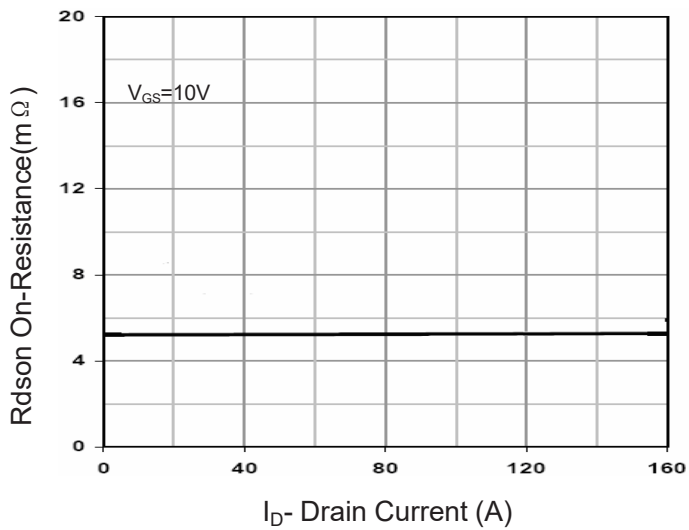
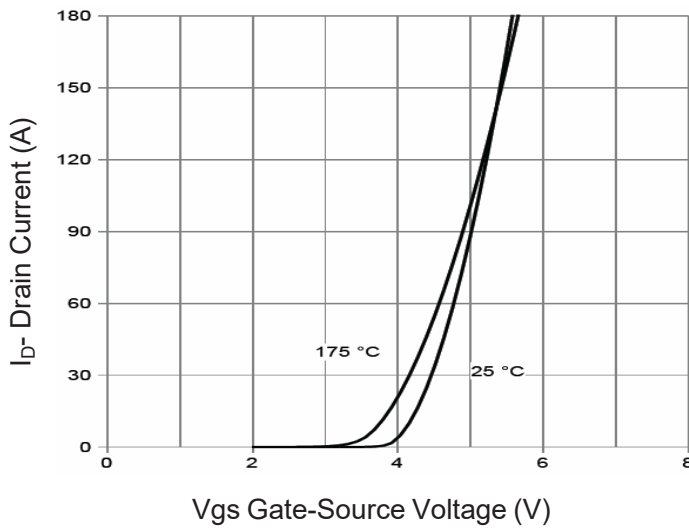
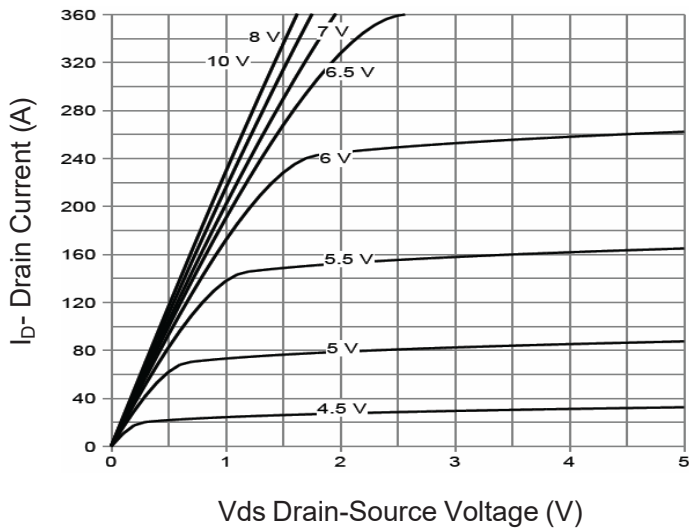
Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

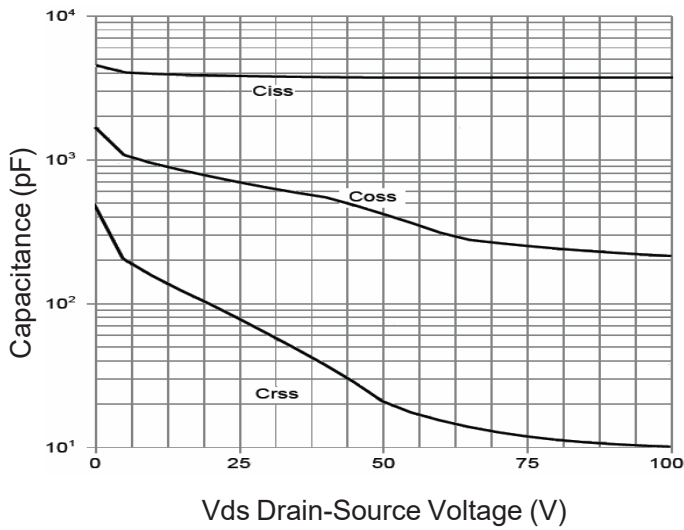
Parameter	Symbol	Condition		Min	Typ	Max	Unit
Off Characteristics							
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA		100		-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V,V _{GS} =0V		-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V		-	-	±100	nA
On Characteristics (Note 3)							
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA		2.0	3.0	4.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =55A	TO-220	-	5.4	5.7	mΩ
			TO-263		5.2	5.7	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V,I _D =55A			60	-	S
Dynamic Characteristics (Note4)							
Input Capacitance	C _{ISS}	V _{DS} =50V,V _{GS} =0V, F=1.0MHz		-	3850	-	PF
Output Capacitance	C _{OSS}			-	410	-	PF
Reverse Transfer Capacitance	C _{rss}			-	20	-	PF
Switching Characteristics (Note 4)							
Turn-on Delay Time	t _{d(on)}	V _{DD} =50V,I _D =55A V _{GS} =10V,R _G =1.6Ω		-	21	-	nS
Turn-on Rise Time	t _r			-	61	-	nS
Turn-Off Delay Time	t _{d(off)}			-	40	-	nS
Turn-Off Fall Time	t _f			-	12	-	nS
Total Gate Charge	Q _g	V _{DS} =50V,I _D =55A, V _{GS} =10V		-	72	-	nC
Gate-Source Charge	Q _{gs}			-	21		nC
Gate-Drain Charge	Q _{gd}			-	22		nC
Drain-Source Diode Characteristics							
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V,I _S =50A		-		1.2	V
Diode Forward Current (Note 2)	I _S			-	-	100	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = I _S di/dt = 100A/μs ^(Note3)		-	67	-	nS
Reverse Recovery Charge	Q _{rr}			-	137	-	nC

Notes:

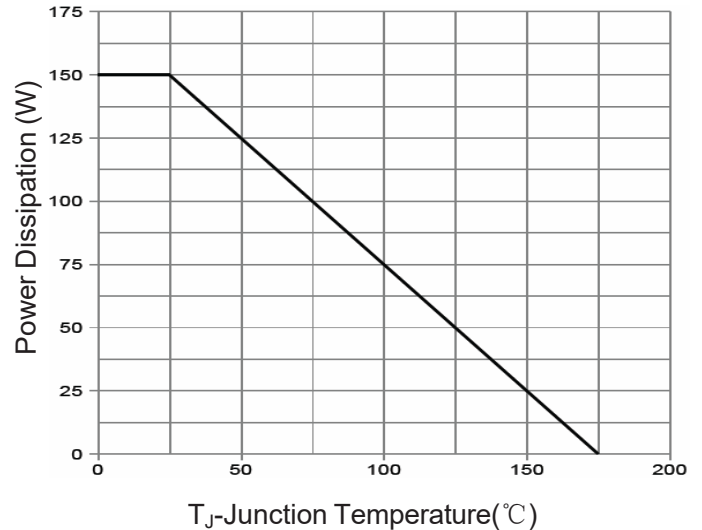
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

Typical Electrical and Thermal Characteristics

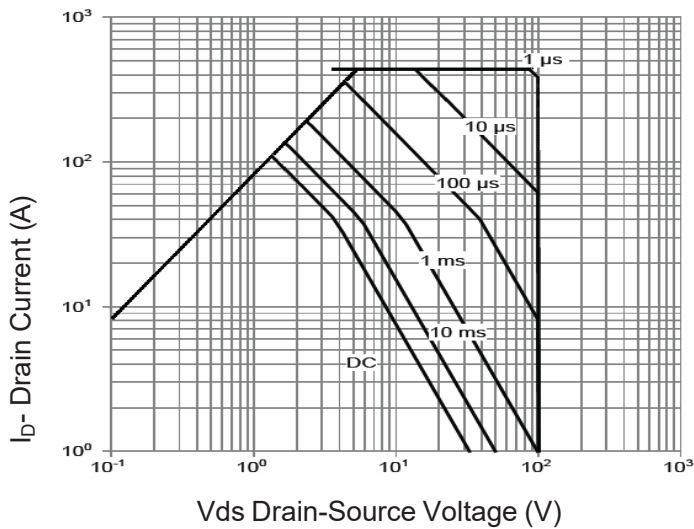




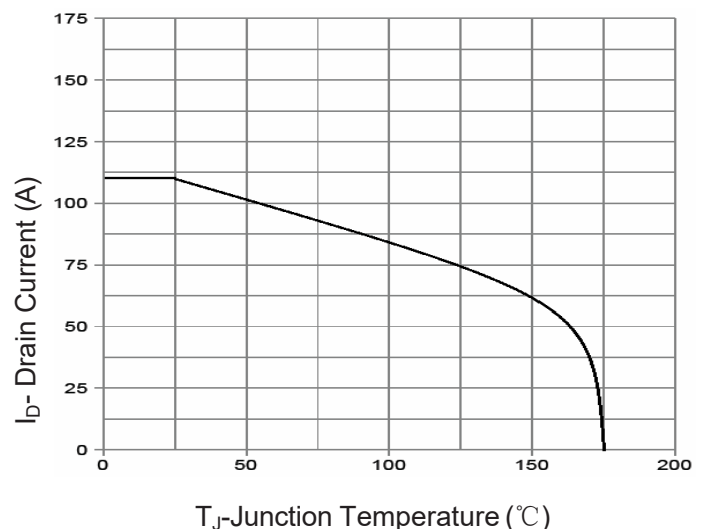
Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



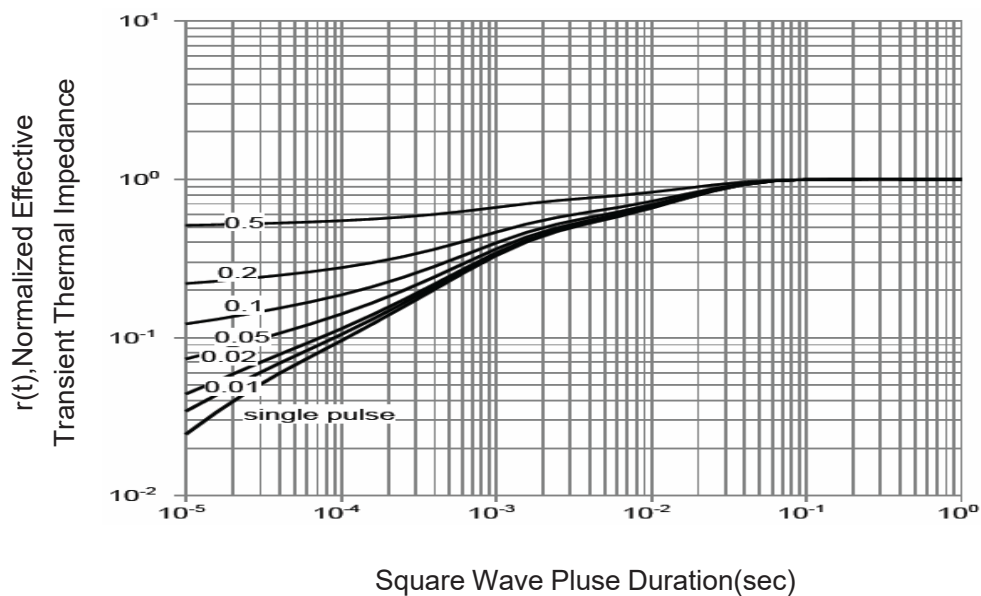
TJ-Junction Temperature(°C)
Figure 9 Power De-rating



Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area



TJ-Junction Temperature (°C)
Figure 10 Current De-rating



Square Wave Pluse Duration(sec)
Figure 11 Normalized Maximum Transient Thermal Impedance