

Description

The VST04N010 uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

General Features

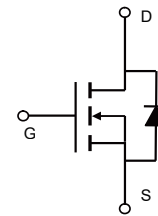
- $V_{DS} = 40V, I_D = 185A$
 $R_{DS(ON)} = 1.0m\Omega$ (typical) @ $V_{GS} = 10V$
 $R_{DS(ON)} = 1.4m\Omega$ (typical) @ $V_{GS} = 4.5V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification



DFN5x6



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VST04N010	VST04N010-D56	DFN5x6	-	-	-

Absolute Maximum Ratings ($T_c = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous (Silicon Limited)	I_D	185	A
Drain Current-Continuous($T_c = 100^\circ C$)	$I_D(100^\circ C)$	140	A
Pulsed Drain Current ^(Note 1) (Package Limited)	I_{DM}	400	A
Maximum Power Dissipation	P_D	160	W
Derating factor		1.28	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	1200	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

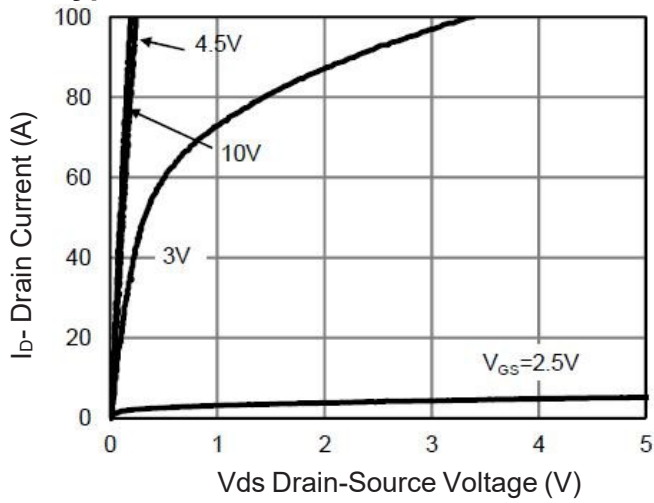
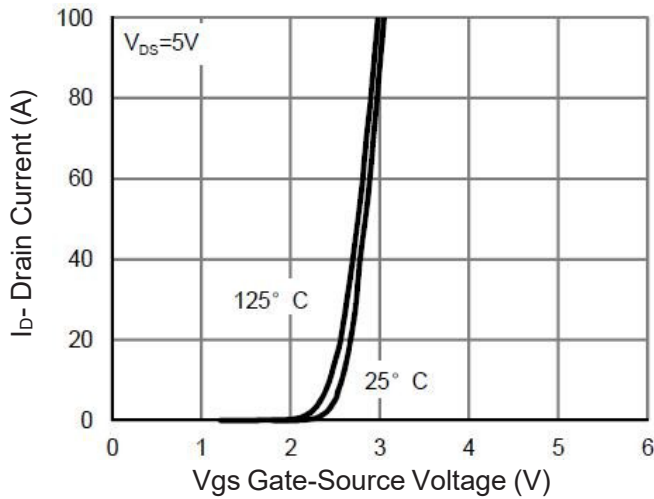
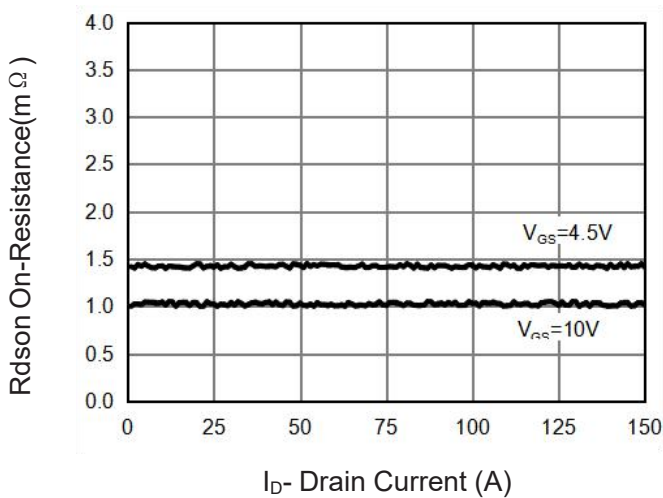
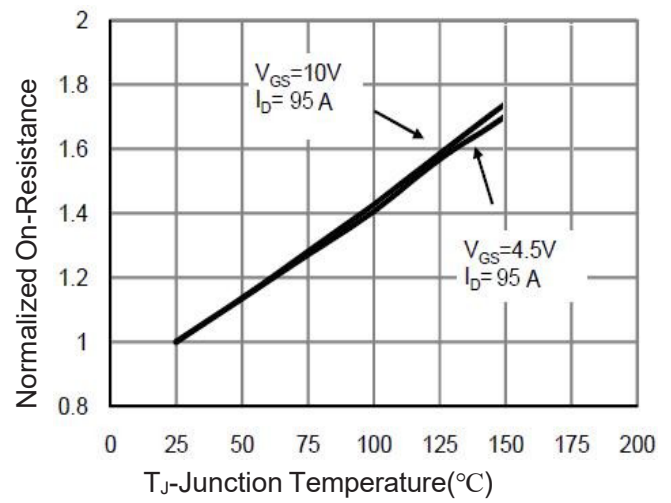
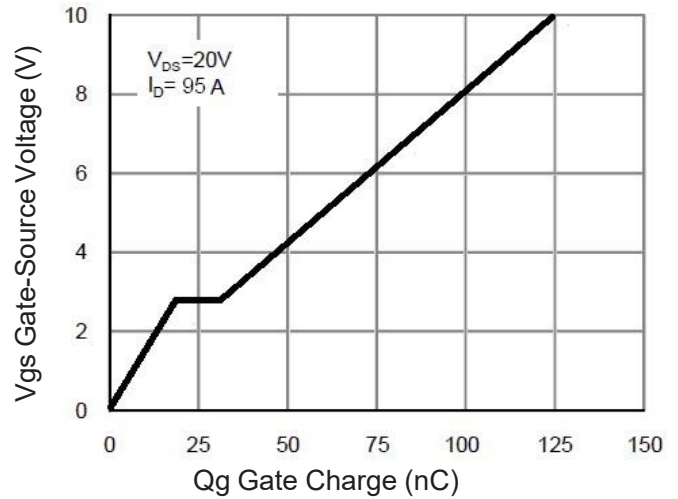
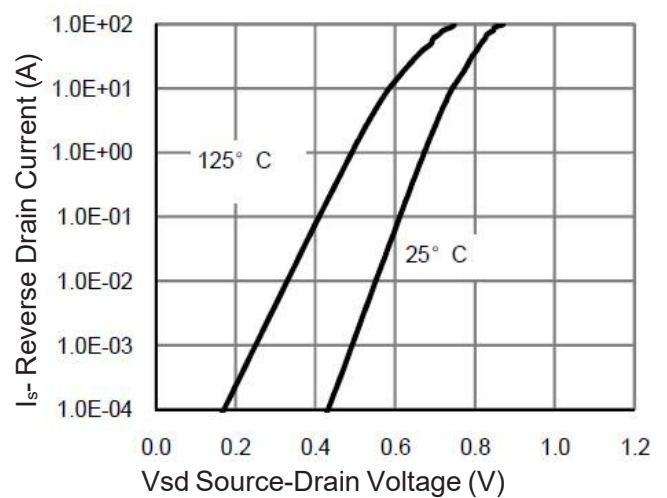
Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.78	$^{\circ}\text{C/W}$
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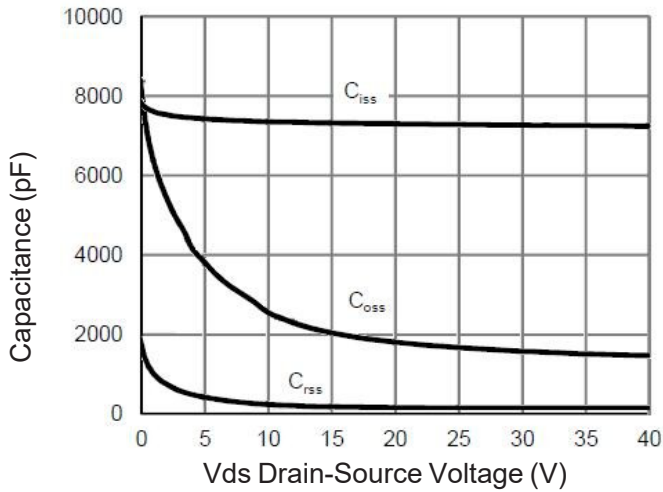
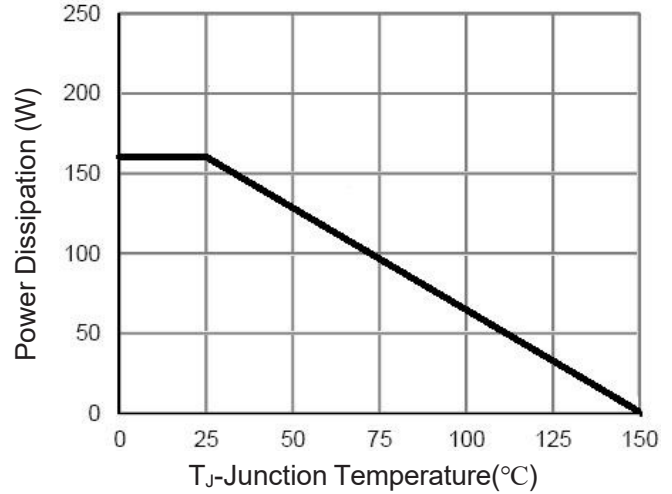
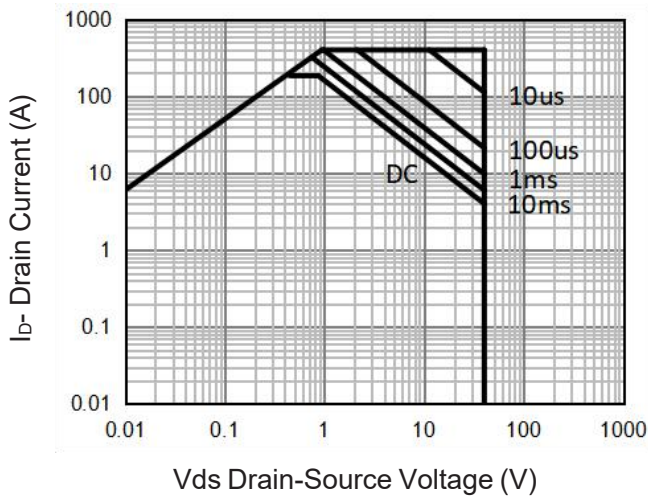
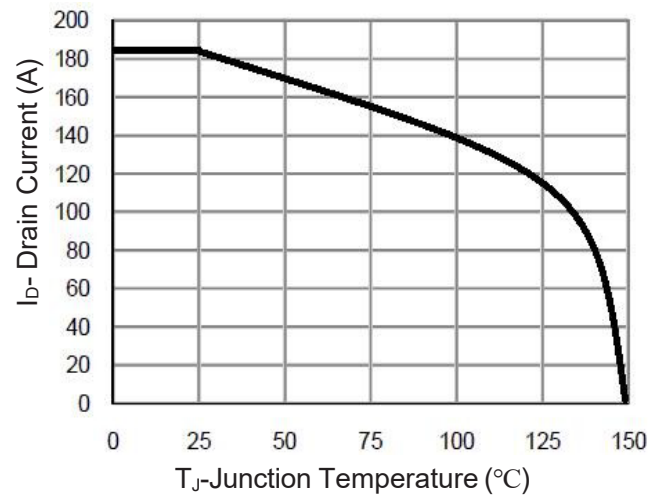
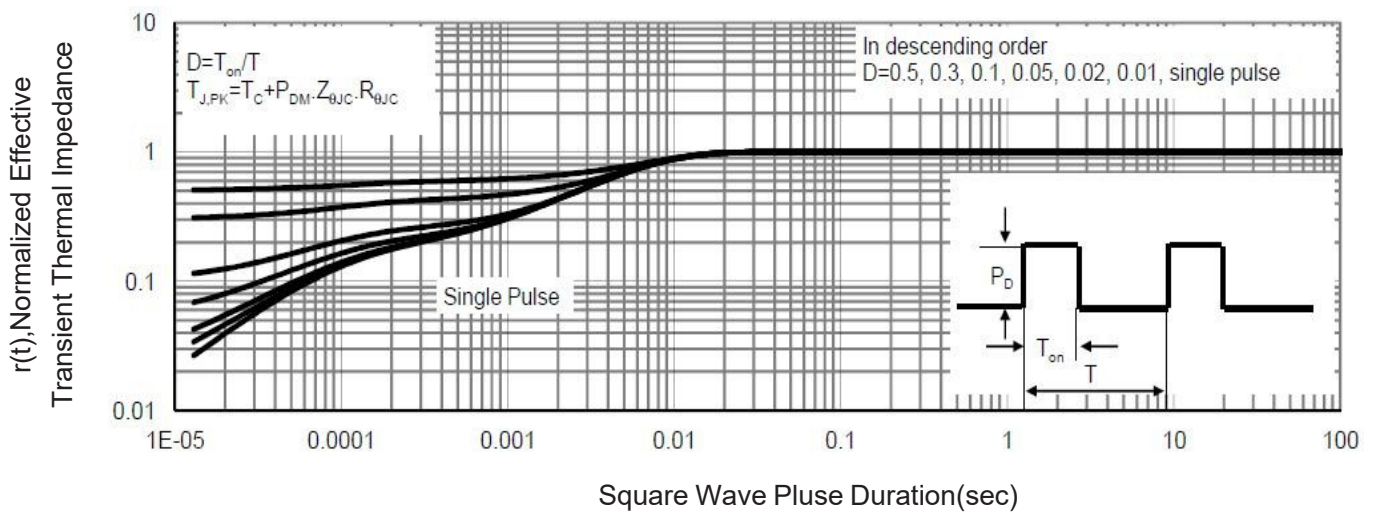
Electrical Characteristics ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	40		-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.2	1.5	2.2	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =95A	-	1.0	1.2	mΩ
		V _{GS} =4.5V, I _D =95A	-	1.4	1.7	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =95A	-	80	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =20V, V _{GS} =0V, F=1.0MHz	-	7400	8800	PF
Output Capacitance	C _{oss}		-	1930	2300	PF
Reverse Transfer Capacitance	C _{rss}		-	110	130	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =20V, I _D =95A V _{GS} =10V, R _G =1.6Ω	-	14.1	-	nS
Turn-on Rise Time	t _r		-	7.9	-	nS
Turn-Off Delay Time	t _{d(off)}		-	56.5	-	nS
Turn-Off Fall Time	t _f		-	9.6	-	nS
Total Gate Charge	Q _g	V _{DS} =20V, I _D =95A, V _{GS} =10V	-	125	140	nC
Gate-Source Charge	Q _{gs}		-	18		nC
Gate-Drain Charge	Q _{gd}		-	13		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =95A	-		1.2	V
Diode Forward Current (Note 2)	I _S		-	-	185	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = I _S	-		35	nS
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs (Note3)	-		124	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^{\circ}\text{C}, V_{DD}=20V, V_G=10V, L=0.5\text{mH}, R_g=25\Omega$

Typical Electrical and Thermal Characteristics

Figure 1 Output Characteristics

Figure 2 Transfer Characteristics

Figure 3 Rdson- Drain Current

Figure 4 Rdson-Junction Temperature

Figure 5 Gate Charge

Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 Power De-rating

Figure 8 Safe Operation Area

Figure 10 Current De-rating

Figure 11 Normalized Maximum Transient Thermal Impedance