Description

The VST15N300 uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g. This device is ideal for high-frequency switching and synchronous rectification.

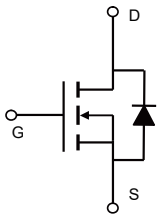
General Features

- V_{DS} =150V,I_D =8A
  $R_{DS(ON)}$ < 35mΩ @ V_{GS}=10V (Typ: 30mΩ)
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature

Application

- DC/DC converters and Off-Line UPS
- High Voltage Synchronous Rectifier
- Hard switched and high frequency circuits
- Uninterruptible power supply

SOP-8



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VST15N300	VST15N300-S8	SOP-8	Ø330mm	12mm	4000 units

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	150	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current-Continuous		I_D	8	A
Drain Current-Continuous(T_A=100℃)		I_D (100℃)	6	A
Pulsed Drain Current		I_{DM}	32	A
Single pulse avalanche energy(Note 1)		E_{AS}	108	mJ
Maximum Power Dissipation	T_A = 25 °C	P_D	5	W
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient(Note 4)	$R_{\theta JA}$	25	℃/W

Electrical Characteristics (T_A=25℃unless otherwise noted)

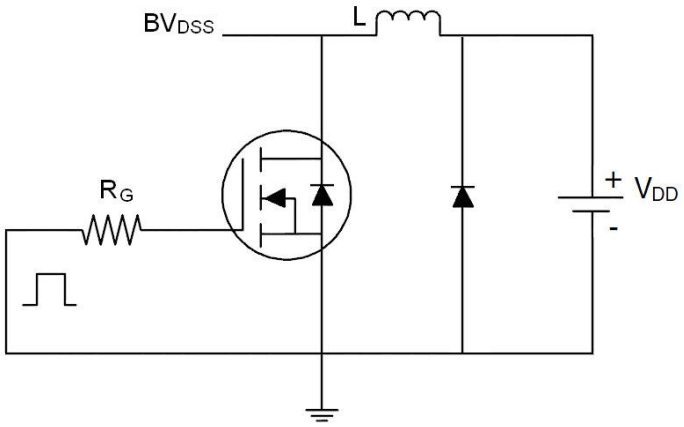
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	150	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=150V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2.5	3.4	4.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=8A	-	30	35	mΩ
Forward Transconductance	g_{FS}	V_{DS}=10V,I_D=8A	-	10	-	S
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=75V,V_{GS}=0V, F=1.0MHz	-	1125	-	PF
Output Capacitance	C_{oss}		-	170	-	PF
Reverse Transfer Capacitance	C_{rss}		-	20	-	PF
Switching Characteristics (Note 2)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=75V, I_D=8A V_{GS}=10V,R_G=3Ω	-	15	-	nS
Turn-on Rise Time	t_r		-	5	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	21	-	nS
Turn-Off Fall Time	t_f		-	8	-	nS
Total Gate Charge	Q_g	V_{DS}=75V,I_D=4A, V_{GS}=10V	-	19.8	-	nC
Gate-Source Charge	Q_{gs}		-	6.1	-	nC
Gate-Drain Charge	Q_{gd}		-	5.6	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=8A	-	-	1.2	V
Diode Forward Current	I_S		-	-	8	A
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F = I_S di/dt = 100A/μs	-	34	-	nS
Reverse Recovery Charge	Qrr		-	80	-	nC

Notes:

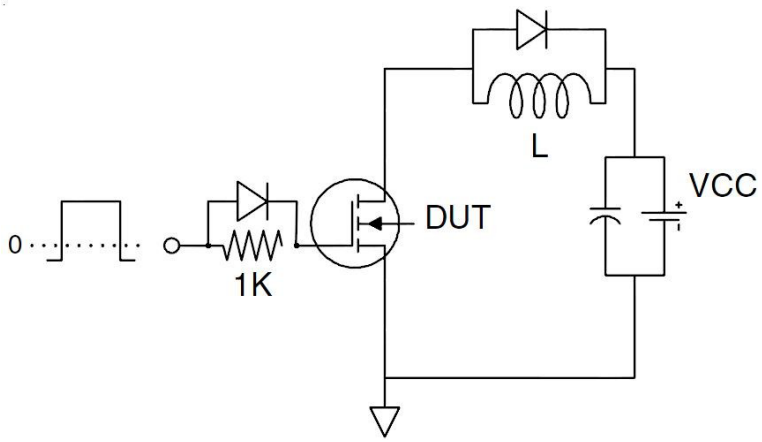
1. EAS condition : Tj=25℃,V_{DD}=50V,V_G=10V,L=0.5mH,Rg=25Ω
2. Guaranteed by design, not subject to production
3. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.
4. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.

Test Circuit

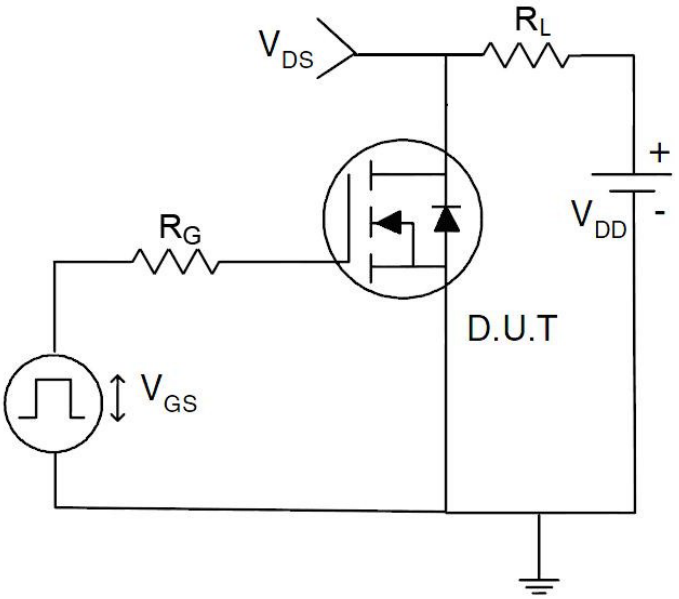
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

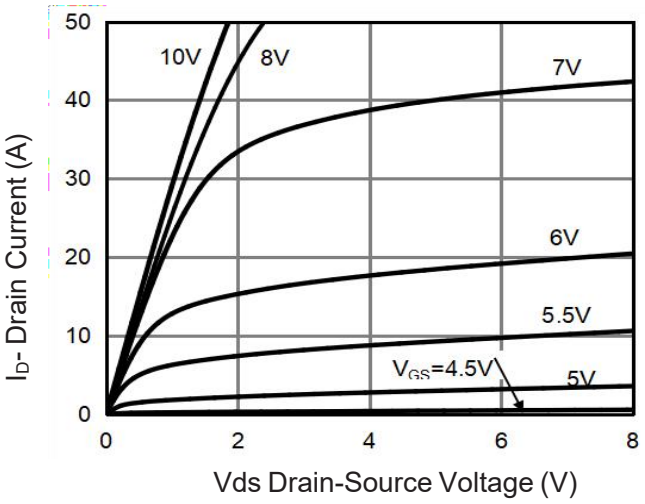


Figure 1 Output Characteristics

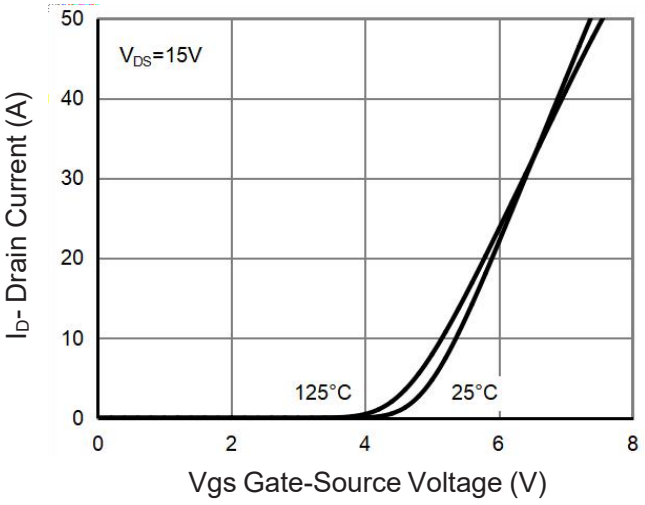


Figure 2 Transfer Characteristics

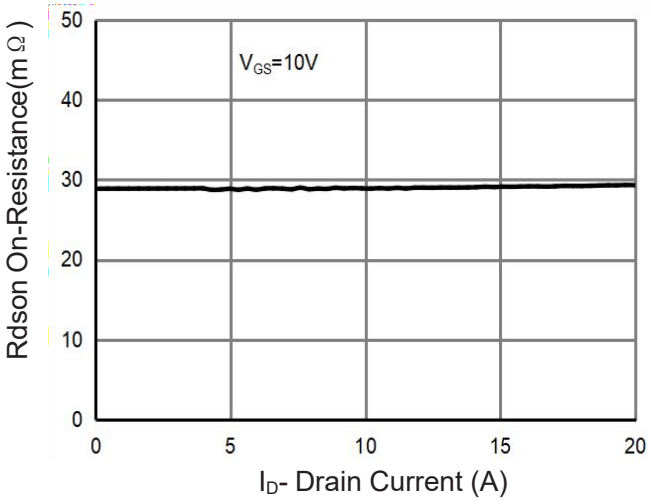


Figure 3 Rdson- Drain Current

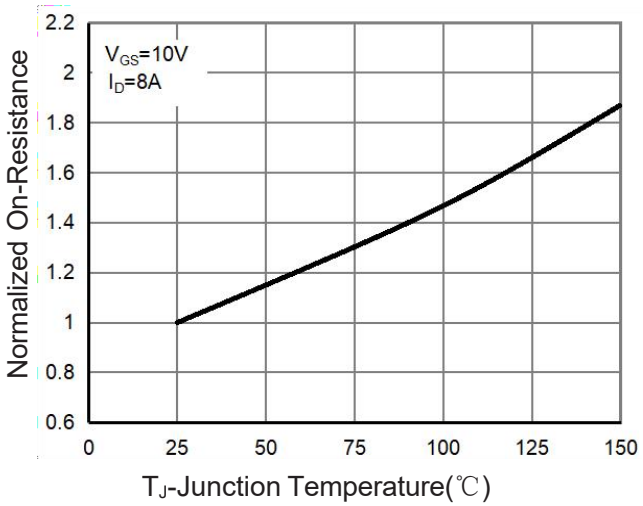


Figure 4 Rdson-JunctionTemperature

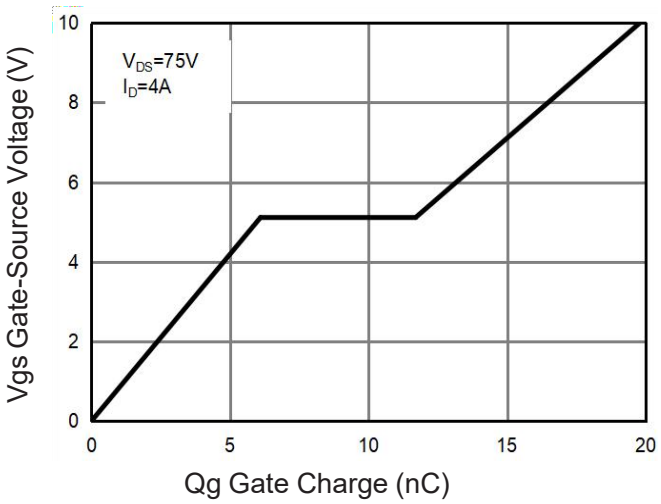


Figure 5 Gate Charge

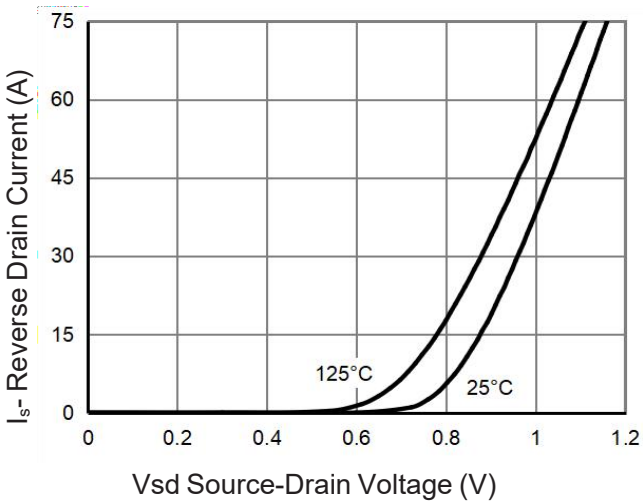


Figure 6 Source- Drain Diode Forward

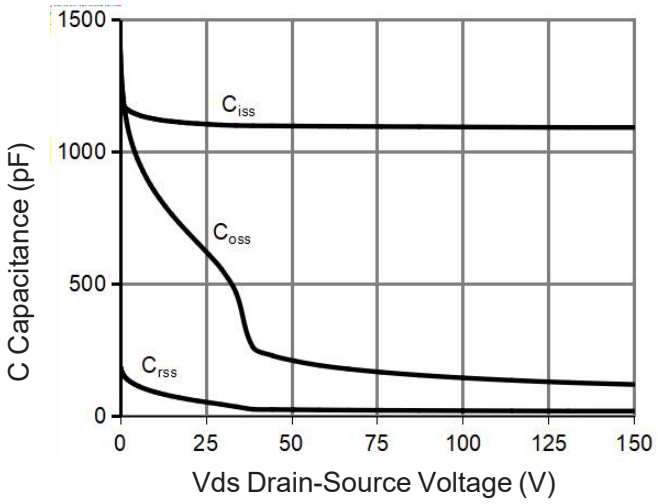


Figure 7 Capacitance vs Vds

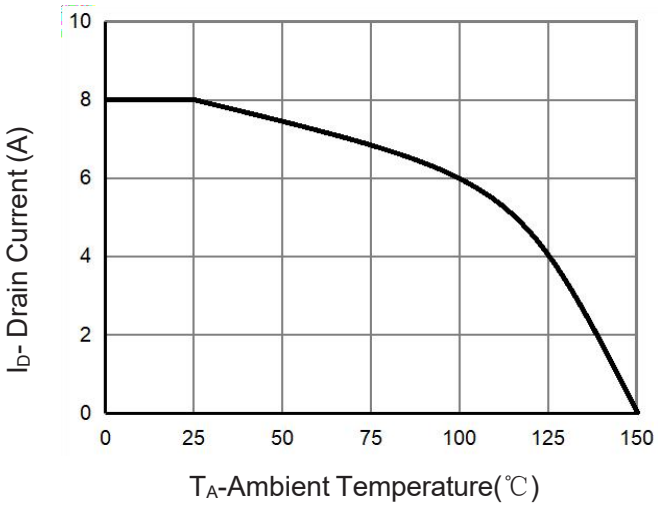


Figure 9 Current De-rating

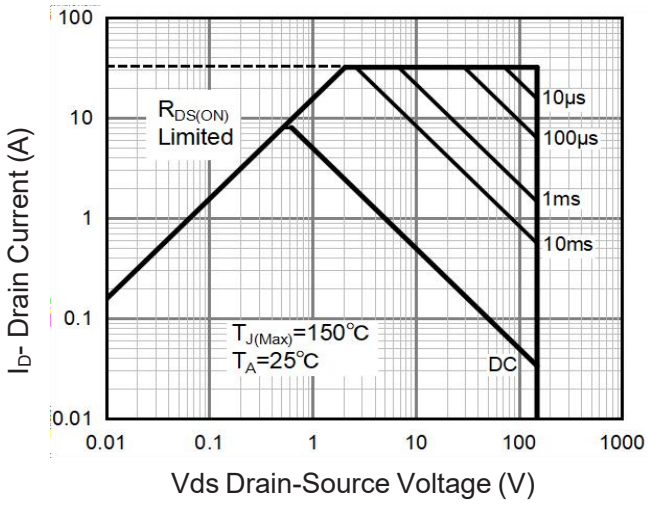


Figure 8 Safe Operation Area (Note3)

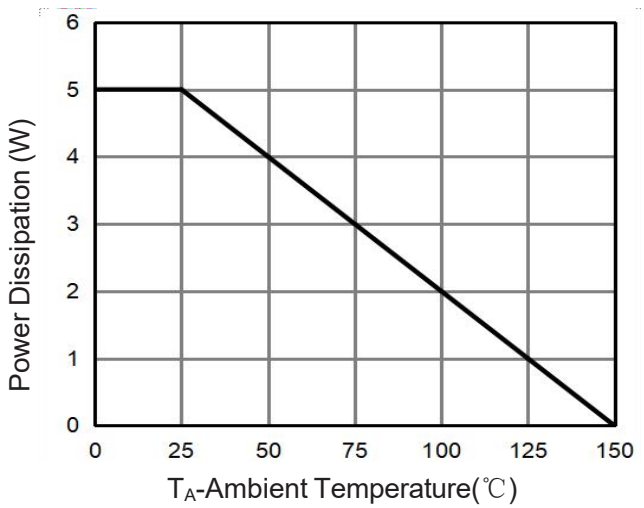


Figure 10 Power De-rating

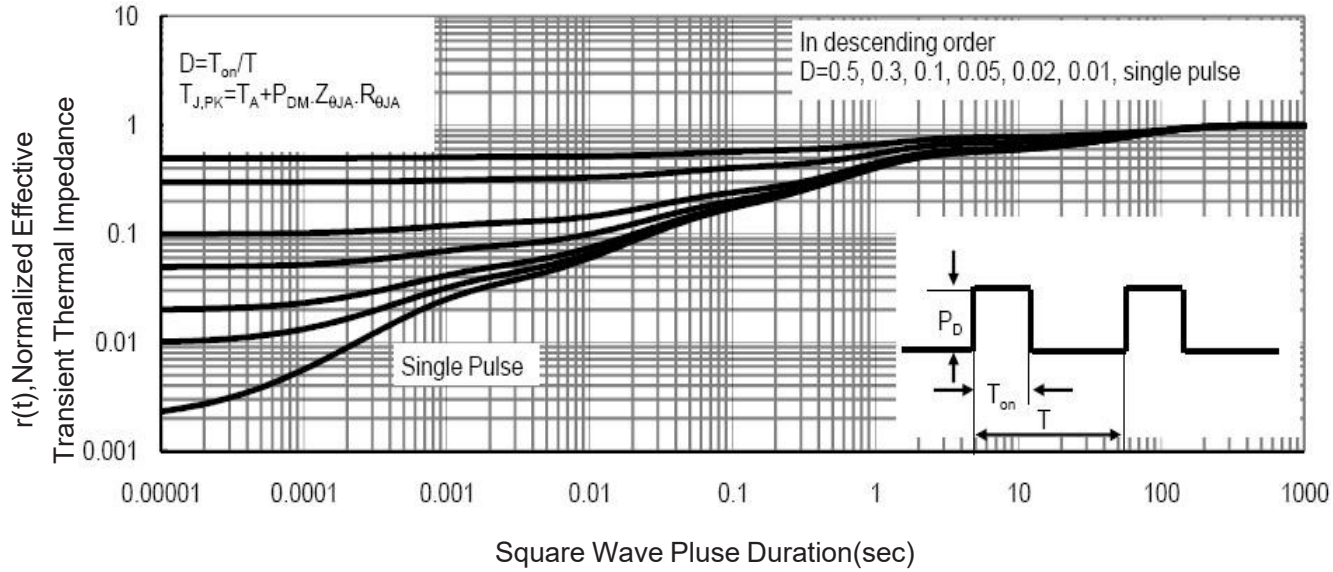


Figure 11 Normalized Maximum Transient Thermal Impedance