

Description

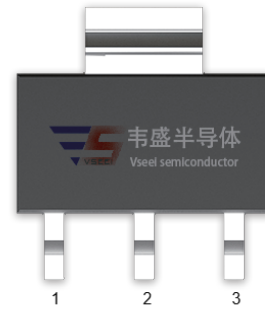
The VST10N210 uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

General Features

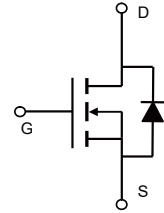
- $V_{DS} = 100V, I_D = 9A$
 $R_{DS(ON)} < 27m\Omega @ V_{GS}=10V$ (Typ:21m Ω)
 $R_{DS(ON)} < 37m\Omega @ V_{GS}=4.5V$ (Typ:30m Ω)
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



SOT-223



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VST10N210	VST10N210-S23	SOT-223	Ø330mm	12mm	2500 units

Absolute Maximum Ratings ($T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	9	A
Drain Current-Pulsed (Note 1)	I_{DM}	36	A
Single pulse avalanche energy (Note 5)	E_{AS}	96	mJ
Maximum Power Dissipation	P_D	2.5	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^{\circ}C$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	50	$^{\circ}C/W$
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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

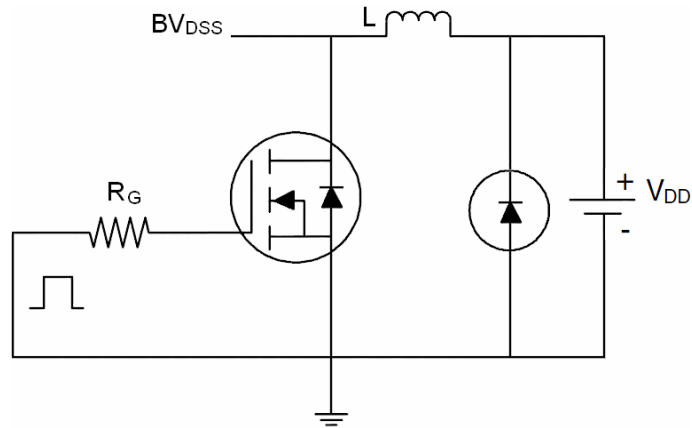
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.2	1.9	2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =9A	-	21	27	mΩ
		V _{GS} =4.5V, I _D =9A	-	30	37	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =9A	-	12	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, F=1.0MHz	-	1600	-	PF
Output Capacitance	C _{oss}		-	139	-	PF
Reverse Transfer Capacitance	C _{rss}		-	11	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =50V, R _L =5.5Ω V _{GS} =10V, R _G =2.5Ω	-	10	-	nS
Turn-on Rise Time	t _r		-	4	-	nS
Turn-Off Delay Time	t _{d(off)}		-	22	-	nS
Turn-Off Fall Time	t _f		-	5	-	nS
Total Gate Charge	Q _g	V _{DS} =50V, I _D =9A, V _{GS} =10V	-	26	-	nC
Gate-Source Charge	Q _{gs}		-	7.4	-	nC
Gate-Drain Charge	Q _{gd}		-	3.8	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =9A	-	-	1.2	V
Diode Forward Current (Note 2)	I _S		-	-	9	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F =4.5A	-	34.6	-	nS
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs (Note3)	-	57.7	-	nC

Notes:

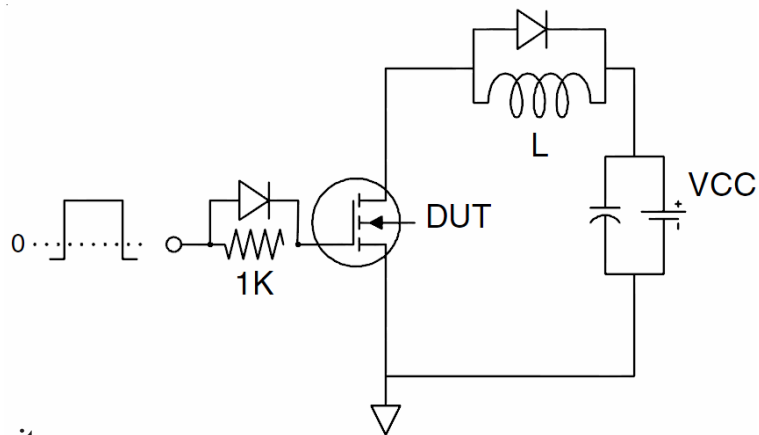
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to product
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test Circuit

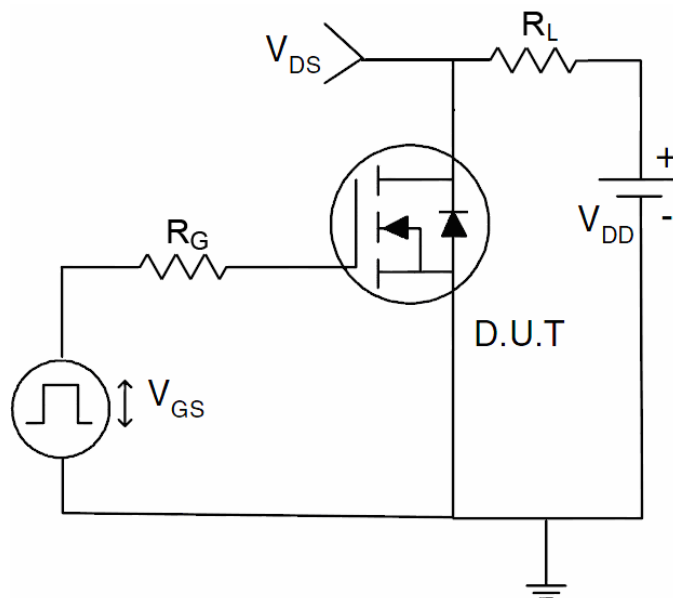
1) E_{AS} test circuit



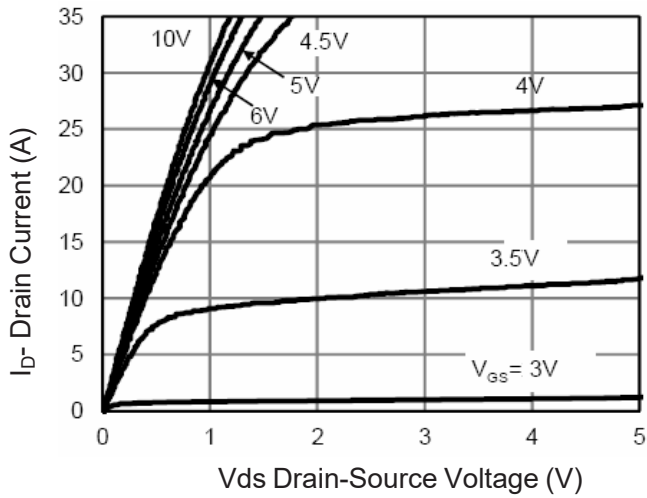
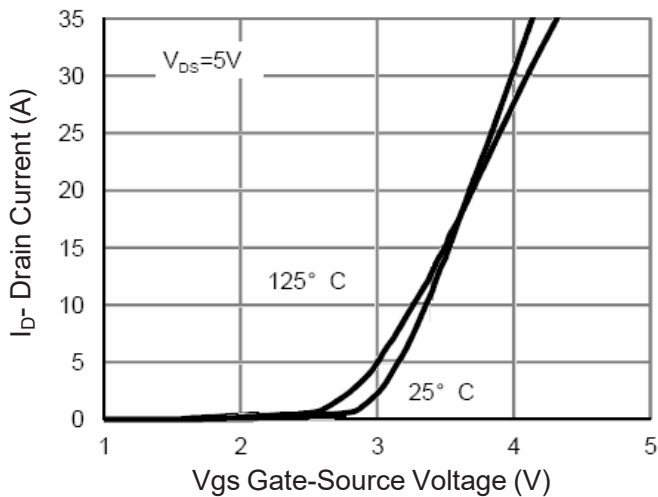
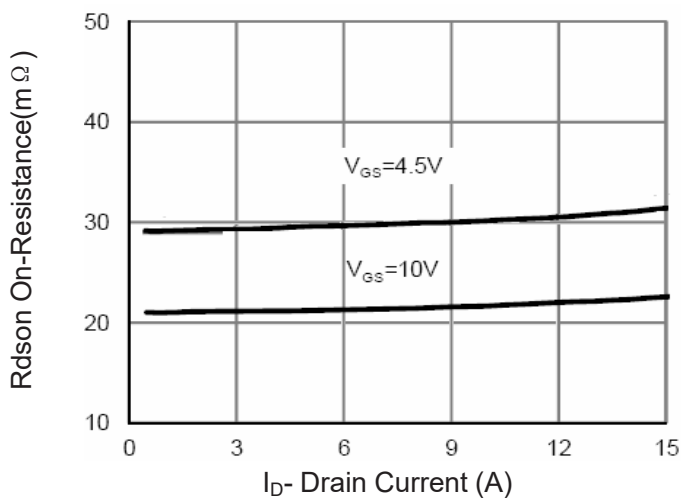
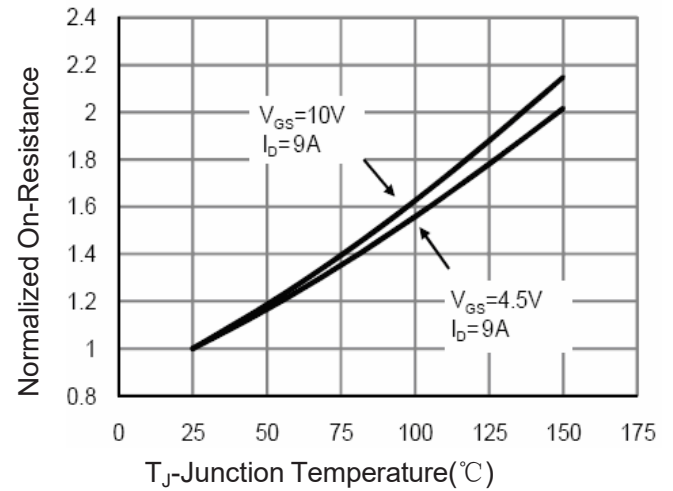
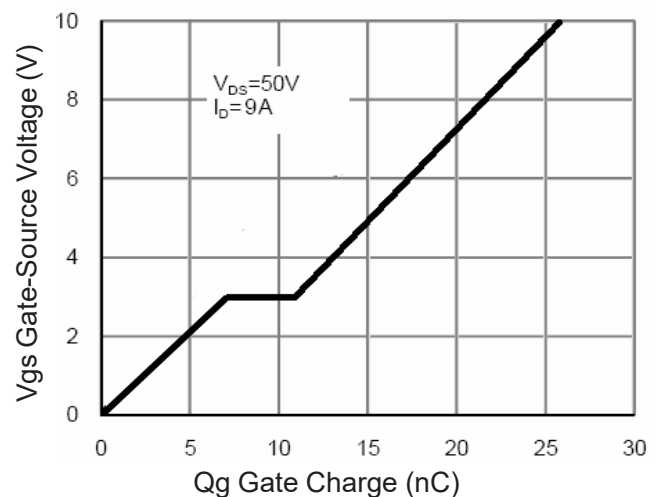
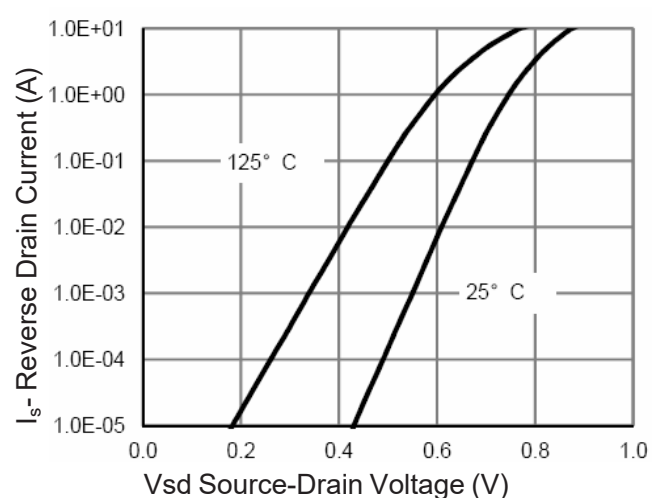
2) Gate charge test circuit

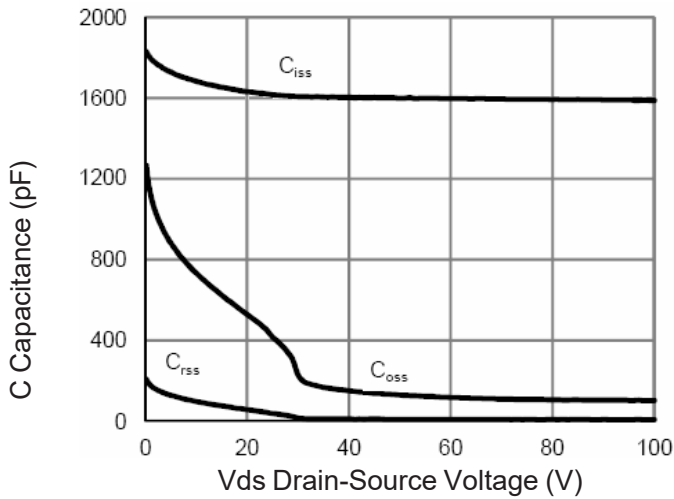
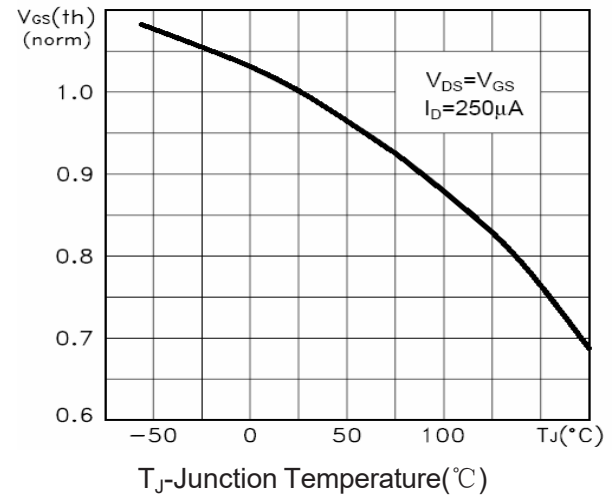
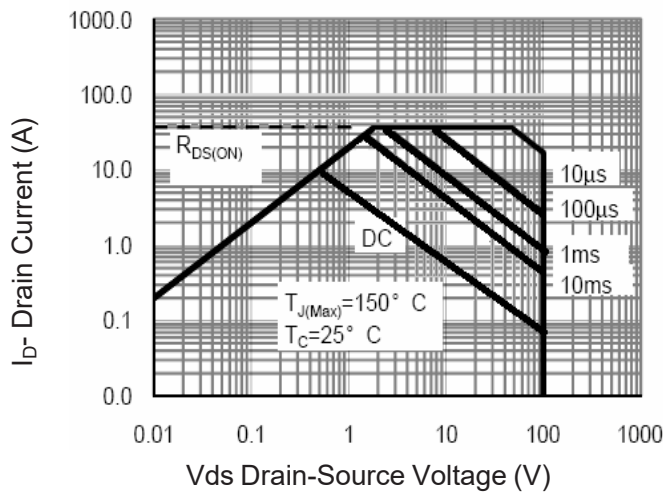
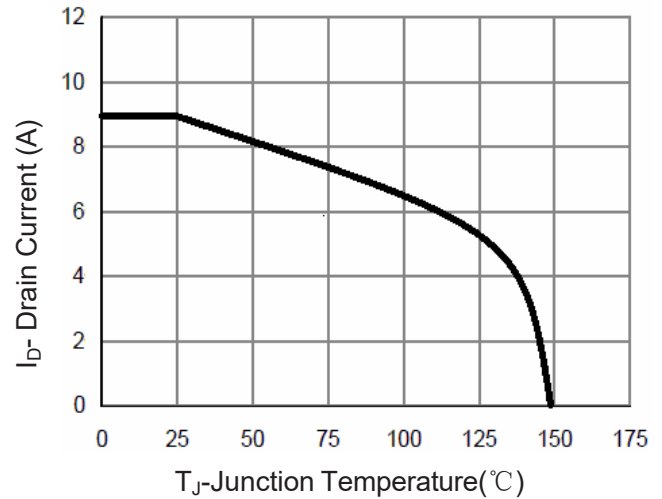
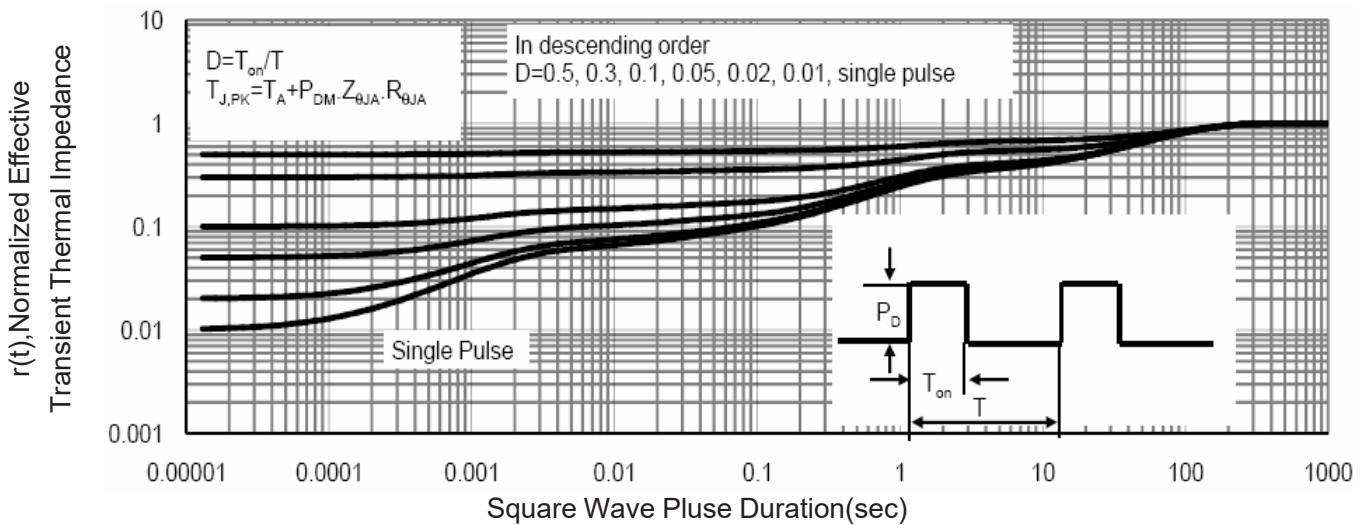


3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics


Figure 1 Output Characteristics

Figure 2 Transfer Characteristics

Figure 3 Rdson- Drain Current

Figure 4 Rdson-Junction Temperature

Figure 5 Gate Charge

Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 V_{GS}(th) vs Junction Temperature

Figure 8 Safe Operation Area

Figure 10 Current De-ratin

Figure 11 Normalized Maximum Transient Thermal Impedance