

Description

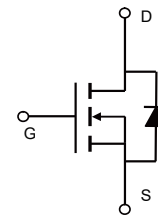
The VST06N020 uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

General Features

- $V_{DS} = 60V, I_D = 180A$
 $R_{DS(ON)} < 3.2m\Omega @ V_{GS}=10V$ (Typ:2.8m Ω)
- Excellent gate charge x $R_{DS(on)}$ product
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VST06N020	VST06N020-TC	TO-220	-	-	-

Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous (Silicon Limited)	I_D	180	A
Drain Current-Continuous($T_c=100^\circ\text{C}$)	$I_D(100^\circ\text{C})$	126	A
Pulsed Drain Current	I_{DM}	720	A
Maximum Power Dissipation	P_D	220	W
Derating factor		1.47	W/ $^\circ\text{C}$
Single pulse avalanche energy ^(Note 1)	E_{AS}	1036	mJ
Drain Source voltage slope, $V_{DS} \leq 48V$,	dv/dt	50	V/ns
Reverse diode dv/dt , $V_{DS} \leq 48V$, $I_{SD} < I_D$	dv/dt	15	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance,Junction-to-Case	$R_{\theta JC}$	0.68	$^{\circ}C/W$
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Electrical Characteristics ($T_c=25^{\circ}C$ unless otherwise noted)

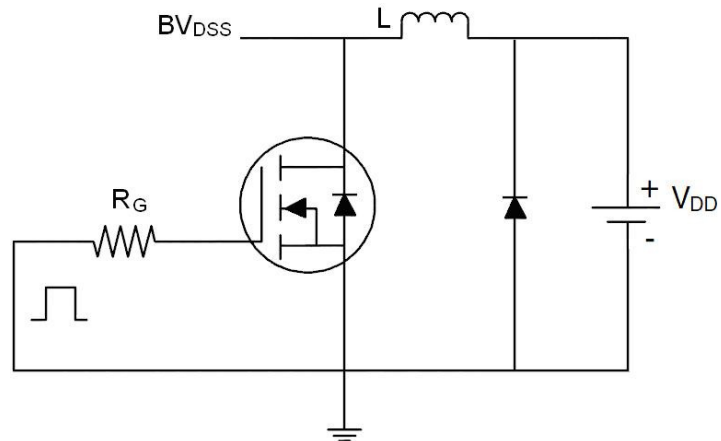
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	60		-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	3.0	4.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=40A$	-	2.8	3.2	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=40A$	50	-	-	S
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{DS}=30V, V_{GS}=0V,$ $F=1.0MHz$	-	4500	-	PF
Output Capacitance	C_{oss}		-	965	-	PF
Reverse Transfer Capacitance	C_{rss}		-	24.2	-	PF
Switching Characteristics (Note 2)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=40A$ $V_{GS}=10V, R_G=4.7\Omega$	-	6	-	nS
Turn-on Rise Time	t_r		-	11	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	23	-	nS
Turn-Off Fall Time	t_f		-	3	-	nS
Total Gate Charge	Q_g	$V_{DS}=30V, I_D=40A,$ $V_{GS}=10V$	-	70	-	nC
Gate-Source Charge	Q_{gs}		-	18.6	-	nC
Gate-Drain Charge	Q_{gd}		-	15.3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=40A$	-		1.2	V
Diode Forward Current	I_S		-	-	180	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}C, I_F = I_S$ $di/dt = 100A/\mu s$	-	50		nS
Reverse Recovery Charge	Q_{rr}		-	66		nC

Notes:

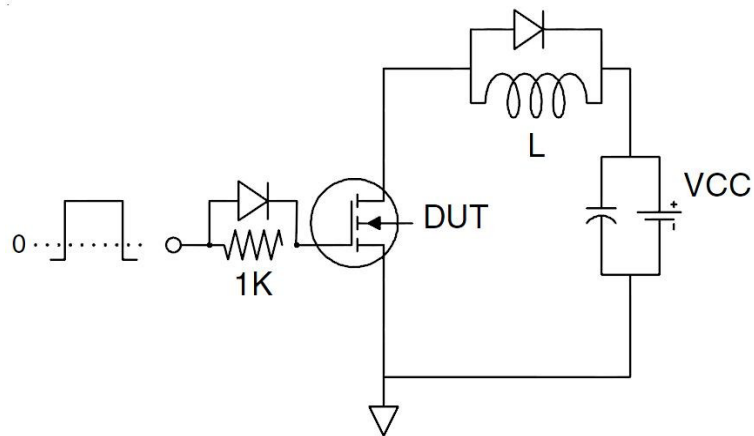
1. EAS condition : $T_J=25^{\circ}C, V_{DD}=30V, V_G=10V, L=0.5mH, R_G=25\Omega$
2. Guaranteed by design, not subject to production.
3. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_J(MAX)=175^{\circ}C$. The SOA curve provides a single pulse rating.

Test Circuit

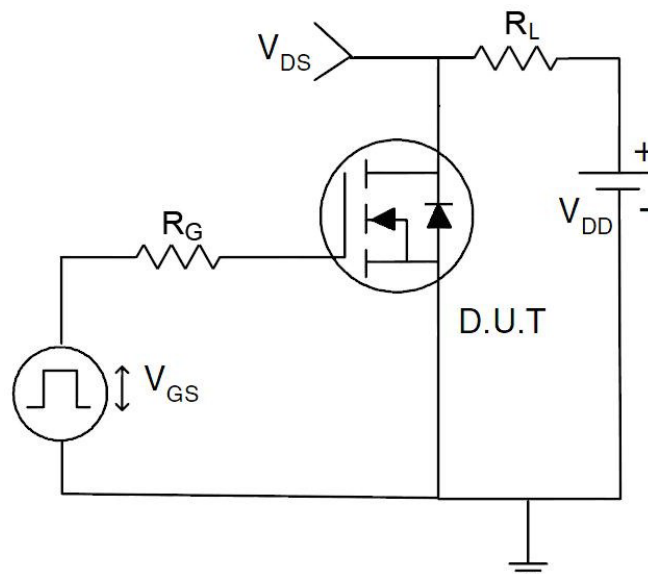
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

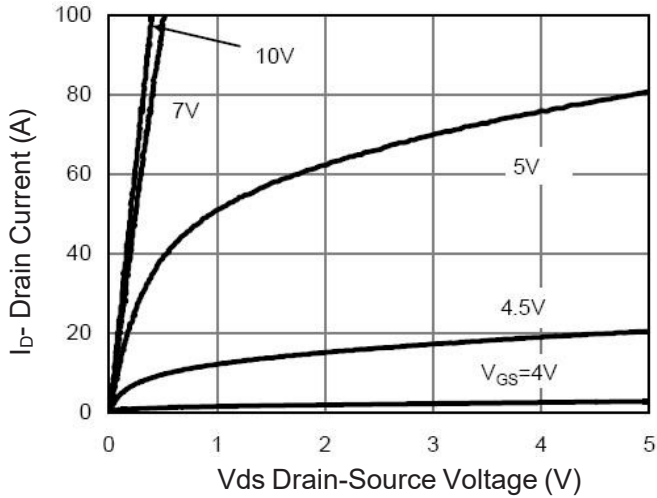


Figure 1 Output Characteristics

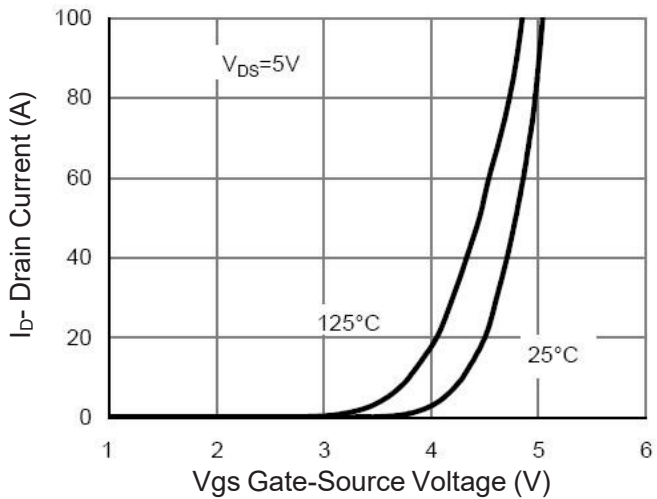


Figure 2 Transfer Characteristics

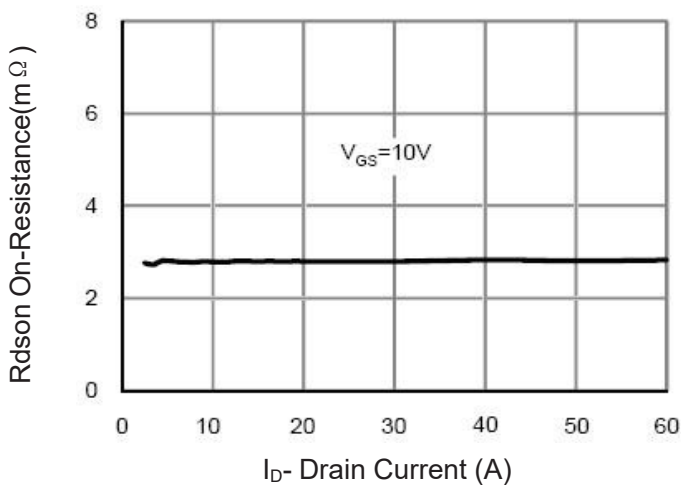


Figure 3 Rdson- Drain Current

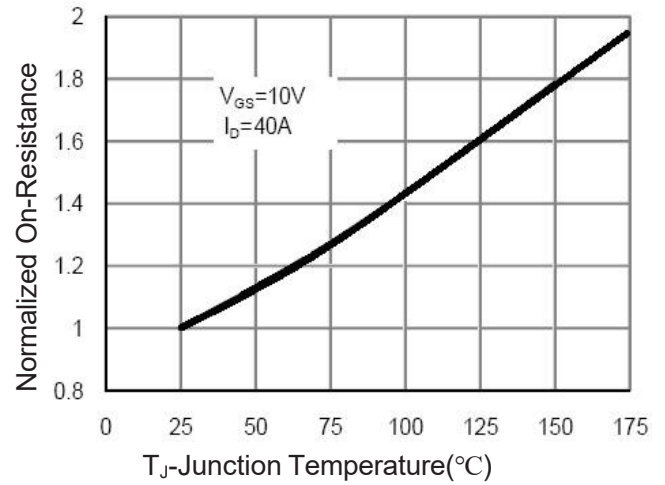


Figure 4 Rdson-Junction Temperature

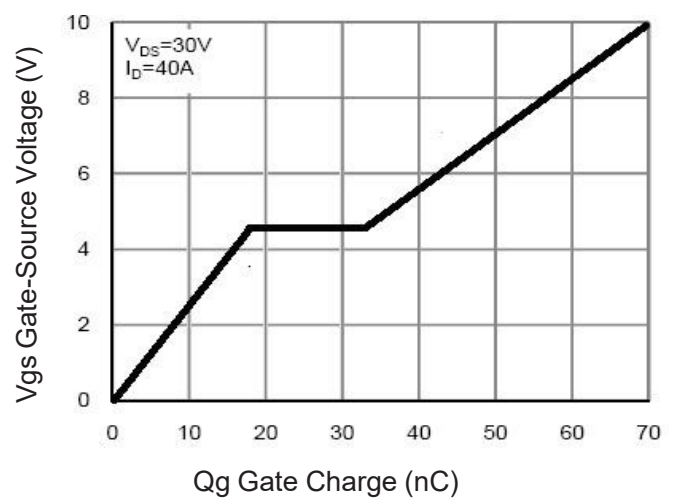


Figure 5 Gate Charge

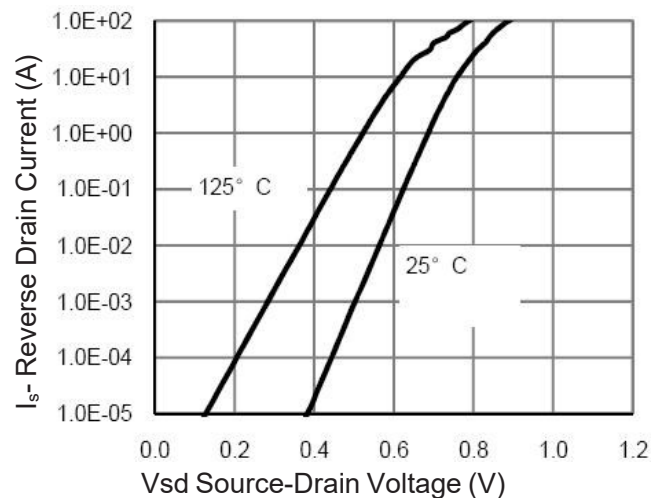
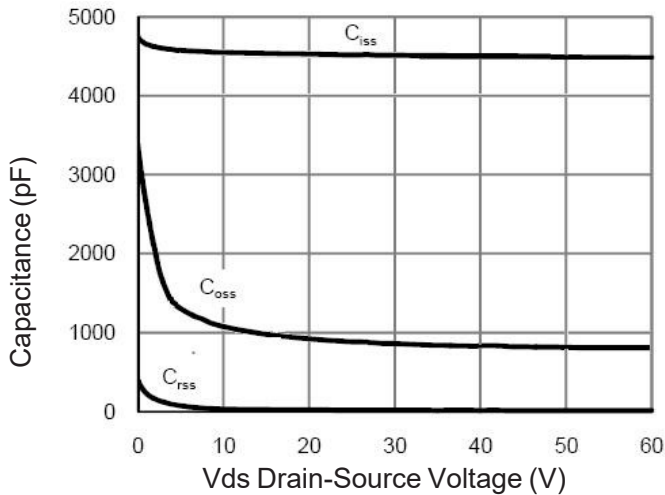
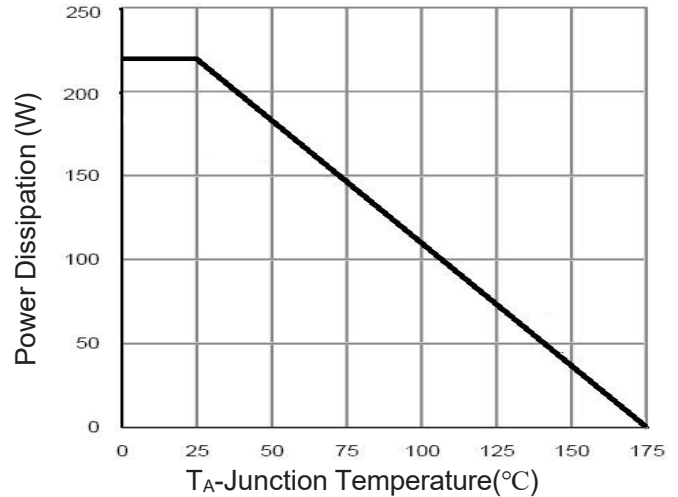
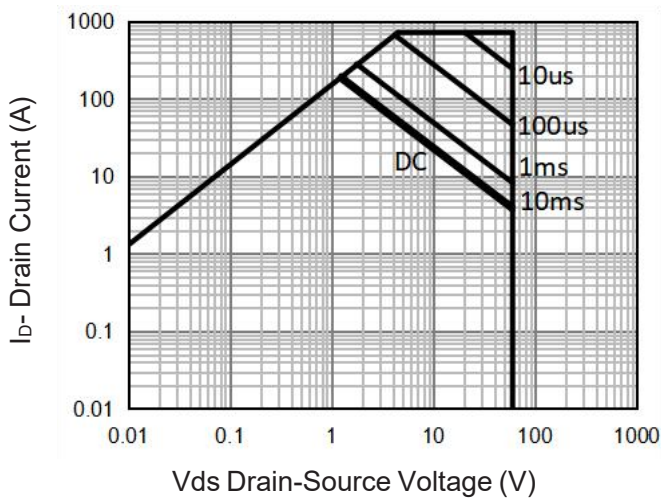
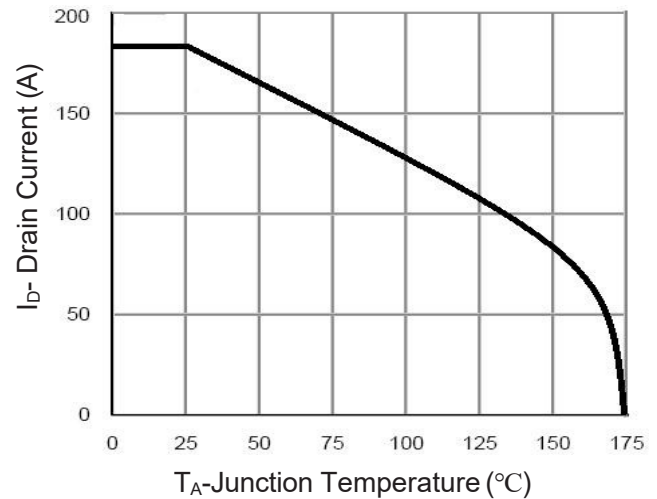
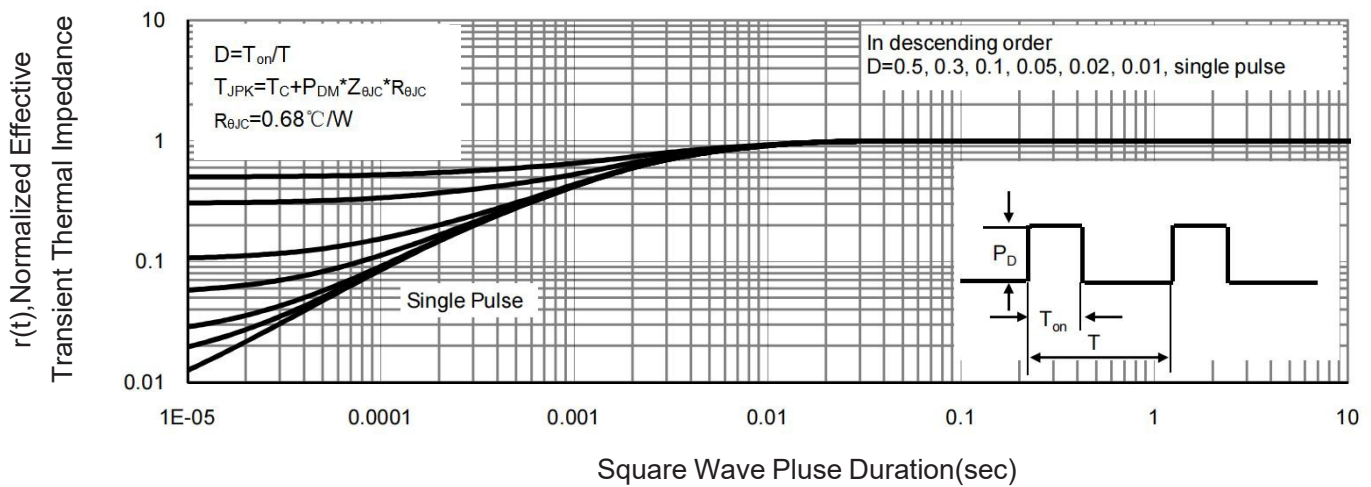


Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 Power De-rating

Figure 8 Safe Operation Area (Note 3)

Figure 10 Current De-rating

Figure 11 Normalized Maximum Transient Thermal Impedance