

Description

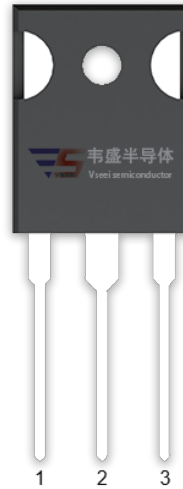
The VST25N140 uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(on)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

General Features

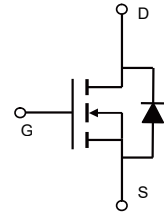
- $V_{DS} = 250V, I_D = 90A$
 $R_{DS(on)} < 16m\Omega @ V_{GS} = 10V$
- Excellent gate charge x $R_{DS(on)}$ product
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating
- Optimized body diode reverse recovery performance

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification



TO-247



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VST25N140	VST25N140-T7	TO-247	-	-	-

Absolute Maximum Ratings ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	250	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	90	A
Drain Current-Continuous($T_c = 100^\circ\text{C}$)	$I_D(100^\circ\text{C})$	63.6	A
Pulsed Drain Current	I_{DM}	360	A
Maximum Power Dissipation	P_D	330	W
Derating factor		2.2	W/ $^\circ\text{C}$
Single pulse avalanche energy ^(Note 1)	E_{AS}	1700	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.45	$^\circ\text{C/W}$
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Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise noted)

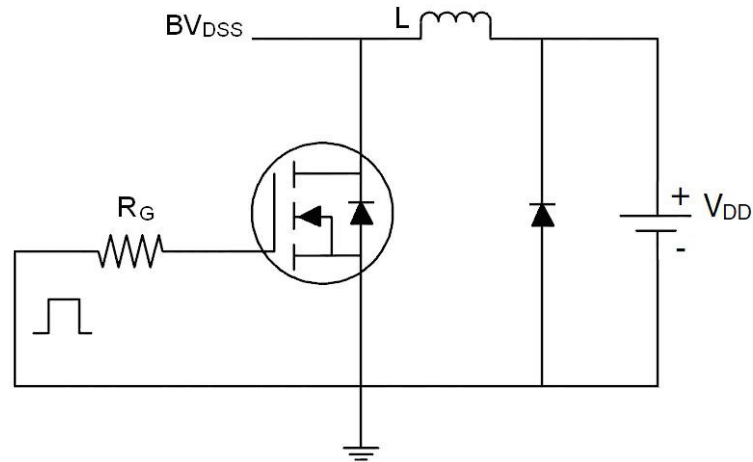
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	250		-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =250V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2.5		4.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =45A	-	14	16	mΩ
Gate resistance	R _G		-	3.3	-	Ω
Forward Transconductance	g _{FS}	V _{DS} =10V, I _D =45A	70	-	-	S
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} =125V, V _{GS} =0V, F=1.0MHz	-	6595	-	PF
Output Capacitance	C _{oss}		-	409.5	-	PF
Reverse Transfer Capacitance	C _{rss}		-	11	-	PF
Switching Characteristics (Note 2)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =125V, I _D =45A V _{GS} =10V, R _G =4.7Ω	-	19.5	-	nS
Turn-on Rise Time	t _r		-	28	-	nS
Turn-Off Delay Time	t _{d(off)}		-	48	-	nS
Turn-Off Fall Time	t _f		-	15	-	nS
Total Gate Charge	Q _g	V _{DS} =125V, I _D =45A, V _{GS} =10V	-	90.9		nC
Gate-Source Charge	Q _{gs}		-	40.4		nC
Gate-Drain Charge	Q _{gd}		-	18		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =90A	-		1.2	V
Diode Forward Current (Note 2)	I _S		-	-	90	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 45A	-	186		nS
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs ^(Note3)	-	1.35		uC

Notes:

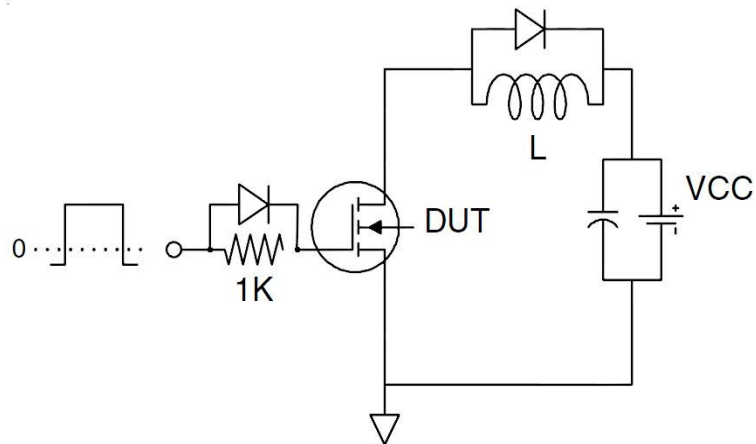
1. EAS condition : $T_J=25^\circ C, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$
2. Guaranteed by design, not subject to production
3. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=175^\circ C$. The SOA curve provides a single pulse rating.

Test Circuit

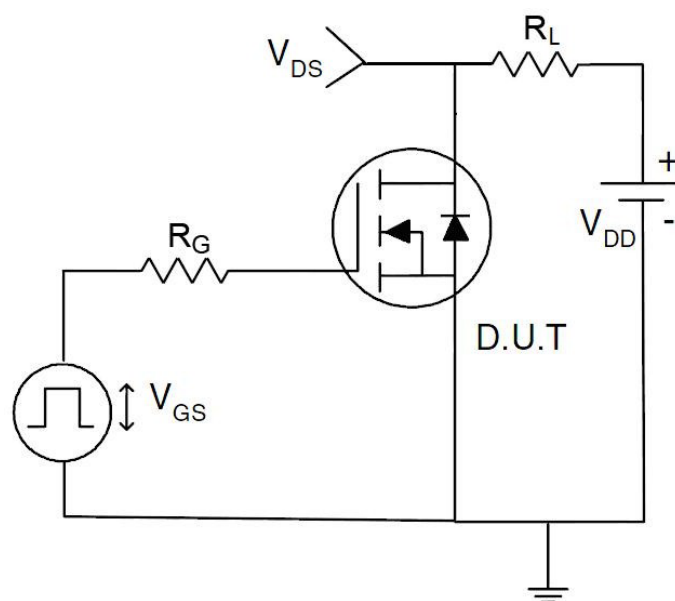
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

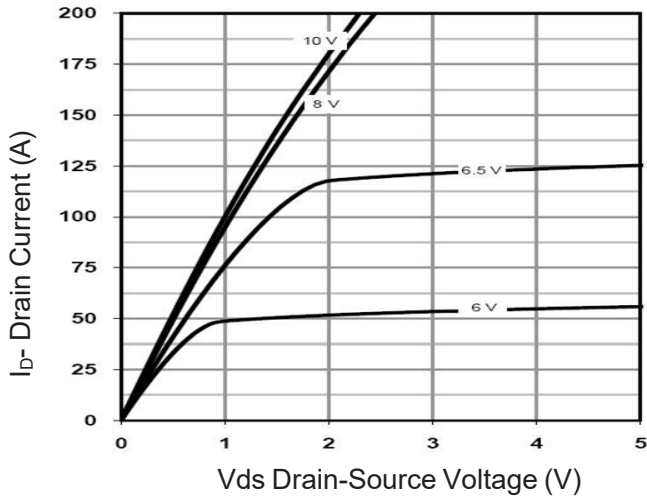


Figure 1 Output Characteristics

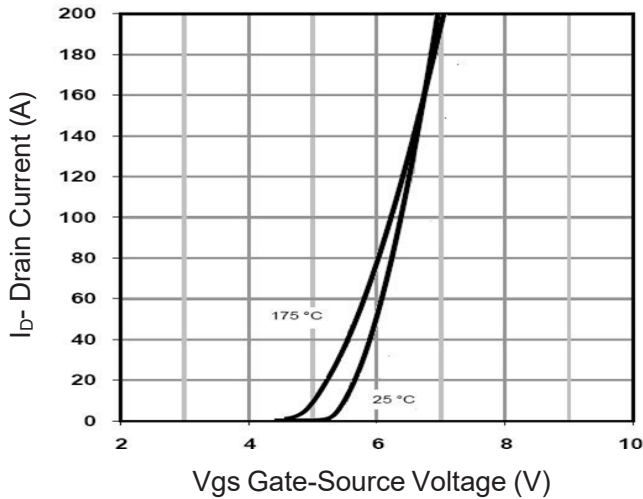


Figure 2 Transfer Characteristics

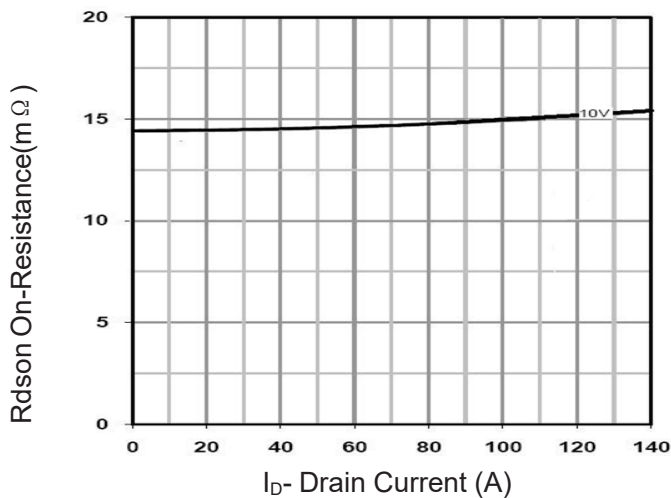


Figure 3 Rdson- Drain Current

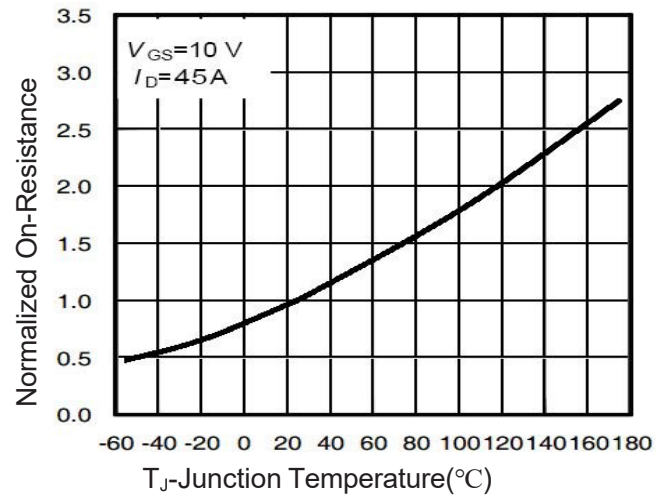


Figure 4 Rdson-Junction Temperature

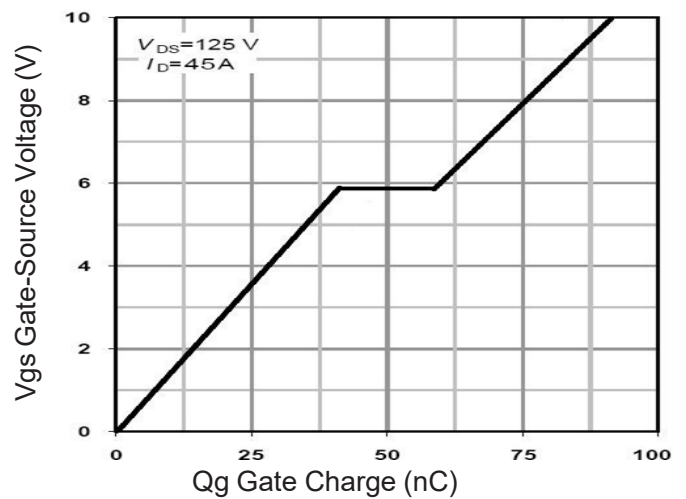


Figure 5 Gate Charge

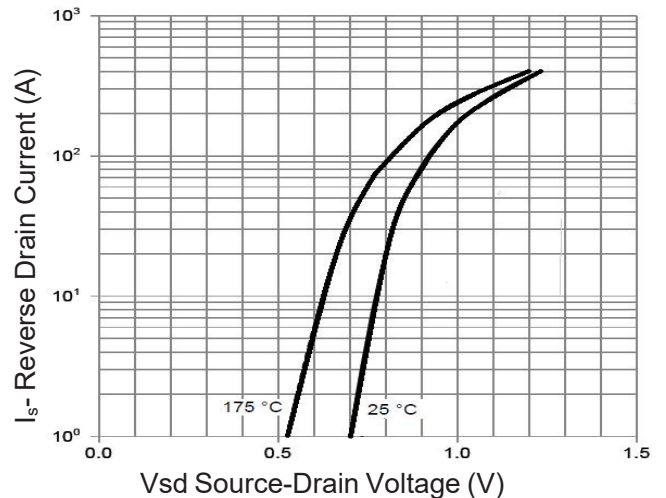
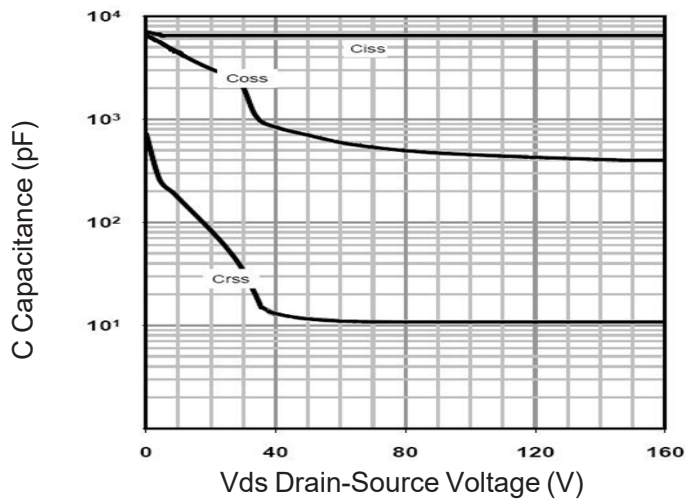
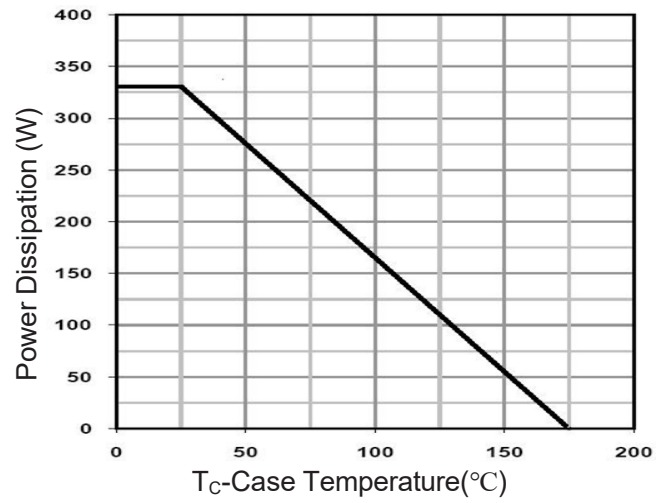
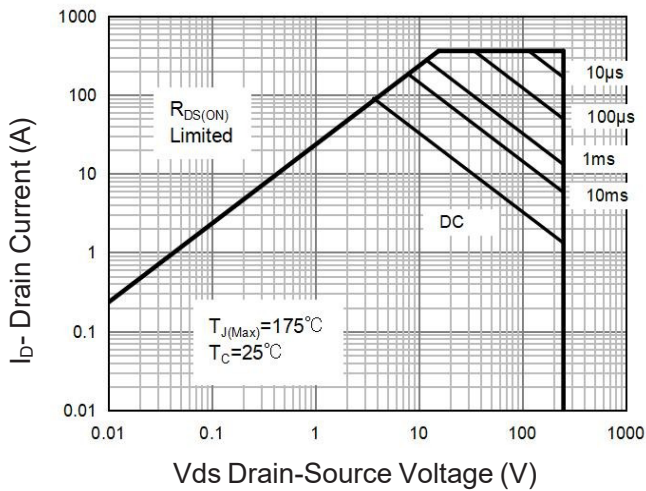
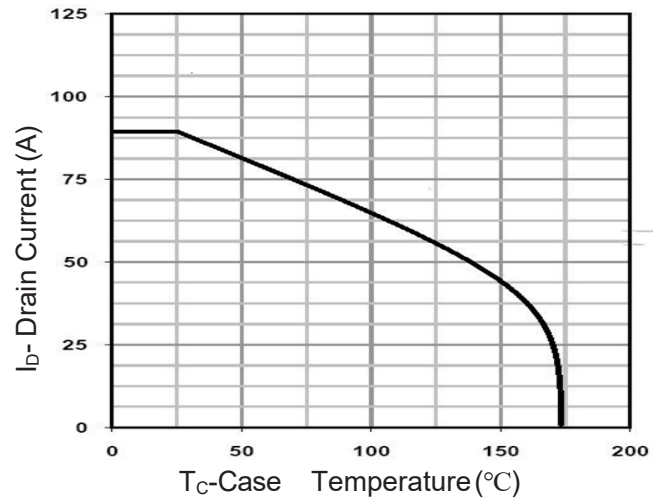
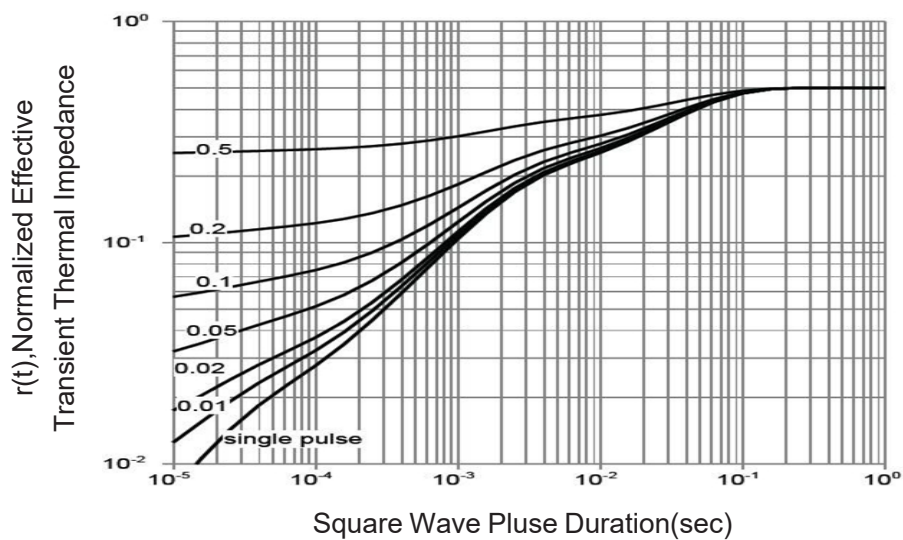


Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 Power De-rating

Figure 8 Safe Operation Area (Note3)

Figure 10 Current De-rating

Figure 11 Normalized Maximum Transient Thermal Impedance