

Description

The VST20N1450 uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(on)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

General Features

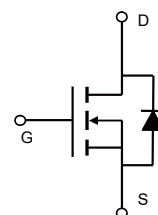
- $V_{DS} = 200V, I_D = 18A$
 $R_{DS(on)} = 145m\Omega$ (typical) @ $V_{GS} = 10V$
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating

Application

- LED backlighting
- Ideal for high-frequency switching and synchronous rectification



TO-252



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VST20N1450	VST20N1450-T2	TO-252	-	-	-

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	200	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	18	A
Drain Current-Continuous ($T_C = 100^\circ\text{C}$)	$I_D (100^\circ\text{C})$	12.7	A
Pulsed Drain Current	I_{DM}	72	A
Maximum Power Dissipation	P_D	140	W
Derating factor		0.93	W/ $^\circ\text{C}$
Single pulse avalanche energy ^(Note 1)	E_{AS}	80	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.07	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient ^(Note 4)	$R_{\theta JA}$	50	$^\circ\text{C/W}$

Electrical Characteristics (T_A=25°C unless otherwise noted)

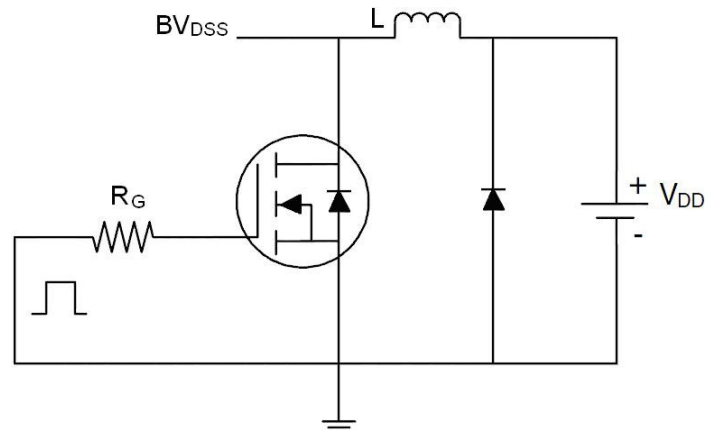
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	200	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =200V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2.5	3.5	4.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =18A	-	145	168	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =18A	-	15	-	S
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} =100V, V _{GS} =0V, F=1.0MHz	-	483		PF
Output Capacitance	C _{oss}		-	42		PF
Reverse Transfer Capacitance	C _{rss}		-	1		PF
Switching Characteristics (Note 2)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =100V, R _L =8Ω V _{GS} =10V, R _G =3Ω	-	4	-	nS
Turn-on Rise Time	t _r		-	5	-	nS
Turn-Off Delay Time	t _{d(off)}		-	10	-	nS
Turn-Off Fall Time	t _f		-	2	-	nS
Total Gate Charge	Q _g	V _{DS} =100V, I _D =18A, V _{GS} =10V	-	9.2	-	nC
Gate-Source Charge	Q _{gs}		-	3.8	-	nC
Gate-Drain Charge	Q _{gd}		-	2.3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _S =18A	-	-	1.2	V
Diode Forward Current	I _S		-	-	18	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F =18A	-	25	-	nS
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs	-	110	-	nC

Notes:

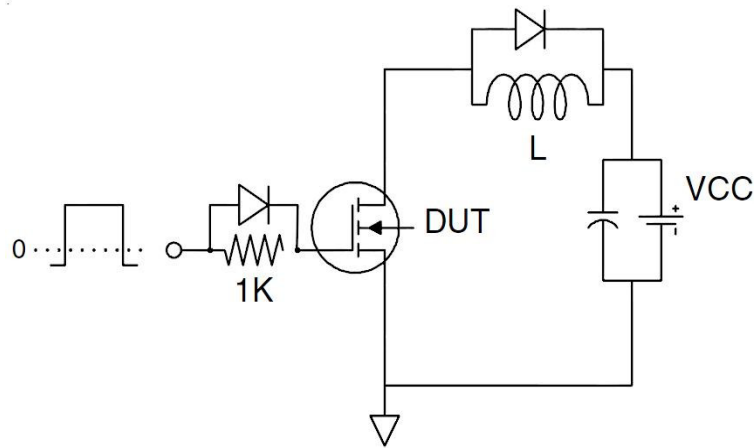
1. EAS condition : T_J=25°C, V_{DD}=50V, V_G=10V, L=0.5mH, R_G=25Ω
2. Guaranteed by design, not subject to production
3. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heat sink, assuming a maximum junction temperature of T_J(MAX)=175° C. The SOA curve provides a single pulse rating.
4. The value of R_{θJA} is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The maximum allowed junction temperature of 175°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

Test Circuit

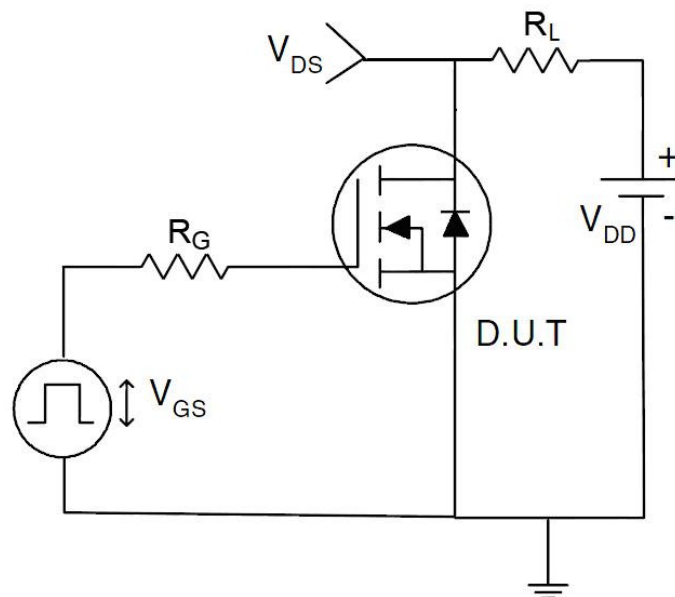
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

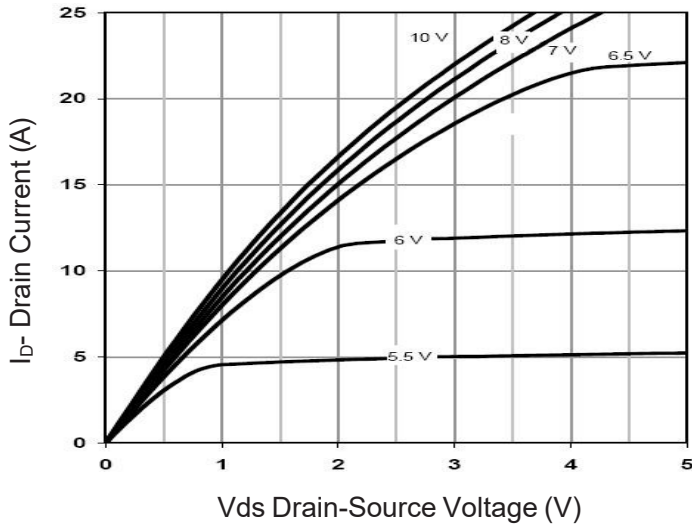


Figure 1 Output Characteristics

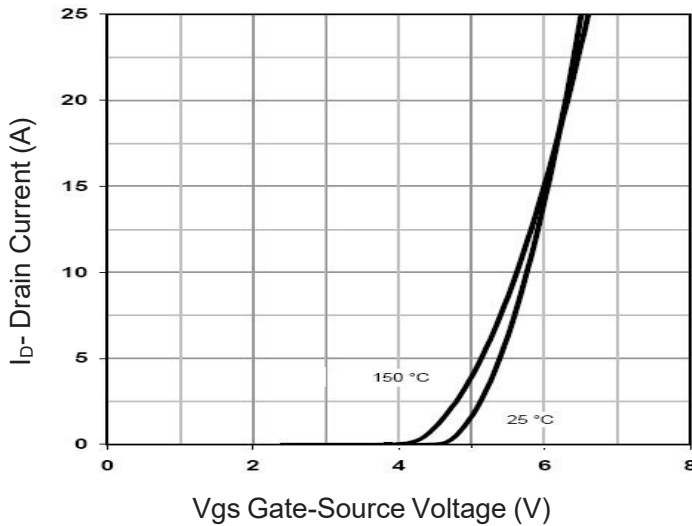


Figure 2 Transfer Characteristics

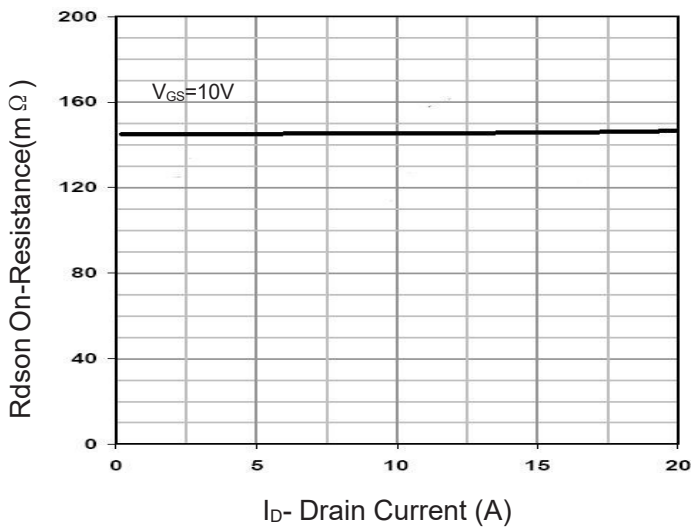


Figure 3 Rdson- Drain Current

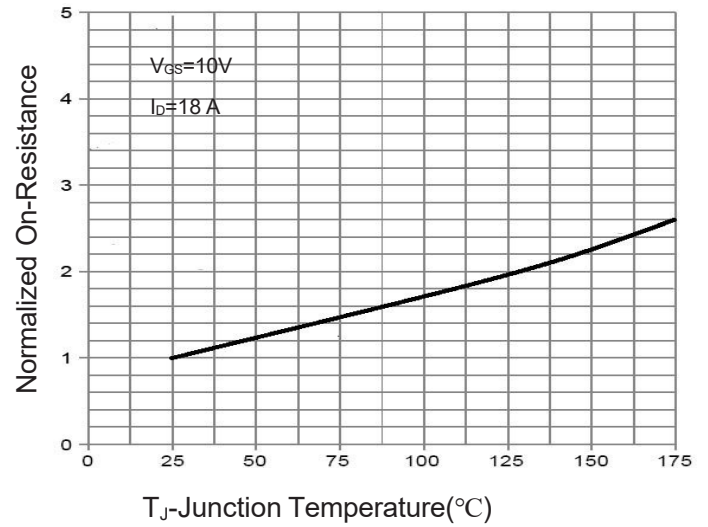


Figure 4 Rdson-Junction Temperature

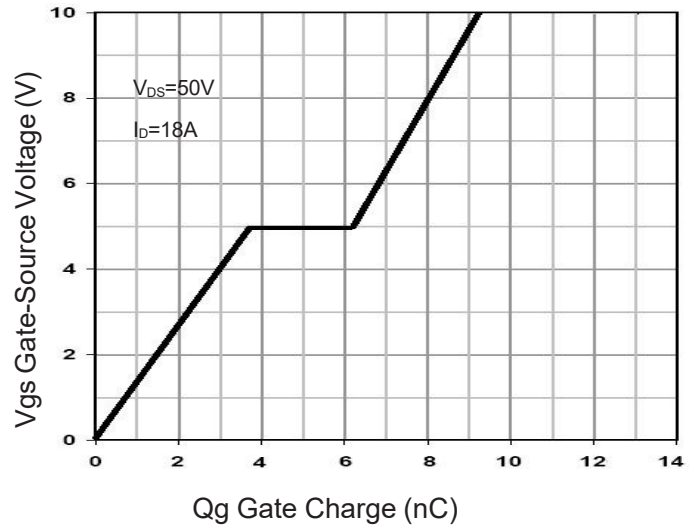


Figure 5 Gate Charge

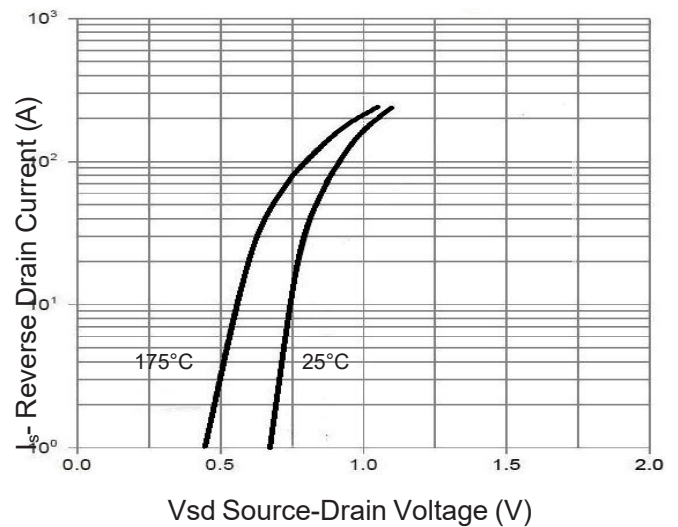
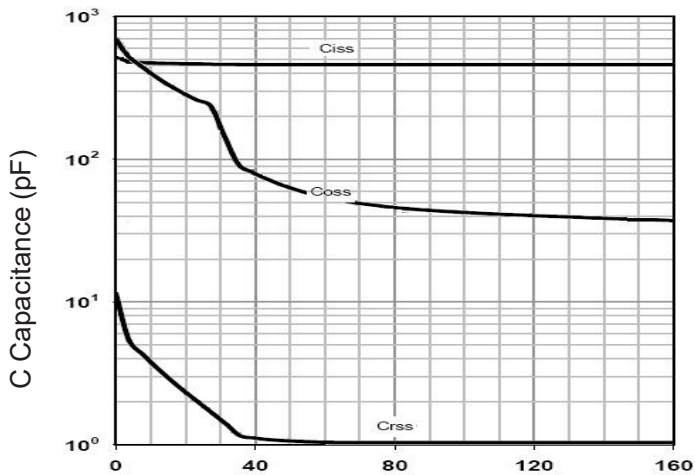
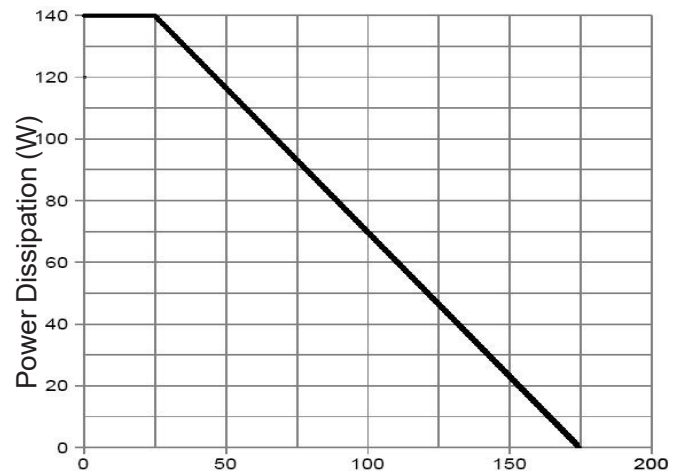


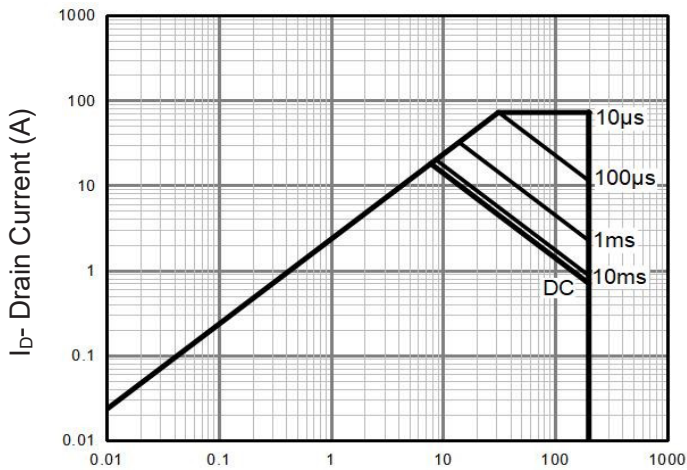
Figure 6 Source- Drain Diode Forward



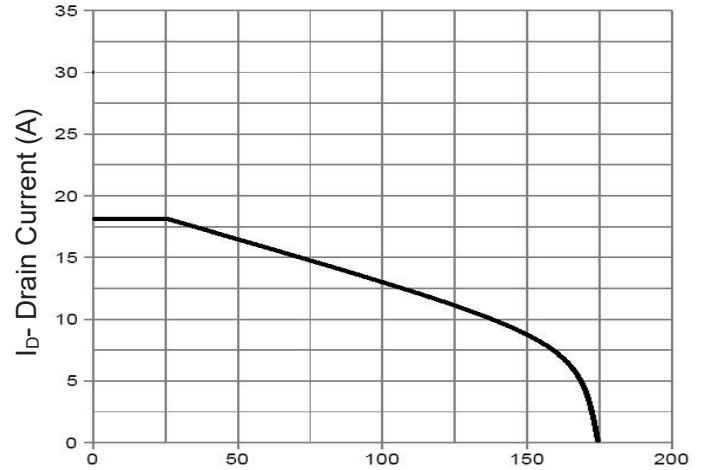
Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



T_C- Case Temperature(°C)
Figure 9 Power De-rating



Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area (Note3)



T_C-Case Temperature(°C)
Figure 10 Current De-rating

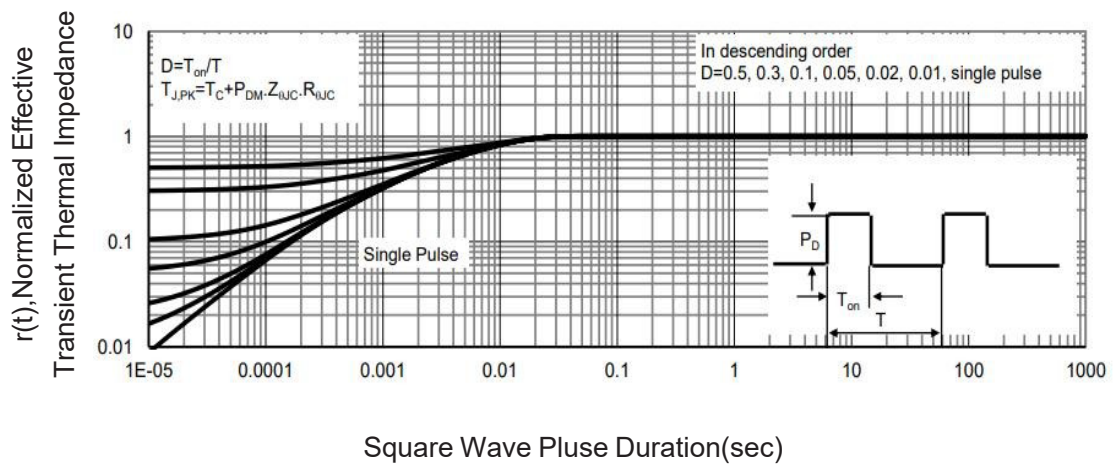


Figure 11 Normalized Maximum Transient Thermal Impedance