

Description

The VST15N050 uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

General Features

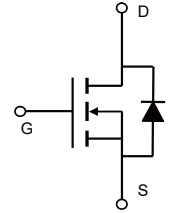
- $V_{DS} = 150V, I_D = 140A$
 $R_{DS(ON)} = 5.6m\Omega$, typical @ $V_{GS} = 10V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification



TO-263



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VST15N050	VST15N050-T3	TO-263	-	-	-

Absolute Maximum Ratings ($T_c = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	150	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	140	A
Drain Current-Continuous($T_c = 100^\circ C$)	$I_D(100^\circ C)$	100	A
Pulsed Drain Current	I_{DM}	560	A
Maximum Power Dissipation	P_D	320	W
Derating factor		2.1	W/ $^\circ C$
Single pulse avalanche energy ^(Note 1)	E_{AS}	1296	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.47	$^\circ C/W$
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Electrical Characteristics (T_c=25°C unless otherwise noted)

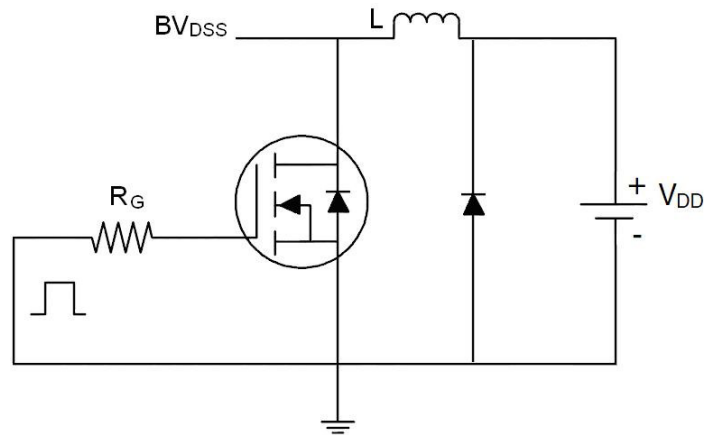
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	150	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =150V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2.0	3.0	4.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =70A	-	5.6	6.4	mΩ
Gate resistance	R _G		-	4.5	-	Ω
Forward Transconductance	g _{FS}	V _{DS} =10V, I _D =70A	70	-	-	S
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} =75V, V _{GS} =0V, F=1.0MHz	-	6000	-	PF
Output Capacitance	C _{oss}		-	690	-	PF
Reverse Transfer Capacitance	C _{rss}		-	24	-	PF
Switching Characteristics (Note 2)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =75V, I _D =70A V _{GS} =10V, R _G =4.7Ω	-	26	-	nS
Turn-on Rise Time	t _r		-	36	-	nS
Turn-Off Delay Time	t _{d(off)}		-	47	-	nS
Turn-Off Fall Time	t _f		-	15	-	nS
Total Gate Charge	Q _g	V _{DS} =75V, I _D =70A, V _{GS} =10V	-	80	-	nC
Gate-Source Charge	Q _{gs}		-	32	-	nC
Gate-Drain Charge	Q _{gd}		-	22	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _F = I _S	-		1.2	V
Diode Forward Current	I _S		-	-	140	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = I _S	-	146	-	nS
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs	-	485	-	nC

Notes:

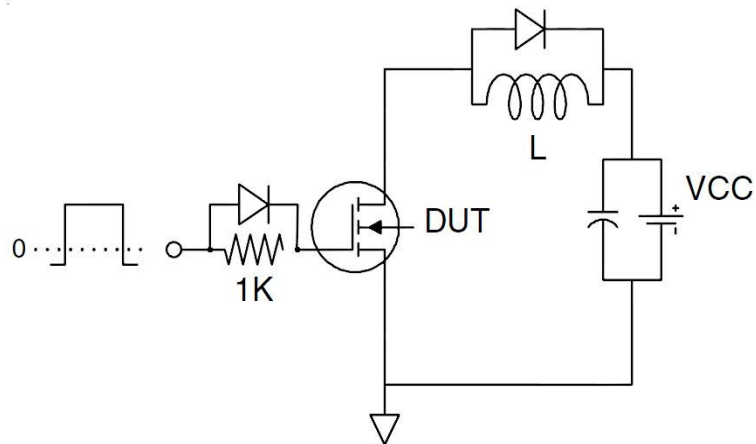
1. EAS condition : T_j=25°C, V_{DD}=50V, V_G=10V, L=0.5mH, R_G=25Ω
2. Guaranteed by design, not subject to production
3. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_J(MAX)=175° C. The SOA curve provides a single pulse rating.

Test Circuit

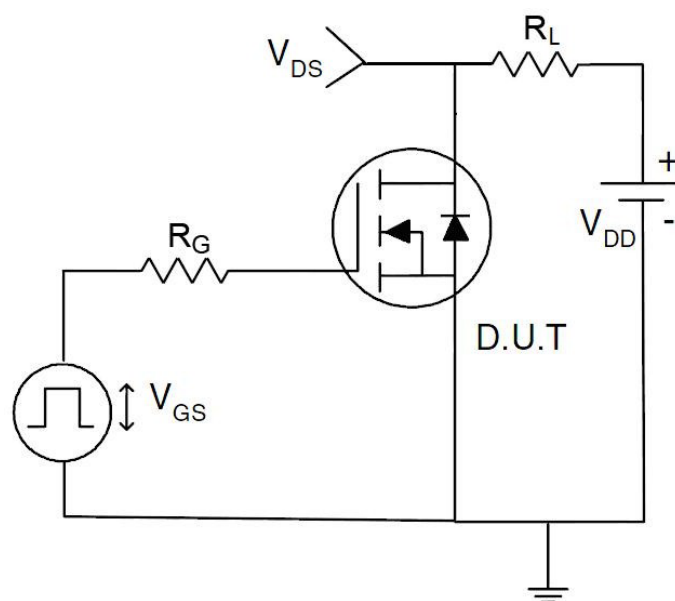
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

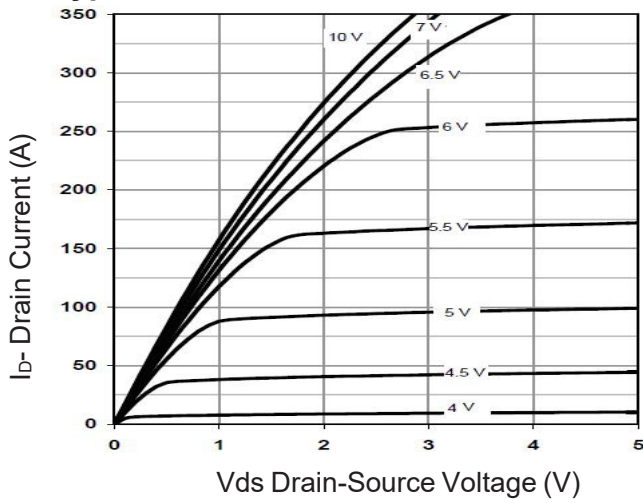


Figure 1 Output Characteristics

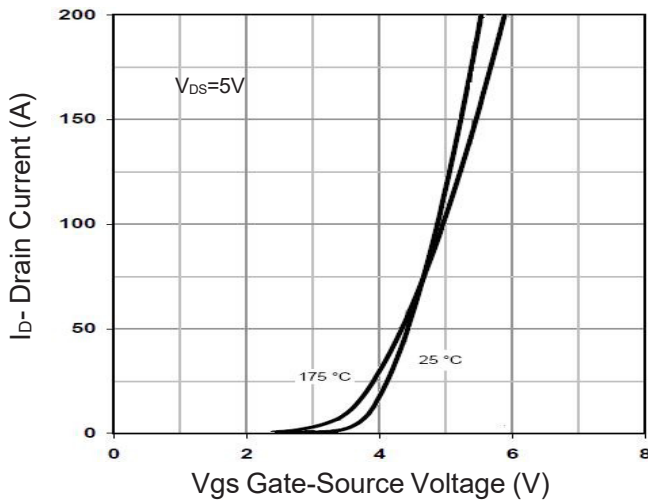


Figure 2 Transfer Characteristics

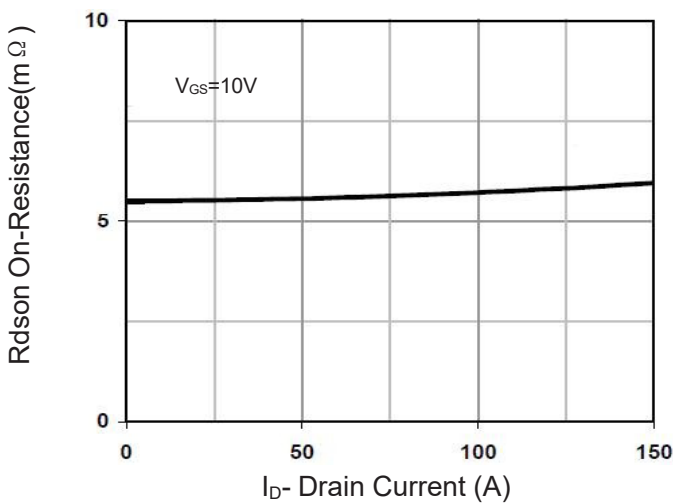


Figure 3 Rdson- Drain Current

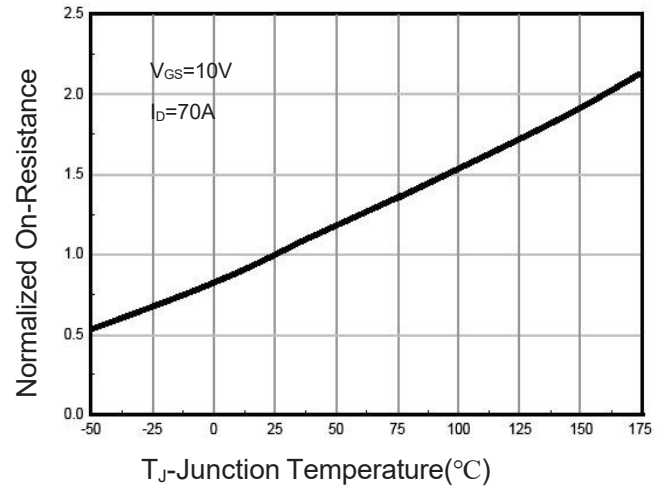


Figure 4 Rdson-Junction Temperature

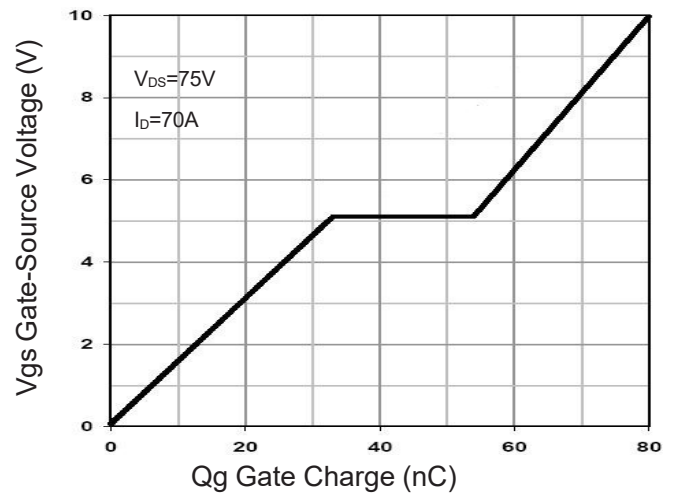


Figure 5 Gate Charge

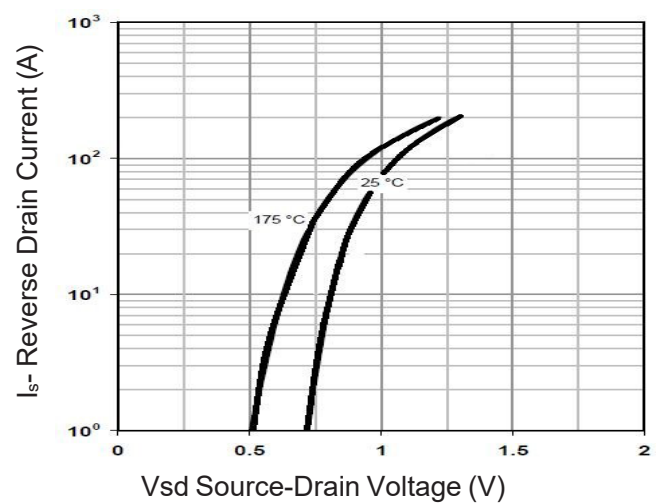
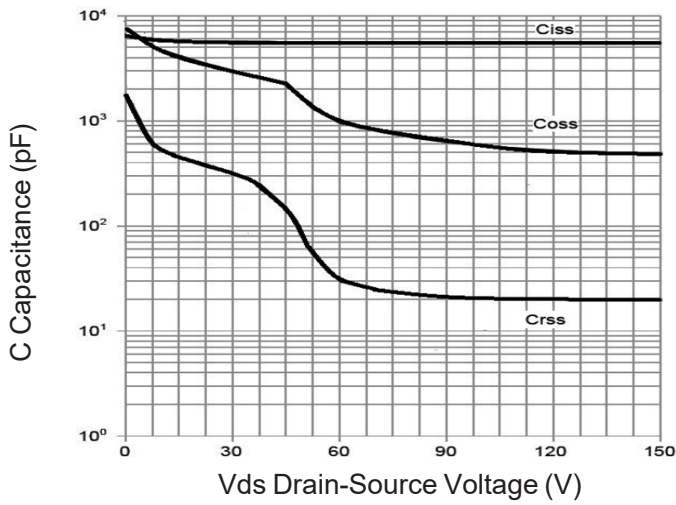
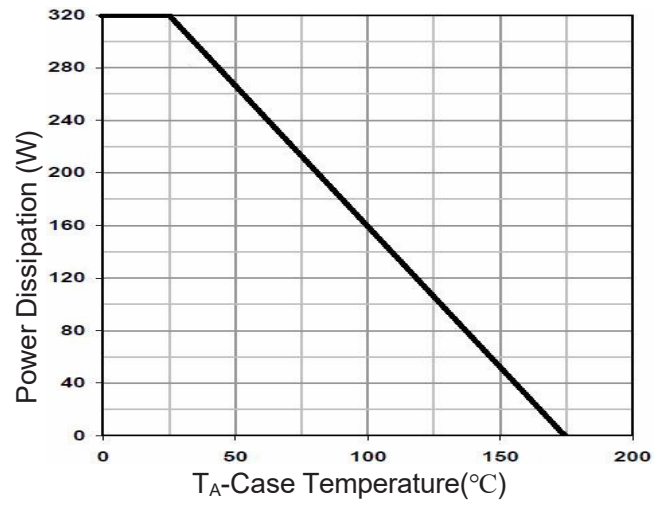
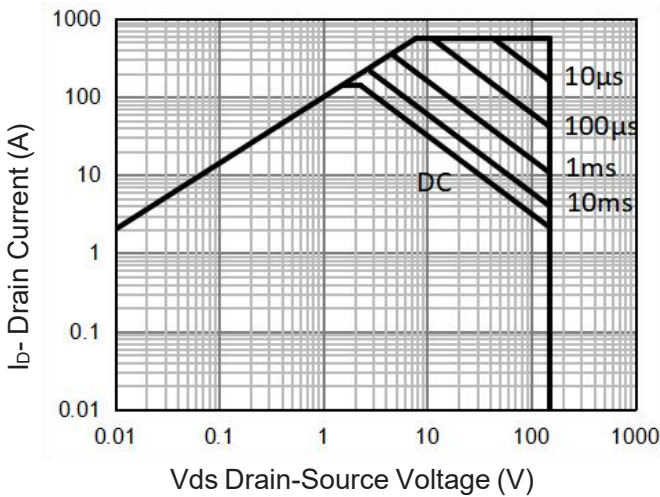
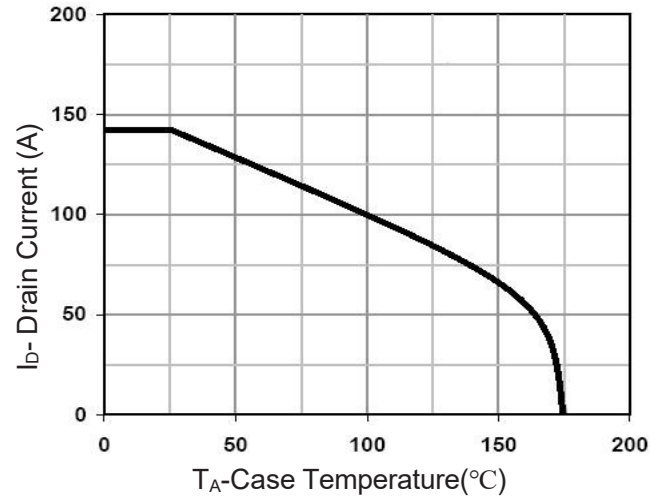
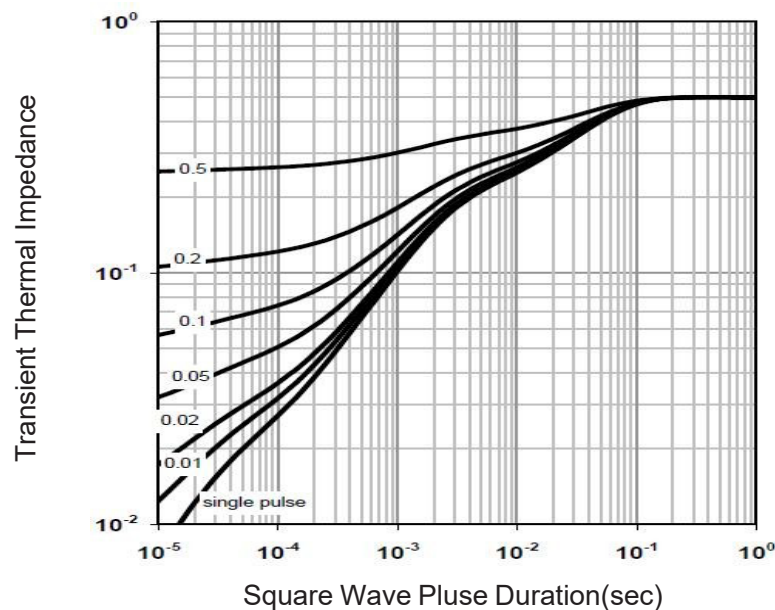


Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 Power De-rating

Figure 8 Safe Operation Area (Note3)

Figure 10 Current De-rating

Figure 11 Normalized Maximum Transient Thermal Impedance