Description

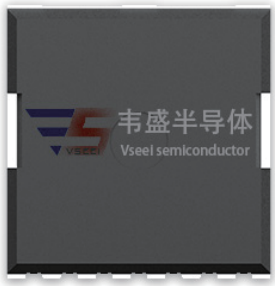
The series of devices uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g. This device is ideal for high-frequency switching and synchronous rectification.

Application

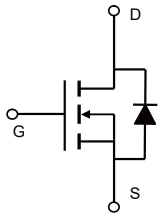
- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

General Features

- V_{DS} =150V,I_D =255A
  $R_{DS(ON)}$=4.2mΩ , typical@ V_{GS}=10V
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating



TOLL



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VST15N040	VST15N040-OL	TOLL	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	150	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous (T_C=25℃)	I_D (T_C=25℃)	255	A
Drain Current-Continuous(T_C=100℃)	I_D (T_C =100℃)	180	A
Pulsed Drain Current	I_{DM}	1020	A
Maximum Power Dissipation (T_C=25℃)	P_D (T_C=25℃)	690	W
Derating factor		4.6	W/℃
Single pulse avalanche energy (Note 1)	E_{AS}	1797	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case	$R_{\theta JC}$	0.22	℃/W
Thermal Resistance,Junction-to-Ambient(Note 4)	$R_{\theta JA}$	40	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

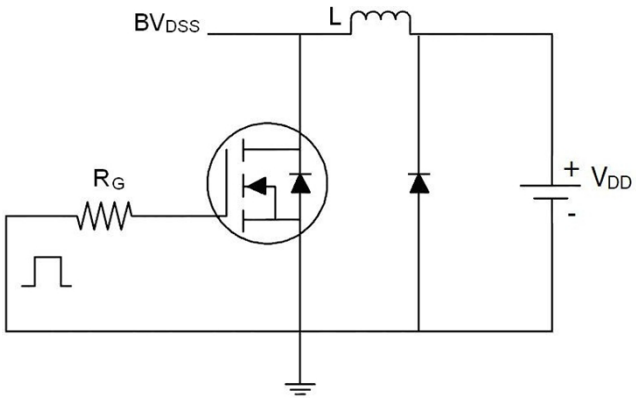
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	150		-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=150V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2.0	3.0	4.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	-	4.2	4.7	mΩ
Forward Transconductance	g_{FS}	V_{DS}=10V,I_D=20A	70	-	-	S
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=75V,V_{GS}=0V, F=1.0MHz	-	7100	-	pF
Output Capacitance	C_{oss}		-	890	-	pF
Reverse Transfer Capacitance	C_{rss}		-	30	-	pF
Switching Characteristics (Note 2)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=75V,I_D=20A V_{GS}=10V,R_G=4.7Ω	-	36	-	nS
Turn-on Rise Time	t_r		-	40	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	60	-	nS
Turn-Off Fall Time	t_f		-	30	-	nS
Total Gate Charge	Q_g	V_{DS}=75V,I_D=20A, V_{GS}=10V	-	97	-	nC
Gate-Source Charge	Q_{gs}		-	32.5	-	nC
Gate-Drain Charge	Q_{gd}		-	22.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_F=20A	-		1.2	V
Diode Forward Current	I_S		-	-	255	A
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F = I_S di/dt = 100A/μs	-	160		nS
Reverse Recovery Charge	Qrr		-	720		nC

Notes:

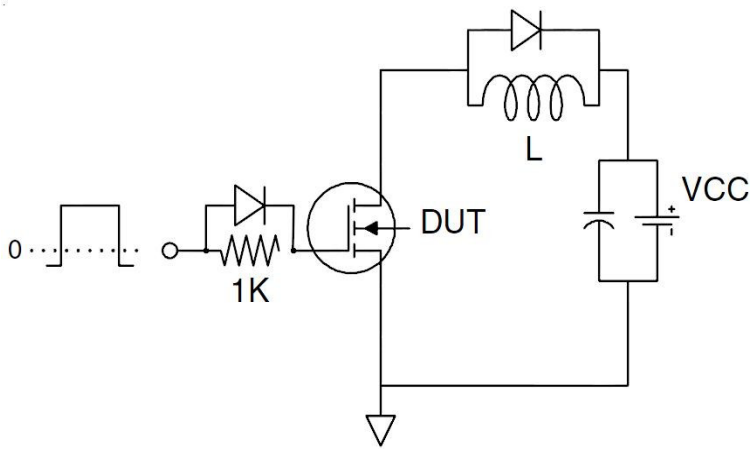
1. EAS condition : Tj=25℃,V_{DD}=50V,V_G=10V,L=0.5mH,Rg=25Ω
2. Guaranteed by design, not subject to production
3. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C. The SOA curve provides a single pulse rating.
4. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.

Test Circuit

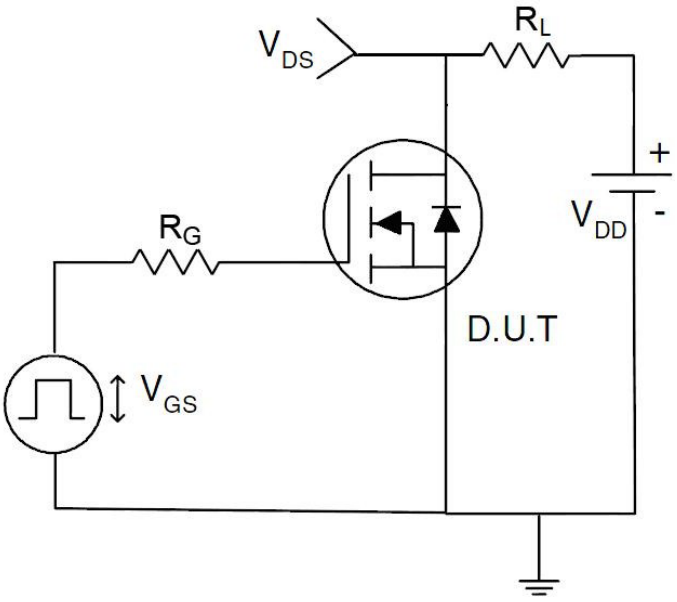
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

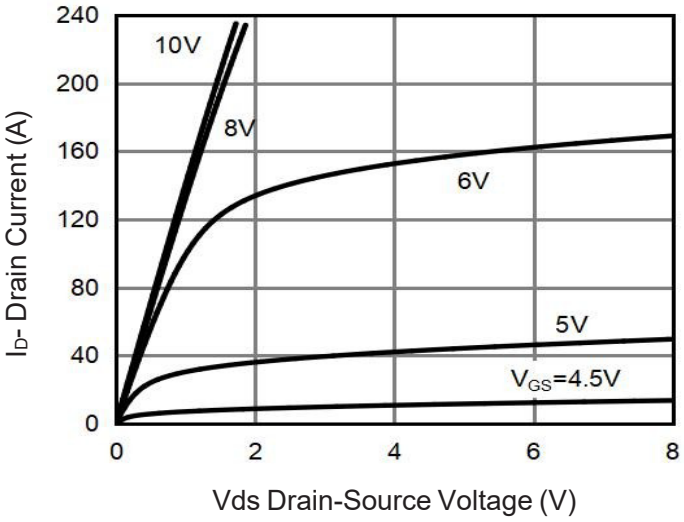


Figure 1 Output Characteristics

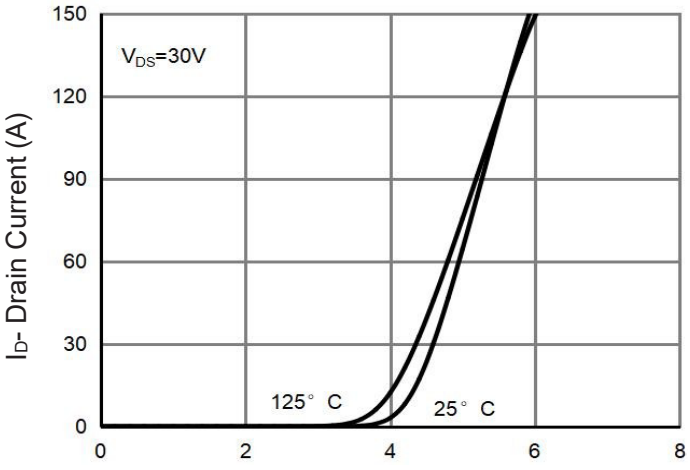


Figure 2 Transfer Characteristics

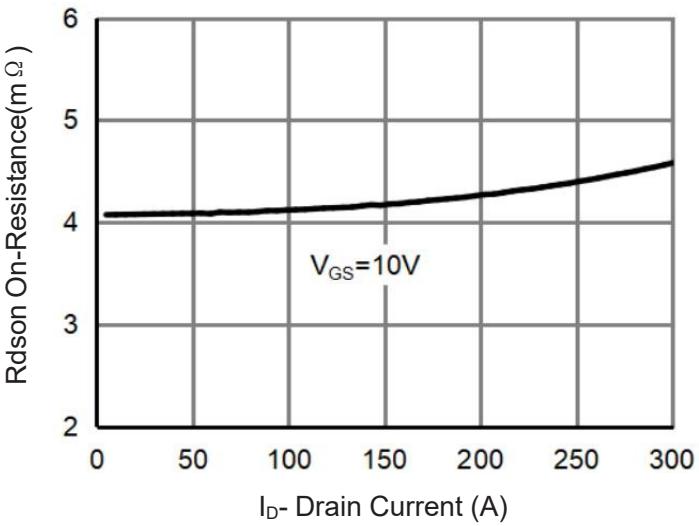


Figure 3 Rdson- Drain Current

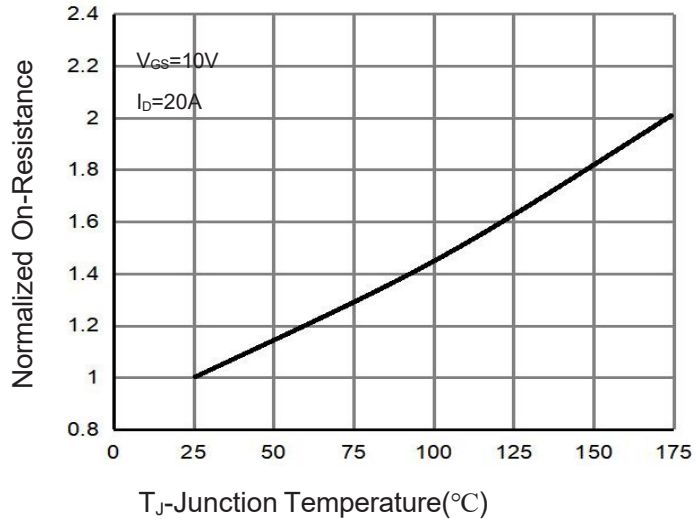


Figure 4 Rdson-JunctionTemperature

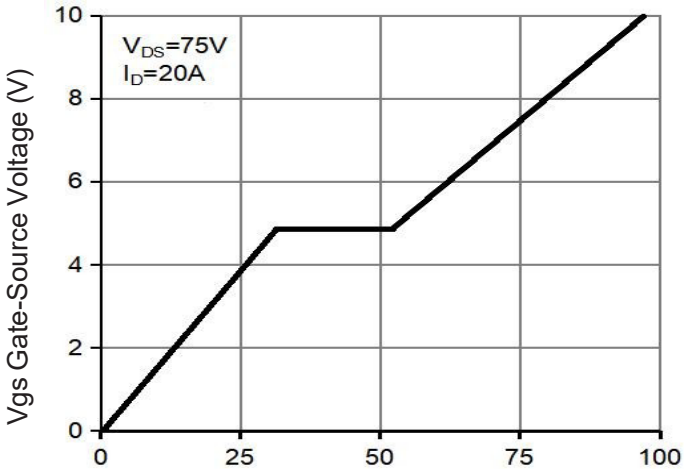


Figure 5 Gate Charge

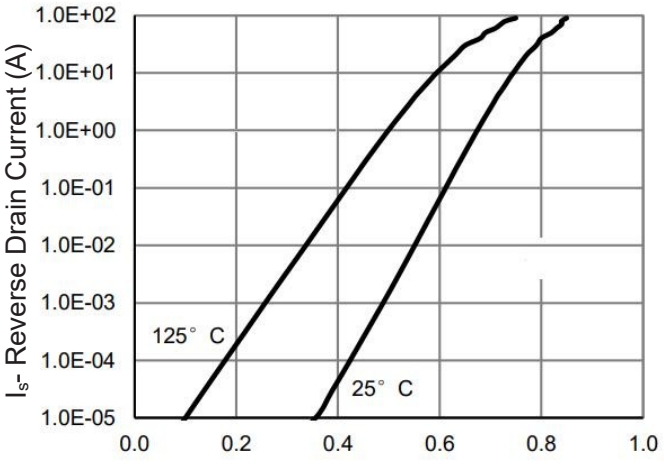


Figure 6 Source- Drain Diode Forward

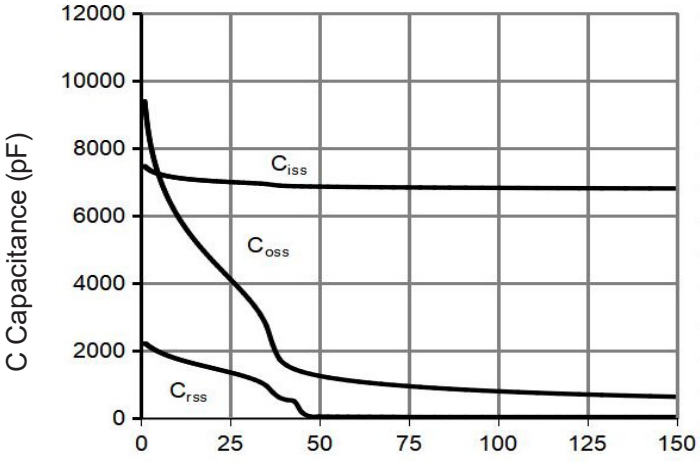


Figure 7 Capacitance vs Vds

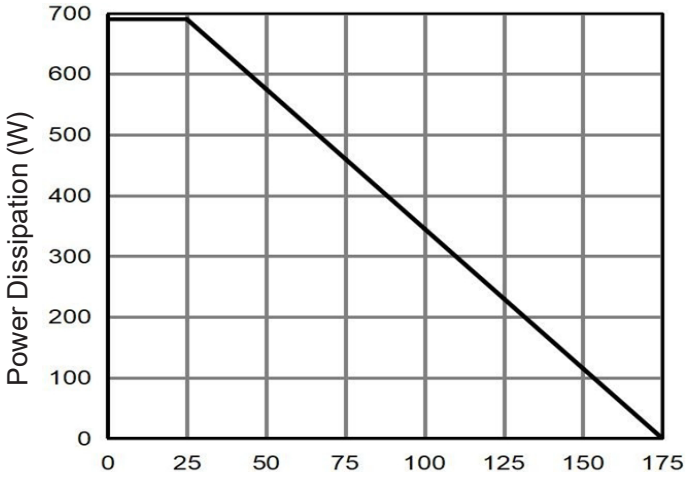


Figure 9 Power De-rating

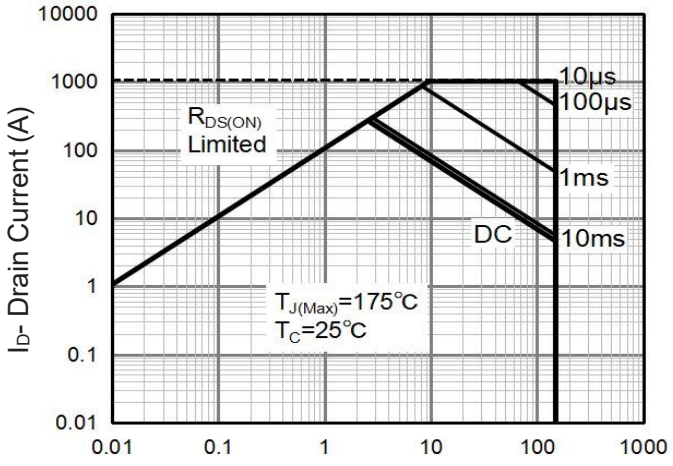


Figure 8 Safe Operation Area (Note3)

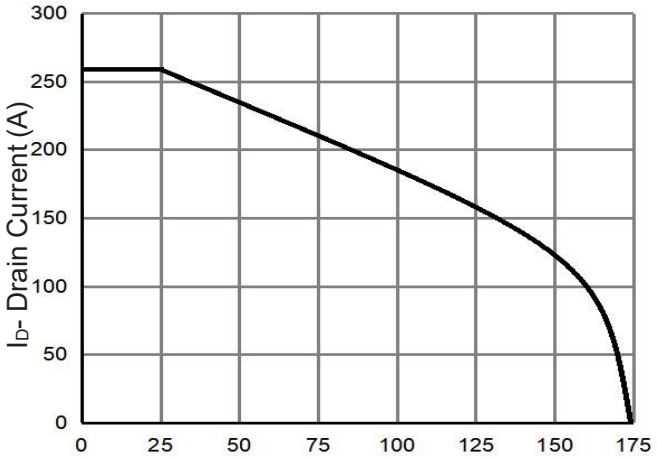


Figure 10 Current De-rating

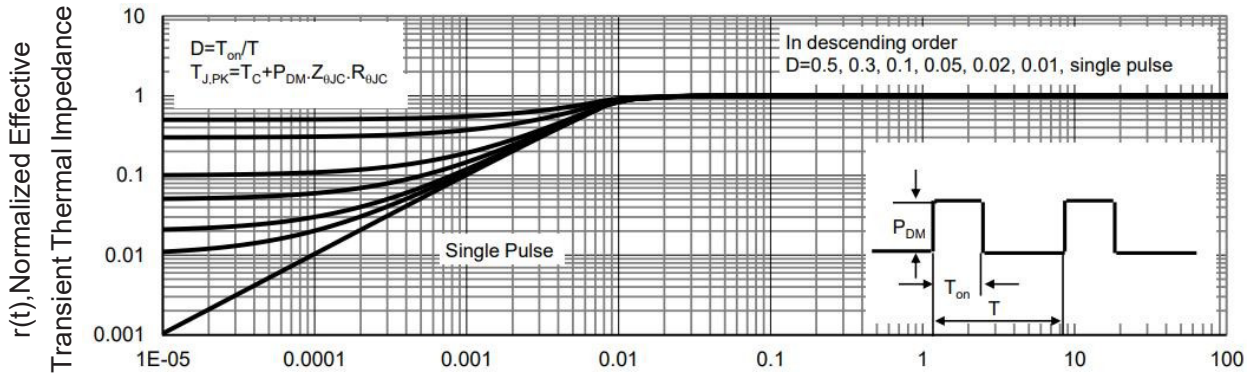


Figure 11 Normalized Maximum Transient Thermal Impedance