

General Description

The series of devices use advanced trench gate super junction technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This super junction MOSFET fits the industry's AC-DC SMPS requirements for PFC, AC/DC power conversion, and industrial power applications.

Features

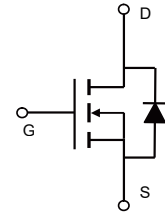
- Optimized body diode reverse recovery performance
- Low on-resistance and low conduction losses
- Small package
- Ultra Low Gate Charge cause lower driving requirements
- 100% Avalanche Tested
- ROHS compliant

Application

- Power factor correction (PFC)
- Switched mode power supplies(SMPS)
- Uninterruptible Power Supply (UPS)
- LLC Half-bridge



TO-252



Schematic

Parameter	Symbol	Value	Unit
Drain-Source Voltage ($V_{GS}=0V$)	V_{DS}	500	V
Gate-Source Voltage ($V_{DS}=0V$), AC ($f>1$ Hz)	V_{GS}	± 30	V
Gate-Source Voltage ($V_{DS}=0V$), DC	V_{GS}	± 20	V
Continuous Drain Current at $T_c=25^\circ C$	$I_{D(DC)}$	1.4	A
Continuous Drain Current at $T_c=100^\circ C$	$I_{D(DC)}$	0.98	A
Pulsed drain current (Note 1)	$I_{DM(pluse)}$	4.2	A
Maximum Power Dissipation($T_c=25^\circ C$)	P_D	18	W
Derate above $25^\circ C$		0.12	W/ $^\circ C$
Single pulse avalanche current (Note 2)	I_{AS}	1	A
Reverse diode dv/dt , $V_{DS} \leq 480V, I_{SD} < I_D$	dv/dt	15	V/ns
Drain Source voltage slope, $V_{DS} \leq 480V$	dv/dt	50	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55...+175	$^\circ C$

Table 2. Thermal Characteristic

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Maximum)	R_{thJC}	8.33	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient (Maximum)	R_{thJA}	62	$^{\circ}\text{C}/\text{W}$

Table 3. Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
On/off states						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250uA	500			V
Zero Gate Voltage Drain Current(Tc=25℃)	I _{DSS}	V _{DS} =500V,V _{GS} =0V			1	μA
Zero Gate Voltage Drain Current(Tc=125℃)	I _{DSS}	V _{DS} =500V,V _{GS} =0V			50	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V			±200	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250uA	2.5	3.2	4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =0.7A		2000	2250	mΩ
Dynamic Characteristics						
Gate Resistance	R _g	F=1MHZ, D-S short		3.1		Ω
Input Capacitance	C _{iss}	V _{DS} =50V,V _{GS} =0V, F=1MHz		58		pF
Output Capacitance	C _{oss}			8.6		pF
Reverse Transfer Capacitance	C _{rss}			4.2		pF
Total Gate Charge	Q _g	V _{DS} =350V,I _D =0.7A, V _{GS} =10V		4	6	nC
Gate-Source Charge	Q _{gs}			0.4		nC
Gate-Drain Charge	Q _{gd}			1.6		nC
Gate plateau voltage	V _{gp}			4		V
Switching times						
Turn-on Delay Time	t _{d(on)}	V _{DD} =380V,I _D =0.7A, R _G =5Ω,V _{GS} =10V		5		nS
Turn-on Rise Time	t _r			4		nS
Turn-Off Delay Time	t _{d(off)}			20		nS
Turn-Off Fall Time	t _f			36		nS
Source- Drain Diode Characteristics						
Source-drain current(Body Diode)	I _{SD}	T _C =25℃			1.4	A
Pulsed-Source-drain current(Body Diode)	I _{SDM}				4.2	A
Forward on voltage	V _{SD}	T _j =25℃,I _{SD} =1.4A,V _{GS} =0V		0.9	1.2	V
Reverse Recovery Time	t _{rr}	T _j =25℃,I _F =0.7A, di/dt=100A/μs		110		nS
Reverse Recovery Charge	Q _{rr}			0.33		uC
Peak reverse recovery current	I _{rm}			6		A

Notes: 1. Repetitive Rating: Pulse width limited by maximum junction temperature

2. $T_j=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, R_G=25\Omega$

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (curves)

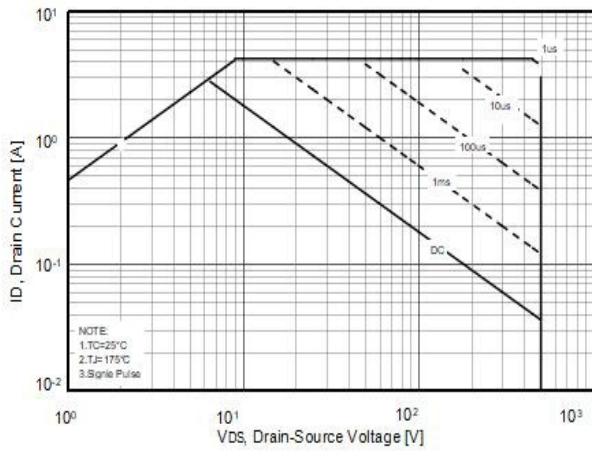
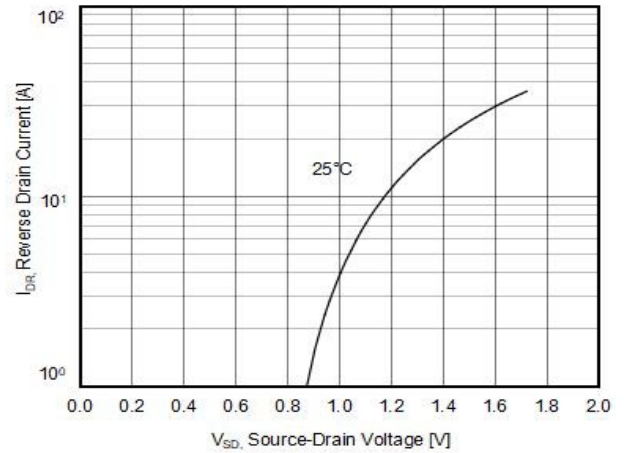
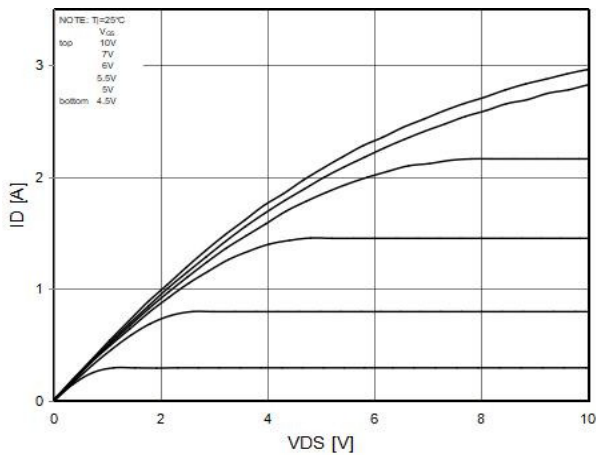
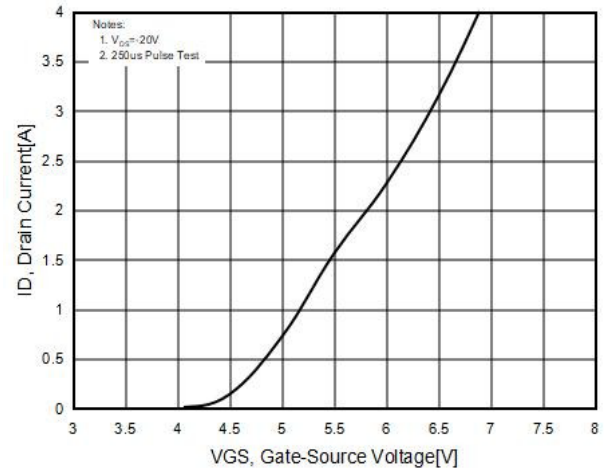
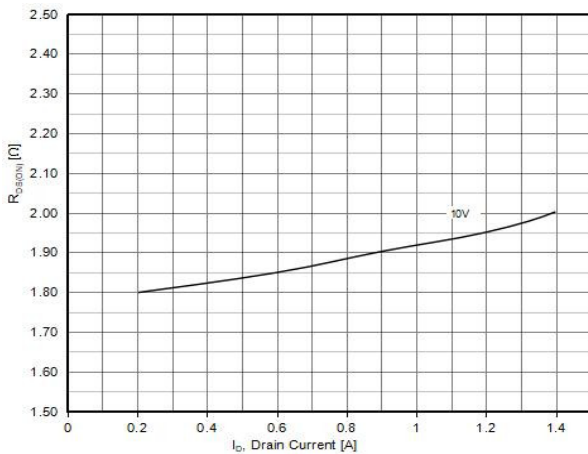
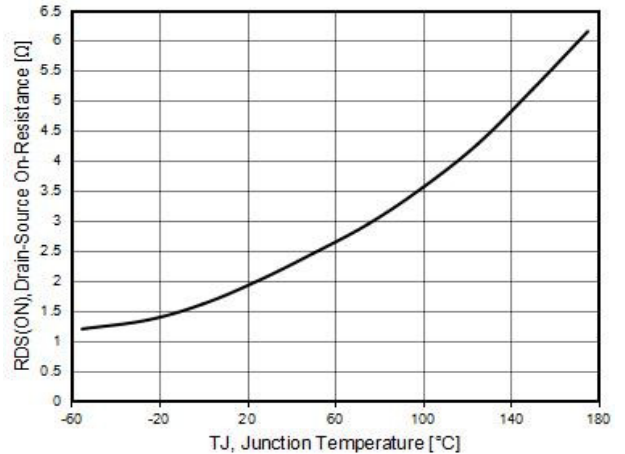
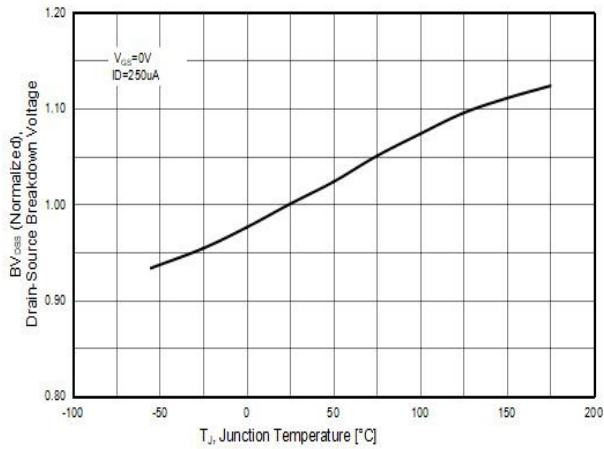
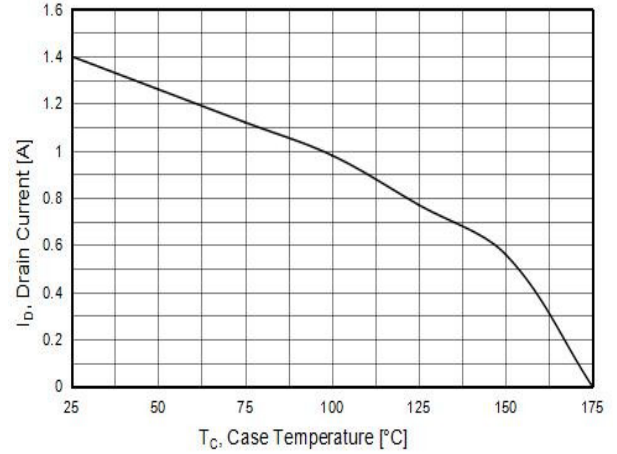
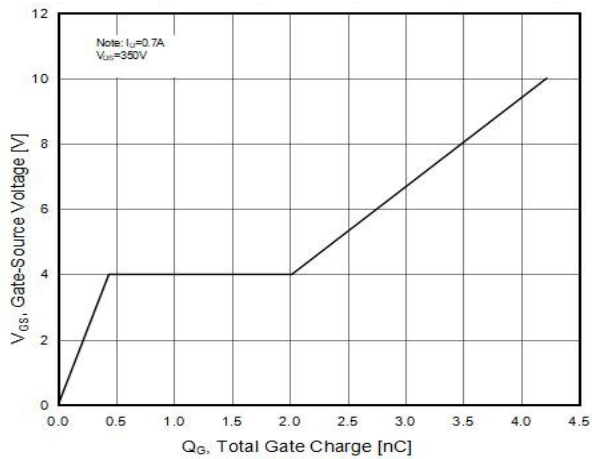
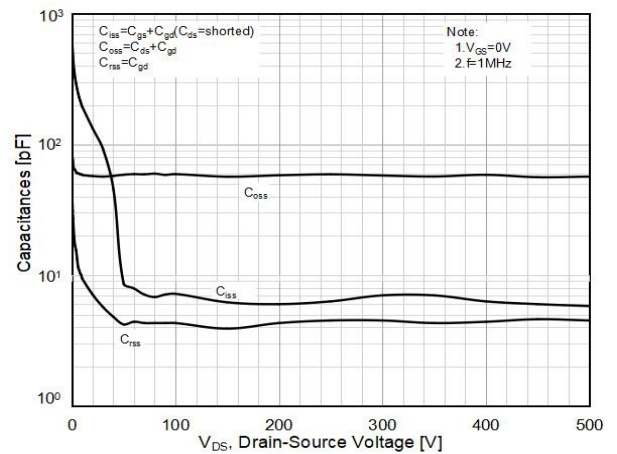
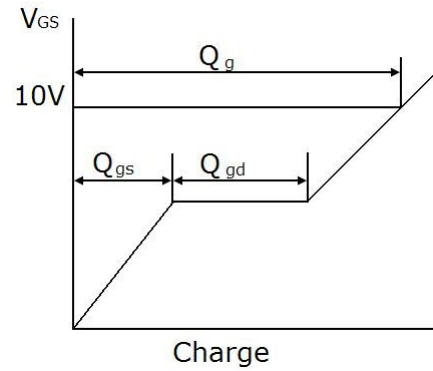
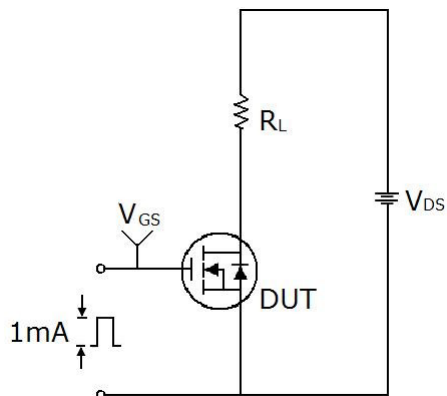
Figure1. Safe operating area

Figure2. Source-Drain Diode Forward Voltage

Figure3. Output characteristics

Figure4. Transfer characteristics

Figure5. Static drain-source on resistance

Figure6. $R_{DS(ON)}$ vs Junction Temperature


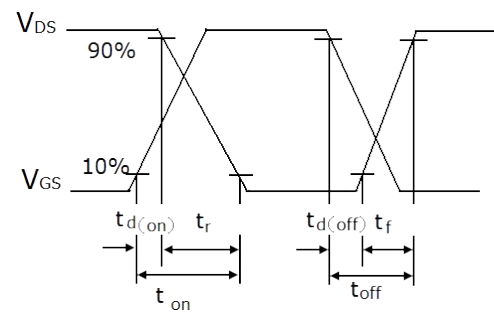
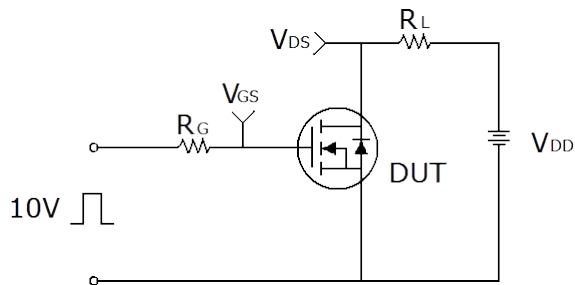
Figure7. BV_{DSS} vs Junction Temperature

Figure8. Maximum I_D vs Junction Temperature

Figure9. Gate charge waveforms

Figure10. Capacitance


Test circuit

1) Gate charge test circuit & Waveform



2) Switch Time Test Circuit:



3) Unclamped Inductive Switching Test Circuit & Waveforms

