

General Description

The series of devices use advanced trench gate super junction technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This super junction MOSFET fits the industry's AC-DC SMPS requirements for PFC, AC/DC power conversion, and industrial power applications.

Features

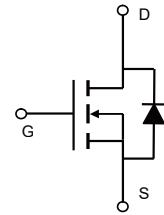
- Optimized body diode reverse recovery performance
- Low on-resistance and low conduction losses
- Small package
- Ultra Low Gate Charge cause lower driving requirements
- 100% Avalanche Tested
- ROHS compliant

Application

- Power factor correction (PFC)
- Switched mode power supplies(SMPS)
- Uninterruptible Power Supply (UPS)
- LLC Half-bridge



TO-220F



Schematic

Parameter	Symbol	Value	Unit
Drain-Source Voltage ($V_{GS}=0V$)	V_{DS}	650	V
Gate-Source Voltage ($V_{DS}=0V$) AC ($f>1$ Hz)	V_{GS}	± 30	V
Gate-Source Voltage ($V_{DS}=0V$) DC	V_{GS}	± 20	V
Continuous Drain Current at $T_c=25^\circ C$	$I_{D(DC)}$	13	A
Continuous Drain Current at $T_c=100^\circ C$	$I_{D(DC)}$	9.1	A
Pulsed drain current (Note 1)	$I_{DM(pluse)}$	39	A
Maximum Power Dissipation($T_c=25^\circ C$)	P_D	29.9	W
Derate above $25^\circ C$		0.2	W/ $^\circ C$
Avalanche current (Note 1)	I_{AS}	2.5	A
Drain Source voltage slope, $V_{DS} \leq 480$ V,	dv/dt	50	V/ns
Reverse diode dv/dt , $V_{DS} \leq 480$ V, $I_{SD} < I_D$	dv/dt	50	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55...+175	$^\circ C$

* limited by maximum junction temperature

Table 2. Thermal Characteristic

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Maximum)	R_{thJC}	5.0	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient (Maximum)	R_{thJA}	62	$^{\circ}\text{C}/\text{W}$

Table 3. Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
On/off states						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	650			V
Zero Gate Voltage Drain Current(Tc=25℃)	I _{DSS}	V _{DS} =650V, V _{GS} =0V			10	μA
Zero Gate Voltage Drain Current(Tc=125℃)	I _{DSS}	V _{DS} =650V, V _{GS} =0V			300	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	3.5	4.2	5.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =6.5A		265	300	mΩ
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, F=1.0MHz		877.0	950.0	pF
Output Capacitance	C _{oss}			33.5		pF
Reverse Transfer Capacitance	C _{rss}			8.1		pF
Total Gate Charge	Q _g	V _{DS} =480V, I _D =6.5A, V _{GS} =10V		20.7		nC
Gate-Source Charge	Q _{gs}			7.5		nC
Gate-Drain Charge	Q _{gd}			6.8		nC
Gate plateau voltage	V _{gp}			6.5		V
Intrinsic gate resistance	R _G	f = 1 MHz open drain		18		Ω
Switching times						
Turn-on Delay Time	t _{d(on)}	V _{DD} =380V, I _D =6.5A, R _G =1.7Ω, V _{GS} =10V		44		nS
Turn-on Rise Time	t _r			18		nS
Turn-Off Delay Time	t _{d(off)}			95		nS
Turn-Off Fall Time	t _f			28		nS
Source- Drain Diode Characteristics						
Source-drain current(Body Diode)	I _{SD}	T _C =25℃			13	A
Pulsed Source-drain current(Body Diode)	I _{SDM}				39	A
Forward On Voltage	V _{SD}	T _J =25℃, I _{SD} =13A, V _{GS} =0V		0.9	1.2	V
Reverse Recovery Time	t _{rr}	T _J =25℃, I _F =6.5A, di/dt=100A/μs		115		nS
Reverse Recovery Charge	Q _{rr}			0.875		uC
Peak Reverse Recovery Current	I _{rrm}			7.6		A

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2. $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, R_G=25\Omega$

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (curves)

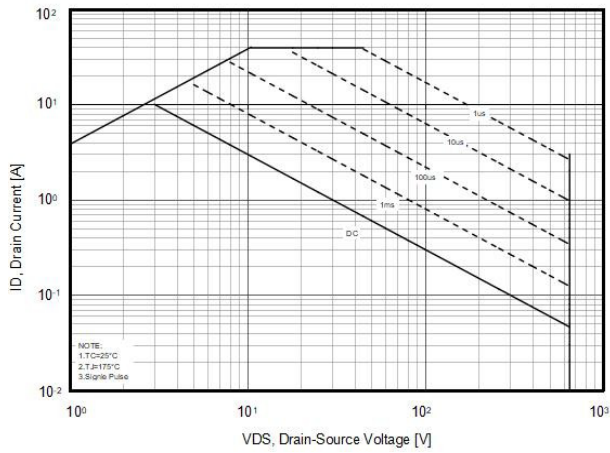
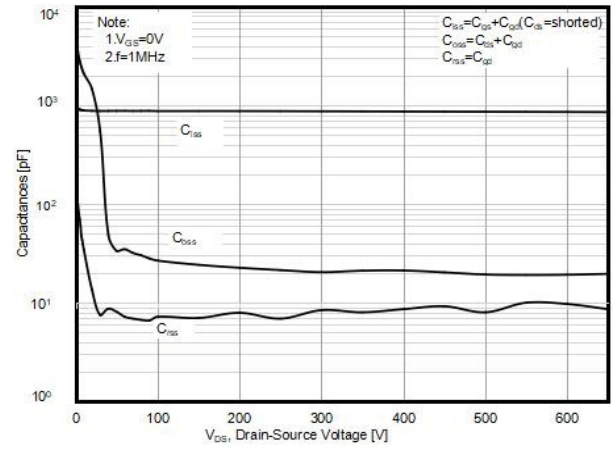
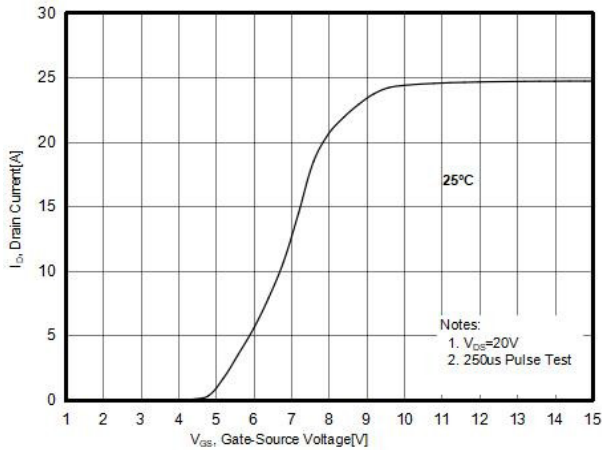
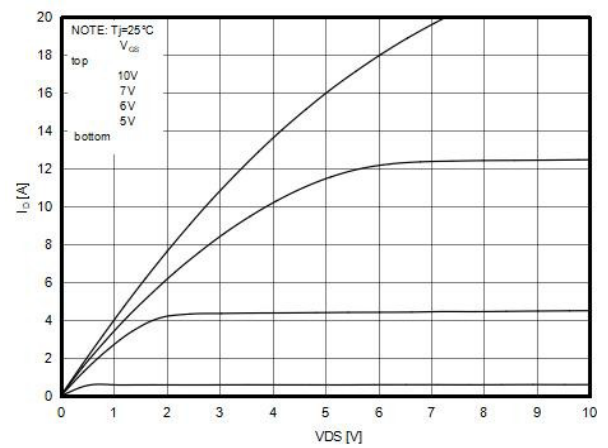
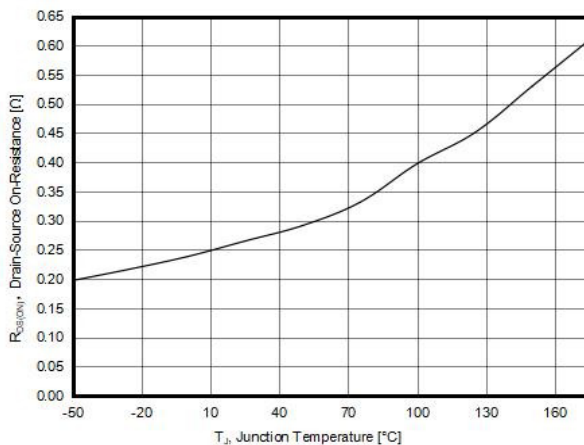
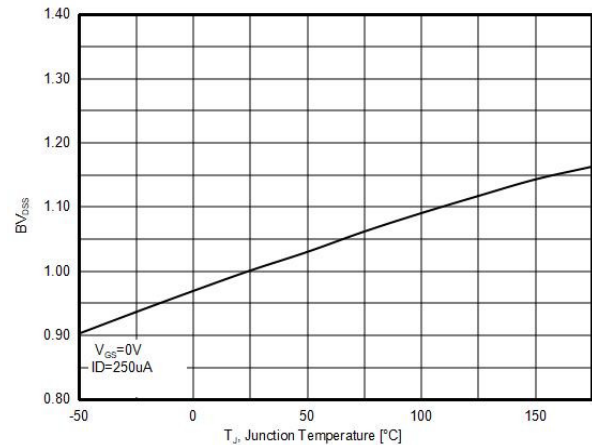
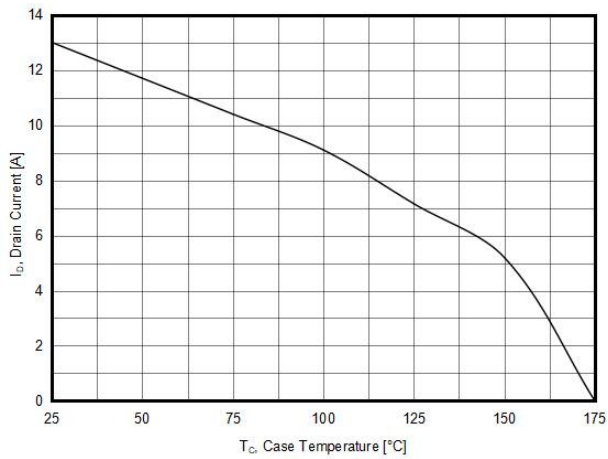
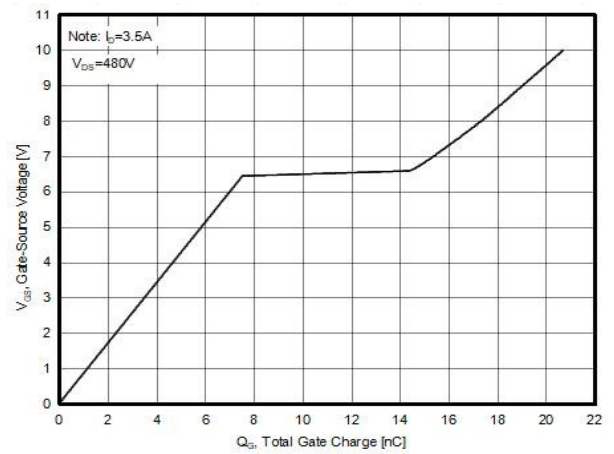
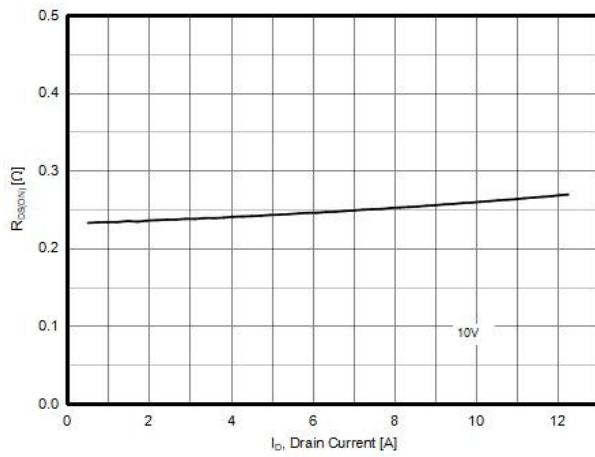
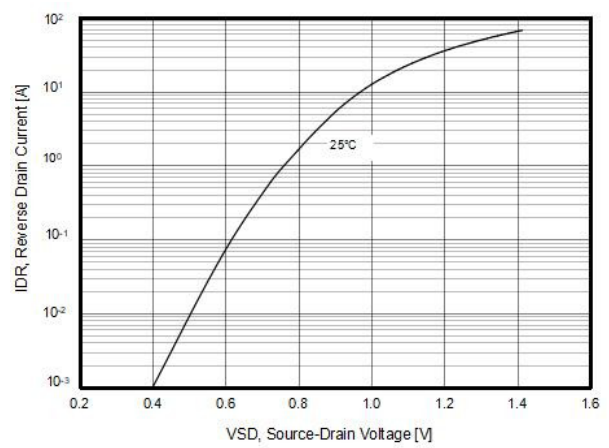
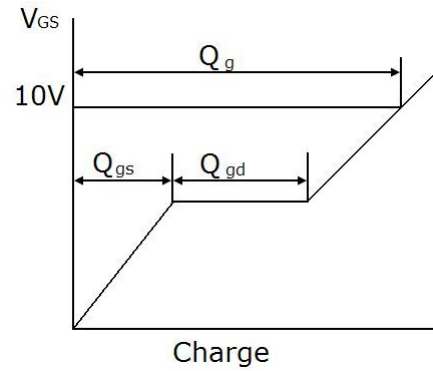
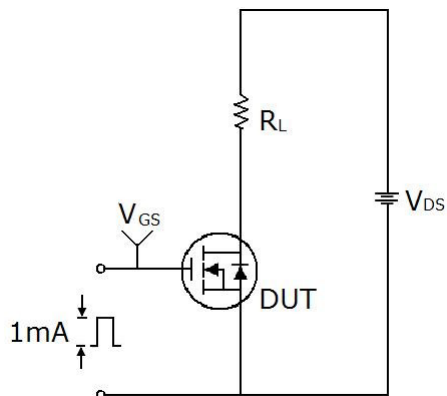
Figure1. Safe operating area

Figure2. Capacitance

Figure3. Transfer characteristics

Figure4. Output characteristics

Figure5. $R_{DS(ON)}$ vs Junction Temperature

Figure6. BV_{DSS} vs Junction Temperature


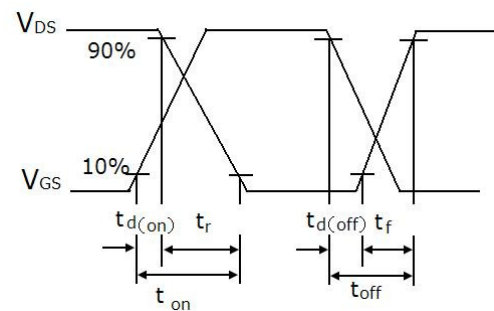
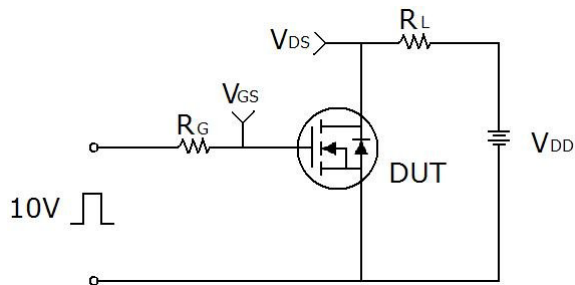
Figure7. Maximum I_D vs Junction Temperature

Figure8. Gate charge waveforms

Figure9. Static drain-source on resistance

Figure10. Source-Drain Diode Forward Voltage


Test circuit

1) Gate charge test circuit & Waveform



2) Switch Time Test Circuit:



3) Unclamped Inductive Switching Test Circuit & Waveforms

