General Description

The series of devices use advanced trench gate super junction technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This super junction MOSFET fits the industry's AC-DC SMPS requirements for PFC, AC/DC power conversion, and industrial power applications.

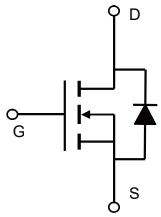
Features

- New technology for high voltage device
- Low on-resistance and low conduction losses
- Small package
- Ultra Low Gate Charge cause lower driving requirements
- 100% Avalanche Tested
- ROHS compliant

Application

- Power factor correction（PFC）
- Switched mode power supplies(SMPS)
- Uninterruptible Power Supply（UPS）

TO-220



Schematic

Parameter	Symbol	Q1	Q2	Unit
Drain-Source Voltage (V_{GS}=0V）	V_{DS}	650		V
Gate-Source Voltage (V_{DS}=0V) AC (f>1 Hz)	V_{GS}	±30		V
Continuous Drain Current at Tc=25°C	$I_{D\ (DC)}$	28	28*	A
Continuous Drain Current at Tc=100°C	$I_{D\ (DC)}$	18	18*	A
Pulsed drain current **(Note 1)**	$I_{DM\ (pluse)}$	112	112*	A
Maximum Power Dissipation(Tc=25℃) Derate above 25°C	P_D	260 2.08	35 0.28	W W/°C
Single pulse avalanche energy **(Note 2)**	E_{AS}	676		mJ
Avalanche current **(Note 1)**	I_{AR}	5.2		A
Repetitive Avalanche energy ， t_{AR} limited by T_{jmax} **(Note 1)**	E_{AR}	3.2		mJ

Parameter	Symbol	Q1	Q2	Unit
Drain Source voltage slope, V_{DS} ≤480 V,	dv/dt	50		V/ns
Reverse diode dv/dt， V_{DS} ≤480 V,I_{SD}<I_D	dv/dt	15		V/ns
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55...+150		°C

* limited by maximum junction temperature

Table 2. Thermal Characteristic

Parameter	Symbol	Q1	Q2	Unit
Thermal Resistance，Junction-to-Case（Maximum）	R_{thJC}	0.48	3.57	°C /W
Thermal Resistance，Junction-to-Ambient （Maximum）	R_{thJA}	62	80	°C /W

Table 3. Electrical Characteristics (TA=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
On/off states						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	650			V
Zero Gate Voltage Drain Current(Tc=25℃)	I_{DSS}	V_{DS}=650V,V_{GS}=0V			1	μA
Zero Gate Voltage Drain Current(Tc=125℃)	I_{DSS}	V_{DS}=650V,V_{GS}=0V			100	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	3	3.5	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=14A		110	130	mΩ
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=50V,V_{GS}=0V, F=1.0MHz		2070		pF
Output Capacitance	C_{oss}			120		pF
Reverse Transfer Capacitance	C_{rss}			0.5		pF
Total Gate Charge	Q_g	V_{DS}=480V,I_D=28A, V_{GS}=10V		37.5		nC
Gate-Source Charge	Q_{gs}			13		nC
Gate-Drain Charge	Q_{gd}			11.5		nC
Switching times						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=380V,I_D=14A, R_G=2.3Ω,V_{GS}=10V		14		nS
Turn-on Rise Time	t_r			12		nS
Turn-Off Delay Time	$t_{d(off)}$			65		nS
Turn-Off Fall Time	t_f			11		nS
Source- Drain Diode Characteristics						
Source-drain current(Body Diode)	I_{SD}	T_C=25°C			28	A
Pulsed Source-drain current(Body Diode)	I_{SDM}				112	A
Forward On Voltage	V_{SD}	Tj=25°C,I_{SD}=28A,V_{GS}=0V		0.9	1.2	V
Reverse Recovery Time	t_{rr}	Tj=25°C,I_F=14A,di/dt=100A/μs		350		nS
Reverse Recovery Charge	Q_{rr}			5.4		uC
Peak Reverse Recovery Current	I_{rrm}			31		A

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2. Tj=25℃,VDD=50V,VG=10V, R_G=25Ω

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (curves)

Figure1. Safe operating area

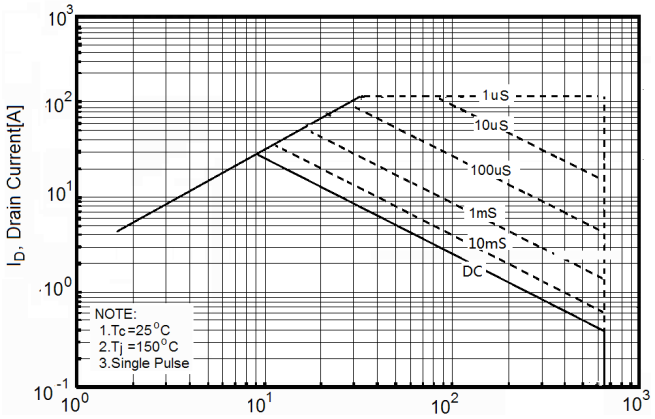


Figure2. Safe operating area for TO-220F

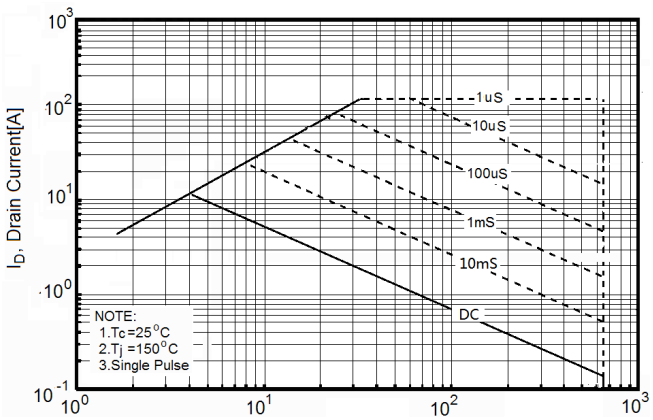


Figure3. Source-Drain Diode Forward Voltage

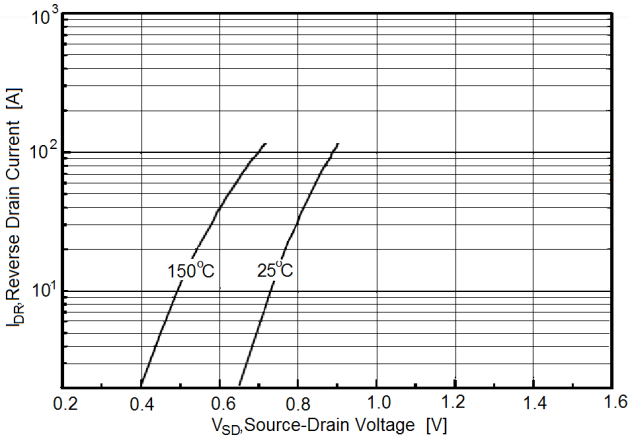


Figure4. Output characteristics

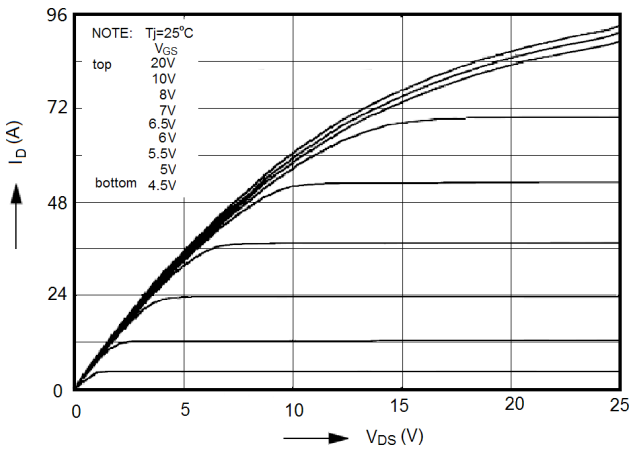


Figure5. Transfer characteristics

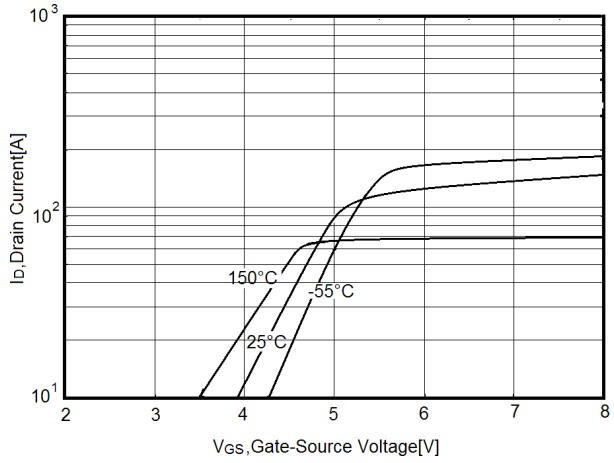


Figure6. Static drain-source on resistance

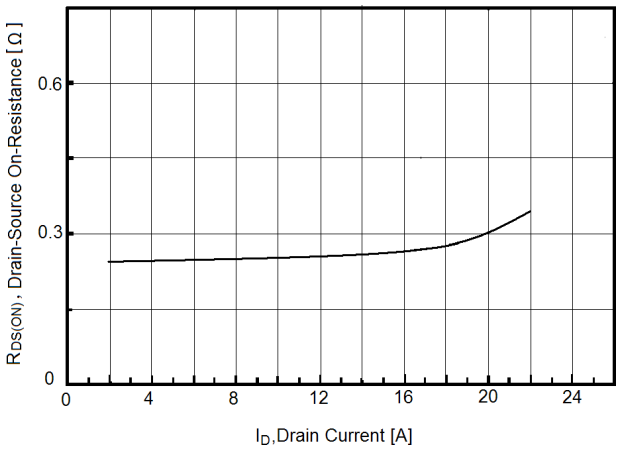


Figure7. $R_{DS(ON)}$ vs Junction Temperature

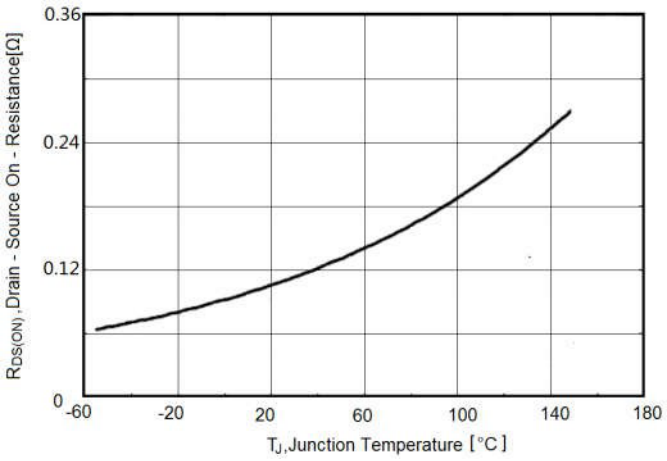


Figure8. BV_{DSS} vs Junction Temperature

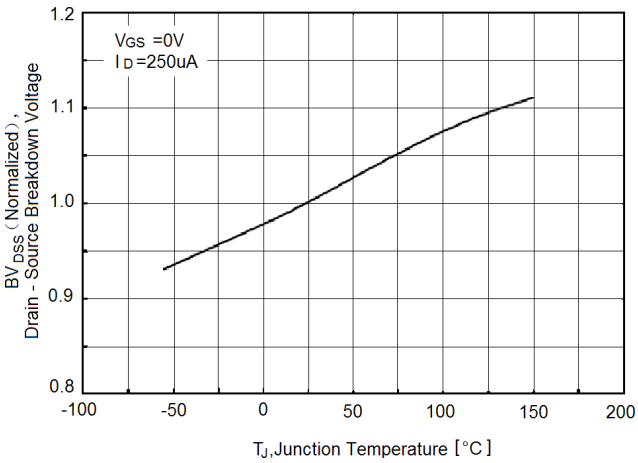


Figure9. Maximum I_D vs Junction Temperature

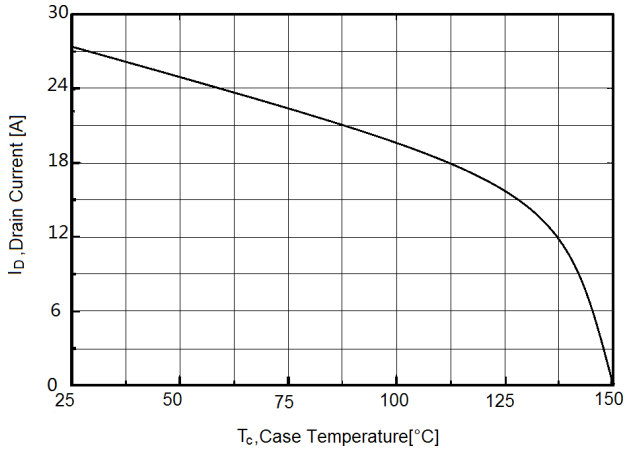


Figure10. Gate charge waveforms

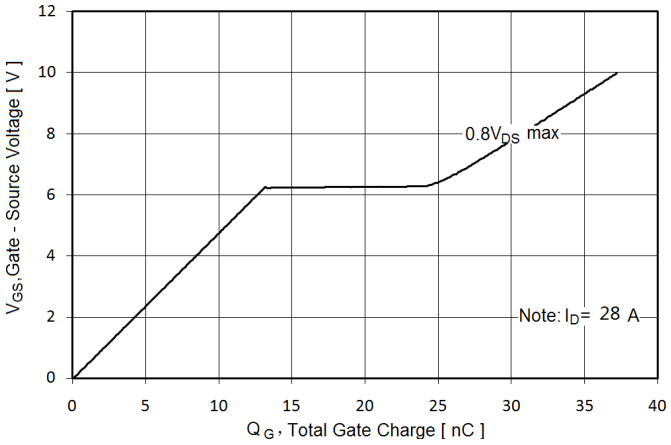


Figure11. Capacitance

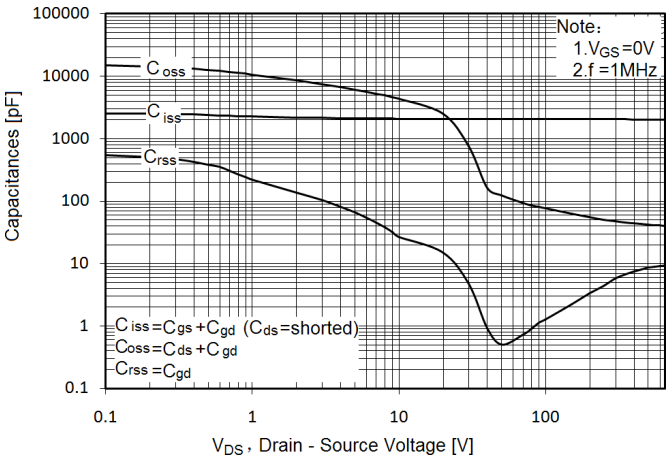


Figure12. Transient Thermal Impedance

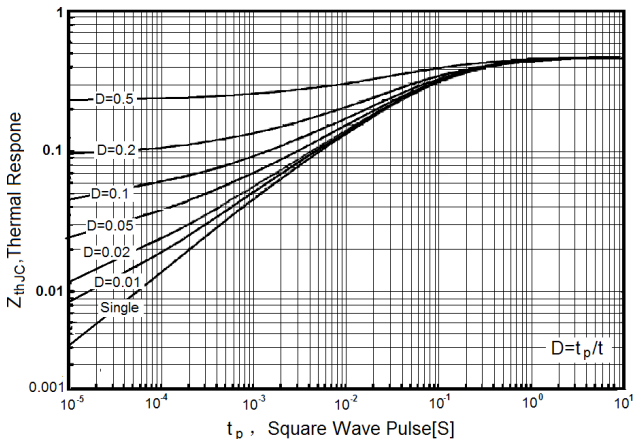
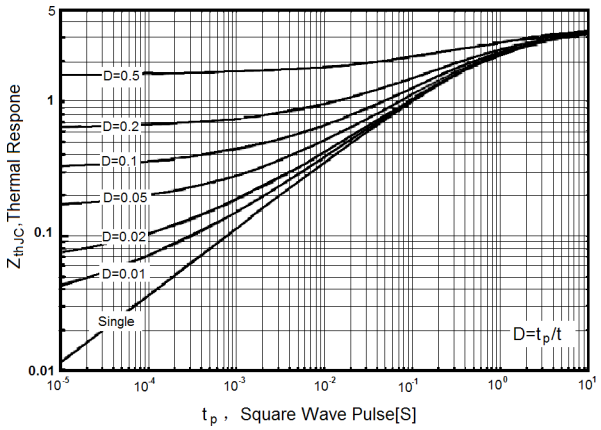
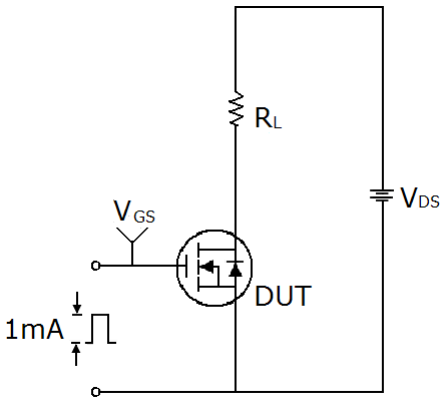


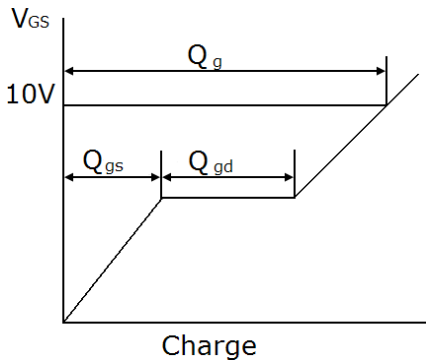
Figure13. Transient Thermal Impedance for TO-220F



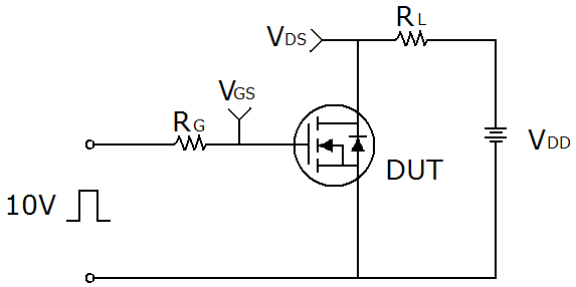
Test circuit

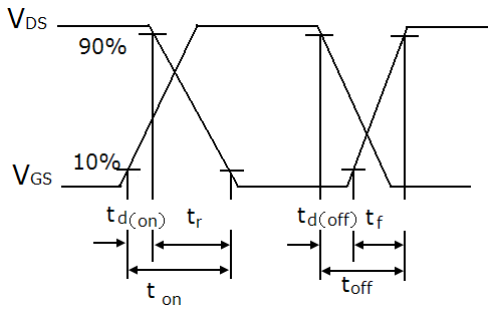
1） **Gate charge test circuit & Waveform**





2） **Switch Time Test Circuit:**





3） **Unclamped Inductive Switching Test Circuit & Waveforms**